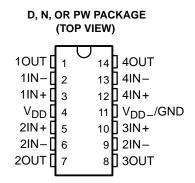
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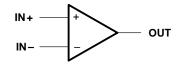
- A-Suffix Versions Offer 5-mV V_{IO}
- B-Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise ... 25 nV/\(\vee{Hz}\) Typ at f = 1 kHz (High-Bias Version)

description

The TLC254, TLC254A, TLC254B, TLC25L4, TLC254L4A, TLC254L4B, TLC25M4, TLC25M4A and TL25M4B are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS[™]



symbol (each amplifier)



process, giving them stable input-offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for these devices include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS operational amplifiers without the power penalties of traditional bipolar devices.

		Availabl	e options		
	Viemov	PAC	KAGED DEVICES		CHIP FORM
TA	V _{IO} max AT 25°C	SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	(Y)
	10 mV 5 mV 2 mV	TLC254CD TLC254ACD TLC254BCD	TLC254ACN — TLC254BCN —	TLC254Y — —	
0°C to 70°C	10 mV 5 mV 2 mV	TLC25L4CD TLC25L4ACD TLC25L2BCD	TLC25L4CN TLC25L4ACN TLC25L4BCN	TLC25L4CPW — —	TLC25L4Y — —
	10 mV 5 mV 2 mV	TLC25M4CD TLC25M4ACD TLC25M4BCD	TLC25M4CN TLC25M4ACN TLC25M4BCN	TLC25M4CPW — —	TLC25M4Y — —

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC254CDR). Chips are tested at 25°C.

LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description (continued)

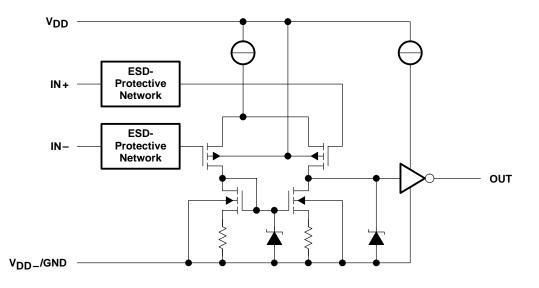
General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with these devices. Remote and inaccessible equipment applications are possible using their low-voltage and low-power capabilities. These devices are well suited to solve the difficult problems associated with single-battery and solar-cell-powered applications. This series includes devices that are characterized for the commercial temperature range and are available in 14-pin plastic dip and the small-outline packages. The device is also available in chip form.

These devices are characterized for operation from 0°C to 70°C.

	DEVICE FEATURES	-	
PARAMETER	TLC25L4_C (LOW BIAS)	TLC25M4_C (MEDIUM BIAS)	TLC254_C (HIGH BIAS)
Supply current (Typ)	40 µA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/µA	0.6 V/μA	4.5 V/μA
Input offset voltage (Max) TLC254C, TLC25L4C, TLC25M4C TLC254AC, TLC25L4AC, TLC25M4AC TLC254BC, TLC25L4BC, TLC25M4BC	10 mV 5 mV 2 mV	10 mV 5 mV 2 mV	10 mV 5 mV 2 mV
Offset voltage drift (Typ)	0.1 μ V/month [†]	0.1 μV/month [†]	0.1 μ V/month [†]
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

[†] The long-term drift value applies after the first month.

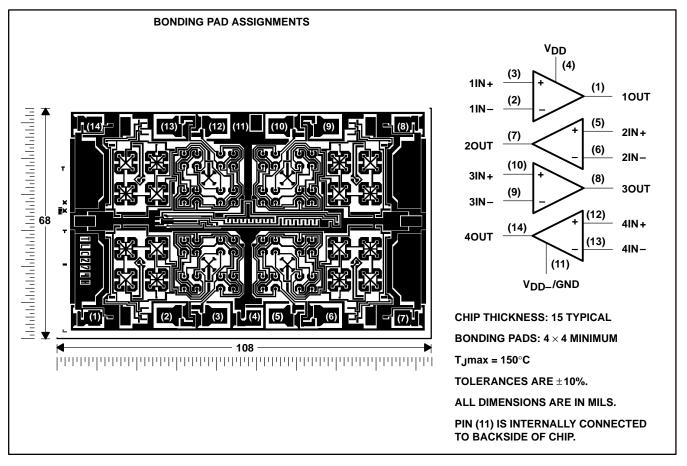
equivalent schematic (each amplifier)





chip information

These chips, when properly assembled, display characteristics similar to the TLC25_4C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{DD} (see Note 1)	18 V
Differential input voltage (see Note 2)	
Input voltage range (any input)	0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	. See Dissipation Rating Table
Operating free-air temperature range	0°C to 70°C
Storage temperature range	65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_D_/GND.

2. Differential voltages are at IN+, with respect to IN-.

3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

	DISSIFAT	ION RATING TABLE	
PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
N	1050 mW	9.2 mW/°C	736 mW
PW	700 mW	5.6 mW/°C	448 mW

DISSIPATION RATING TABLE

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V _{DD}		1.4	16	V
	V _{DD} = 1.4 V	0	0.2	
Common-mode input voltage, VIC	$V_{DD} = 5 V$	-0.2	4	V
Common-mode input voltage, vic	V _{DD} = 10 V	-0.2	9	v
	V _{DD} = 16 V	-0.2	14	
Operating free-air temperature, T_A		0	70	°C



SLOS003G – JUNE 1983 – REVISED MARCH 2001	Lincmos TM QUAD OPERATIONAL AMPLIFIERS	TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y	TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B
ED MARCH 2001	IPLIFIERS	LC25M4Y	FLC25L4B

				_	TL	.C254_C	;	TL	C25L4_	c	TLO	C25M4_	C	
	PARAMETER		TEST CONDITIONS [†]	TA	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
		TLC25_4C		25°C			10			10			10	
		12025_40		0°C to 70°C			12			12			12	
VIO	Input offset voltage	TLC25_4AC	$V_{O} = 0.2 V, R_{S} = 50 \Omega$	25°C			5			5			5	mV
٩O	input onset voltage	16020_4A0	$V_0 = 0.2 V, V_0 = 50 S_2$	0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
		12023_400		0°C to 70°C			3			3			3	
aVIO	Average temperature input offset voltage	coefficient of		25°C to 70°C		1			1			1		μV/°C
l. a	Innut offent ourrent			25°C		1	60		1	60		1	60	
ΙΟ	Input offset current		V _O = 0.2 V	0°C to 70°C			300			300			300	рA
lin.	Input bias current		V _O = 0.2 V	25°C		1	60		1	60		1	60	рА
lΒ	input bias current		VO = 0.2 V	0°C to 70°C			600			600			600	
VICR	Common-mode input	voltage range		25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
VOM	Peak output voltage s	wing‡	V _{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A _{VD}	Large-signal differenti amplification	al voltage	V_{O} = 100 to 300 mV, R _S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode reject	tion ratio	V _O = 0.2 V, V _{IC} = V _{ICR} min	25°C	60	77		60	77		60	77		dB
IDD	Supply current		$V_{O} = 0.2 V$, No load	25°C		600	750		50	68		400	500	μA

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: for low bias, R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.
[‡] The output swings to the potential of V_{DD}_/GND.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	Т	TLC254_C		TLC25L4_C			TLC25M4_C			UNIT
	FARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	See Figure 1		0.1			0.001			0.01		V/µs
B ₁	Unity-gain bandwidth	$\begin{array}{lll} A_V = 40 \ dB, & C_L = 10 \ pF, \\ R_S = 50 \ \Omega, & See Figure 1 \end{array}$		12			12			12		kHz
	Overshoot factor	See Figure 1		30%			35%			35%		

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST CONI	DITIONS	TAT		4, TLC2 _C254B(UNIT
						MIN	TYP	MAX	
		TLC254C	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		1202540	R _S = 50 Ω,	$R_L = 10 k\Omega$	Full range			12	
Via	Input offect voltage	TLC254AC	V _O = 1.4 V,	VIC = 0,	25°C		0.9	5	mV
VIO	Input offset voltage	TLC254AC	R _S = 50 Ω,	$R_L = 10 \ k\Omega$	Full range			6.5	IIIV
		TLC254BC	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.34	2	
		1023460	R _S = 50 Ω,	$R_L = 10 k\Omega$	Full range			3	
αΛΙΟ	Average temperature coeffici offset voltage	ient of input			25°C to 70°C		1.8		μV/°C
h	lanut affact current (can blatt	. 4)			25°C		0.1	60	4
IO	Input offset current (see Note	e 4)	V _O = 2.5 V,	V _{IC} = 2.5 V	70°C		7	300	pА
L.=	lanut hing summark (and Nieto	4)			25°C		0.6	60	
IВ	Input bias current (see Note	4)	V _O = 2.5 V,	$V_{IC} = 2.5 V$	70°C		40	600	pА
	Common-mode input voltage	rande			25°C	-0.2 to 4	-0.3 to 4.2		
VICR	Common-mode input voltage range (see Note 5)	range			Full range	-0.2 to 3.5			V
					0°C	3	3.8		
Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \ k\Omega$	25°C	3.2	3.8		V
					70°C	3	3.8		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
					0°C	4	27		
AVD	Large-signal differential volta amplification	ige	$V_{O} = 0.25 V \text{ to } 2 V,$	$R_L = 10 \ k\Omega$	25°C	5	23		V/mV
					70°C	4	20		
					0°C	60	84		
CMRR	Common-mode rejection rati	0	$V_{IC} = V_{ICR}min$		25°C	65	80		dB
					70°C	60	85		
					0°C	60	94		
^k SVR	Supply-voltage rejection ratio	$(\Delta V_{DD}/\Delta V_{IO})$	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	25°C	65	95		dB
					70°C	60	96		
			V _O = 2.5 V,	V _{IC} = 2.5 V,	0°C		3.1	7.2	
IDD	Supply current (four amplifier	rs)	No load	ν _{IC} = 2.5 v,	25°C		2.7	6.4	mA
					70°C		2.3	5.2	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	TAT		C, TLC2 C254B		UNIT
						MIN	TYP	MAX	
		TL 005 40	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLC254C	R _S = 50 Ω,	$R_L = 10 k\Omega$	Full range			12	
\/	Input offent voltage		V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	
VIO	Input offset voltage	TLC254AC	R _S = 50 Ω,	$R_L = 10 k\Omega$	Full range			6.5	mV
		TLC254BC	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.39	2	
		TLC254BC	R _S = 50 Ω,	$R_L = 10 \text{ k}\Omega$	Full range			3	
∝VIO	Average temperature coeffi offset voltage	cient of input			25°C to 70°C		2		μV/°C
	Unser Voltage				25°C		0.1	60	
10	Input offset current (see No	ote 4)	V _O = 5 V,	V _{IC} = 5 V	70°C		7	300	pА
					25°C		0.7	60	
IВ	Input bias current (see Note	e 4)	V _O = 5 V,	V _{IC} = 5 V	70°C		50	600	pА
					100	-0.2	-0.3	000	
					25°C	to	to		
Vion	Common-mode input voltage	ge range				9	9.2		v
VICR	(see Note 5)	(see Note 5)				-0.2			v
					Full range	to 8.5			
					0°C	7.8	8.5		
∨он	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \ k\Omega$	25°C	8	8.5		v
011	ngin ioron output ronago				70°C	7.8	8.4		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
0L				0L	70°C		0	50	
					0°C	7.5	42		
AVD	Large-signal differential vol	tage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 10 \ k\Omega$	25°C	10	36		V/m\
	amplification		-	_	70°C	7.5	32		
					0°C	60	88		
CMRR	Common-mode rejection ra	itio	$V_{IC} = V_{ICR}min$		25°C	65	85		dB
					70°C	60	88		
					0°C	60	94		
k SVR	Supply-voltage rejection rat (ΔVDD/ΔVIO)	tio	$V_{DD} = 5 V$ to 10 V,	V _O = 1.4 V	25°C	65	95		dB
					70°C	60	96		
				N	0°C		4.5	8.8	
IDD	Supply current (four amplifi	ers)	V _O = 5 V, No load	V _{IC} = 5 V,	25°C		3.8	8	mA
					70°C		3.2	6.8	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



operating characteristics, V_{DD} = 5 V

	PARAMETER	т	EST CONDITIO	NS	TA	TLC254 TL	C, TLC2 C254BC		UNIT	
						MIN	TYP	MAX		
				VI(PP) = 1 V	0°C		4			
				VI(PP) = 1 V	25°C		3.6			
SR	Slew rate at unity gain	$R_L = 10 k\Omega$,	C _L = 20 pF,	V _{I(PP)} = 1 V	70°C		3)//uo	
SK	Siew rate at unity gain	See Figure 1			0°C		3.1		V/μs	
				V _{I(PP)} = 2.5 V	25°C		2.9			
					70°C		2.5			
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω,	See Figure 2	25°C		25		nV/√Hz	
				_	0°C		340			
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	$R_L = 10 k\Omega$,	25°C		320		kHz	
		See Figure 1			70°C		260			
					0°C		2			
B ₁	Unity-gain bandwidth	V _I = 10 mV,	C _L = 20 pF,	See Figure 1	25°C		1.7		MHz	
					70°C		1.3			
		N 40 M	<i>.</i> .	0 00 5	0°C		47°			
φm	Phase margin	VI = 10 mV, See Figure 3	$f = B_1,$	C _L = 20 pF,	25°C		46°			
					70°C		43°			

operating characteristics, $V_{DD} = 10 V$

	PARAMETER	т	EST CONDITIO	NS	Тд	TLC254 TL	C, TLC2 .C254B(UNIT	
						MIN	TYP	MAX		
					0°C		5.9			
				VI(PP) = 1 V	25°C		5.3			
SR	Slew rate at unity gain	$R_L = 10 k\Omega$,	C _L = 20 pF,		70°C		4.3		V/µs	
SK	Siew rate at unity gain	See Figure 1			0°C		5.1		v/µS	
				VI(PP) = 5.5 V	25°C		4.6			
					70°C		3.8			
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω,	See Figure 2	25°C		25		nV/√Hz	
					0°C		220			
Вом	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	$R_{L} = 10 k\Omega$,	25°C		200		kHz	
		Occ riguie i			70°C		140			
					0°C		2.5			
B ₁	Unity-gain bandwidth	Vj = 10 mV,	CL = 20 pF,	See Figure 1	25°C		2.2		MHz	
					70°C		1.8			
		10	<u> </u>	0 00 -5	0°C		50°			
φm	Phase margin	V _I = 10 mV, See Figure 3	f = B ₁ ,	C _L = 20 pF,	25°C		49°			
		See Figure 6			70°C		46°			



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	τ _A †	TL	LC25L40 C25L4A C25L4B	C	UNIT
						MIN	TYP	C MAX 10 12 5 6.5 2	
		TLC25L4C	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		12023240	R _S = 50 Ω,	$R_L = 1 M\Omega$	Full range			12	
VIO	Input offset voltage	TLC25L4AC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	mV
٩O	input onset voltage	TEOZOLANO	R _S = 50 Ω,	$R_L = 1 M\Omega$	Full range			6.5	IIIV
		TLC25L4BC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.24	2	
		120202400	R _S = 50 Ω,	$R_L = 1 M\Omega$	Full range			3	
∝VIO	Average temperature coef	icient of input			25°C to 70°C		1.1		μV/°C
lia	Input offset current (see N	oto (1)	V _O = 2.5 V,	VIC = 2.5 V	25°C		0.1	60	pА
١O	input onset current (see N	Jle 4)	VO = 2.5 V,	VIC = 2.5 V	70°C		7	300	рА
lin.	Input bias current (see Not	·• 1)	V _O = 2.5 V,	VIC = 2.5 V	25°C		0.6	60	pА
IВ	input bias current (see No	.e 4)	V() = 2.3 V,	VIC = 2.5 V	70°C		40	600	РА
	Common-mode input volta	ge range			25°C	-0.2 to 4	-0.3 to 4.2		V
VICR	(see Note 5)	gorango			Full range	-0.2 to 3.5			V
					0°C	3	4.1		
Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 1 M\Omega$	25°C	3.2	4.1		V
					70°C	3	4.2		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
		14			0°C	50	680		
AVD	Large-signal differential vo amplification	itage	$V_{O} = 0.25 V \text{ to } 2 V,$	$R_L = 1 M\Omega$	25°C	50	520		V/mV
					70°C	50	380		
					0°C	60	95		
CMRR	Common-mode rejection ra	atio	VIC = VICRmin		25°C	65	94		dB
					70°C	60	95		
	Cupply voltone relation	tio			0°C	60	97		
k SVR	Supply-voltage rejection ra $(\Delta V_{DD}/\Delta V_{IO})$	IIIO	V_{DD} = 5 V to 10 V,	V _O = 1.4 V	25°C	70	98		dB
					70°C	60	97		
			$V_{0} = 25 V_{0}$	$V_{10} = 25 V_{10}$	0°C		48	84	
IDD	Supply current (four amplifiers)	$V_{O} = 2.5 V,$ V_{IO} No load	V _{IC} = 2.5 V,	25°C		40	68	μA	
				70°C		31	56		

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	τ _A †	TL	LC25L40 C25L4A C25L4B	С	UNIT
						MIN	TYP	C MAX 10 12 5 6.5 2	
		TLC25L4C	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		1.1	10	
		12023240	R _S = 50 Ω,	$R_L = 1 M\Omega$	Full range			12	
VIO	Input offset voltage	TLC25L4AC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	mV
٩O	input onoet voltage	1202024/10	R _S = 50 Ω,	$R_L = 1 M\Omega$	Full range			6.5	iiiv
		TLC25L4BC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.26	2	
		120202480	R _S = 50 Ω,	$R_L = 1 M\Omega$	Full range			3	
αΛΙΟ	Average temperature coef input offset voltage	ficient of			25°C to 70°C		1		μV/°C
lio	Input offset current (see N	ote 1)	$V_{0} = 5 V$	$V_{10} = 5 V$	25°C		0.1	60	nA
ΙΟ	Input offset current (see N		V _O = 5 V,	V _{IC} = 5 V	70°C		7	300	pА
lun	Input bias current (see No	to (1)	V _O = 5 V,	V _{IC} =.5 V	25°C		0.7	60	pА
IВ	input bias current (see No	(le 4)	$v_{\rm O} = 5 v$,	VIC =.5 V	70°C		50	600	рА
.,	Common-mode input volta	age range (see			25°C	-0.2 to 9	-0.3 to 9.2		V
VICR	Note 5)	5			Full range	-0.2 to 8.5			V
					0°C	7.8	8.9		
Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 1 M\Omega$	25°C	8	8.9		V
					70°C	7.8	8.9		
					0°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
					0°C	50	1025		
AVD	Large-signal differential vo amplification	oltage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 1 M\Omega$	25°C	50	870		V/mV
	amplineation				70°C	50	660		
					0°C	60	97		
CMRR	Common-mode rejection r	atio	$V_{IC} = V_{ICR}min$		25°C	65	97		dB
					70°C	60	97		
					0°C	60	97		
ksvr	Supply-voltage rejection ra $(\Delta V_{DD}/\Delta V_{IO})$	atio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	25°C	70	97		dB
					70°C	60	98		
			<u> </u>	N/ = N/	0°C		72	132	
IDD	Supply current (four ampli	fiers)	$V_{O} = 5 V$, No load	V _{IC} = 5 V,	25°C		57	92	μA
			No load		70°C		44	80	

[†]Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



operating characteristics, $V_{DD} = 5 V$

	PARAMETER	ТЕ	EST CONDITION	NS	TA	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
				_		MIN	TYP	MAX	
					0°C		0.04		
				V _{I(PP)} = 1 V	25°C		0.03		
SR Slew rate at uni	Slew rate at unity gain	$R_L = 1 M\Omega$,	C _L = 20 pF,		70°C		0.03		V/μs
	Siew rate at unity gain	See Figure 1			0°C		0.03		v/µs
				V _{I(PP)} =2.5V	25°C	0.03			
					70°C		0.02		
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω,	See Figure 2	25°C		70		nV/√Hz
				B	0°C		6		
Вом	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	$R_{L} = 1 M\Omega,$	25°C		5		kHz
		See rigure r			70°C		4.5		
					0°C		100		
B ₁	Unity-gain bandwidth	V _I = 10 mV,	C _L = 20 pF,	See Figure 1	25°C		85		kHz
					70°C		65		
		10	()	0 00 - 5	0°C		36°		
φm	Phase margin	V _I = 10 mV, See Figure 3	f = B ₁ ,	$C_{L} = 20 \text{ pF},$	25°C		34°		
	in the second	Gee i igure e		70°C		30°			

operating characteristics, V_{DD} = 10 V

	PARAMETER	TE	EST CONDITIO	NS	TA	TLC25L4C TLC25L4AC TLC25L4BC			UNIT
						MIN	TYP	MAX	
					0°C		0.05		
				VI(PP) = 1 V	25°C		0.05		
SR	Slew rate at unity gain	$R_L = 1 M\Omega$,	C _L = 20 pF,		70°C		0.04		V/μs
SK	Siew rate at unity gain	See Figure 1			0°C		0.05		v/µs
				V _{I(PP)} =5.5V	25°C	0.04			
					70°C		0.04		
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω,	See Figure 2	25°C		70		nV/√Hz
					0°C		1.3		
вом	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	$R_{L} = 1 M\Omega,$	25°C		1		kHz
		See rigure r			70°C		0.9		
					0°C		125		
B ₁	Unity-gain bandwidth	V _I = 10 mV,	C _L = 20 pF,	See Figure 1	25°C		110		kHz
					70°C		90		
	φ _m Phase margin		()	0 00 - 5	0°C		40°		
φm		V _I = 10 mV, See Figure 3	f = B ₁ ,	C _L = 20 pF,	25°C		38°		
		coor iguio o			70°C		34°		



electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS	τ _A †	TL	.C25M40 C25M4A C25M4B	С	UNIT
						MIN	TYP	MAX	
		TLC25M4C	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		162310140	R _S = 50 Ω,	R _L = 100 kΩ	Full range			12	
VIO	Input offset voltage	TLC25M4AC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	mV
чЮ	input onset voltage	TECZOWARC	R _S = 50 Ω,	RL = 100 kΩ	Full range			6.5	IIIV
		TLC25M4BC	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.25	2	
		TEC25W4BC	R _S = 50 Ω,	RL = 100 kΩ	Full range			3	
∝VIO	Average temperature c input offset voltage	oefficient of			25°C to 70°C		1.7		μV/°C
l. a	Input offset current (see Note 4) $V_{O} = 2.5 V$, $V_{IC} = 2.5 V$						0.1	60	-
IO	input offset current (se	out offset current (see Note 4)		VIC = 2.5 V	70°C		7	300	pА
	leave bies summer (see	nut hing gurrant (and Note 4)		N 05N	25°C		0.6	60	
IВ	Input bias current (see	Note 4)	V _O = 2.5 V,	VIC = 2.5 V	70°C		40	600	pА
	Common-mode input v	oltage range			25°C	-0.2 t0 4	-0.3 to 4.2		V
VICR	(see Note 5)	0 0			Full range	-0.2 to 3.5			V
					0°C	3	3.9		
Vон	High-level output voltag	ge	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	25°C	3.2	3.9		V
					70°C	3	4		
					0°C		0	50	
VOL	Low-level output voltag	le	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
					0°C	15	200		
AVD	Large-signal differentia amplification	l voltage	$V_{O} = 0.25 V$ to 2 V,	$R_L = 100 \text{ k}\Omega$	25°C	25	170		V/mV
	amplification				70°C	15	140		
					0°C	60	91		
CMRR	Common-mode rejection	on ratio	VIC = VICRmin		25°C	65	91		dB
					70°C	60	92		
					0°C	60	92		
ksvr	Supply-voltage rejectio	n ratio	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	25°C	70	93		dB
	$(\Delta V_{DD}/\Delta V_{IO})$				70°C	60	94		
					0°C		500	1280	
IDD	Supply current (four an	nplifiers)	$V_{O} = 2.5 V$,	V _{IC} = 2.5 V,	25°C		420	1120	μA
			No load	70°C		340	880		

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS	τ _A †	TLO	TLC25M4C TLC25M4AC TLC25M4BC		
						MIN	TYP	C	
		TLC25M4C	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		1202310140	R _S = 50 Ω,	$R_L = 100 \text{ k}\Omega$	Full range			12	
VIO	Input offset voltage	TLC25M4AC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.9	5	mV
۷IO	input onset voltage	TEOZOWIARO	R _S = 50 Ω,	RL = 100 kΩ	Full range			6.5	IIIV
		TLC25M4BC	V _O = 1.4 V,	$V_{IC} = 0,$	25°C		0.26	2	
		1202011120	R _S = 50 Ω,	RL = 100 kΩ	Full range			3	
αΛΙΟ	Average temperature co offset voltage	efficient of input			25°C to 70°C		2.1		μV/°C
ha	Input offect current (see	Note 4)	V _O = 5 V,	V _{IC} = 5 V	25°C		0.1	60	n۸
ΙΟ	Input offset current (see	Note 4)	$v_{\rm O} = 5 v$,	VIC = 2 V	70°C		7	300	pА
lin.	Input bias current (see N	loto (1)	V _O = 5 V,	V _{IC} = 5 V	25°C		0.7	60	pА
IВ	input bias current (see h	NOLE 4)	$v_0 = 3 v$,	VIC = 3 V	70°C		50	600	рА
.,	Common-mode input vo	Itage range (see			25°C	-0.2 to 9	-0.3 to 9.2		V
VICR	Note 5)				Full range	-0.2 to 8.5			V
					0°C	7.8	8.7		
Vон	High-level output voltage	e	V _{ID} = 100 mV,	$R_L = 100 \text{ k}\Omega$	25°C	8	8.7		V
					70°C	7.8	8.7		
					0°C		0	50	
VOL	Low-level output voltage	•	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	25°C		0	50	mV
					70°C		0	50	
	Leave stored differential				0°C	15	320		
AVD	Large-signal differential amplification	voltage	$V_{O} = 1 V \text{ to } 6 V,$	$R_L = 100 \text{ k}\Omega$	25°C	25	275		V/mV
	ampinioation				70°C	15	230		
					0°C	60	94		
CMRR	Common-mode rejection	n ratio	$V_{IC} = V_{ICR}min$		25°C	65	94		dB
					70°C	60	94		
					0°C	60	92		
k SVR	Supply-voltage rejection	ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 5 V \text{ to } 10 V,$	V _O = 1.4 V	25°C	70	93		dB
					70°C	60	94		
					0°C		690	1600	
IDD	Supply current (four amp	olifiers)	V _O = 5 V, No load	V _{IC} = 5 V,	25°C		570	1200	μΑ
							440	1120	

[†]Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



operating characteristics, V_{DD} = 5 V

	PARAMETER	т	EST CONDITIO	NS	TA	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
				-		MIN	TYP	MAX	
					0°C		0.46		V/µs
				V _{I(PP)} = 1 V	25°C		0.43		V/µs
SR	Slew rate at unity gain	$R_L = 100 \text{ k}\Omega,$	C _L = 20 pF,		70°C		0.36		
SK	Siew rate at unity gain	See Figure 1			0°C		0.43		V/µs
				V _{I(PP)} = 2.5 V	25°C				ν/μ5
					70°C				
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω,	See Figure 2	25°C		32		nV/√Hz
				B (AA) A	0°C		60		
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	C _L = 20 pF,	R _L = 100 kΩ,	25°C		55		kHz
		See ligure l			70°C		50		
					0°C		610		
B ₁	Unity-gain bandwidth	V _I = 10 mV,	CL = 20 pF,	See Figure 1	25°C		525		kHz
					70°C		400		
		10	()	0 00 - 5	0°C		41°		
фт	Phase margin	V _I = 10 mV, See Figure 3	$f = B_1$,	C _L = 20 pF,	25°C		40°		
	g.r	Gee Liguie e		70°C		39°			

operating characteristics, V_{DD} = 10 V

	PARAMETER	т	EST CONDITIO	NS	TA	TLC25M4C TLC25M4AC TLC25M4BC			UNIT
						MIN	TYP	MAX	
					0°C		0.67		
				VI(PP) = 1 V	25°C		0.62		
SR	Slow roto of unity goin	R _L = 100 kΩ,	C _L = 20 pF,		70°C		0.51		\//uo
	Slew rate at unity gain	See Figure 1			0°C		0.61		V/μs
				V _{I(PP)} = 5.5 V	25°C	0.56			
					70°C		0.46		
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω,	See Figure 2	25°C		32		nV/√Hz
				D	0°C		40		
Вом	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	CL = 20 pF,	R _L = 100 kΩ,	25°C		35		kHz
		Occ rigure r			70°C		30		
					0°C		710		
B ₁	Unity-gain bandwidth	V _I = 10 mV,	C _L = 20 pF,	See Figure 1	25°C		635		kHz
					70°C		510		
		10	<u> </u>	0. 00 = 5	0°C		44°		
φm	Phase margin	V _I = 10 mV, See Figure 3	$f = B_1,$	C _L = 20 pF,	25°C		43°		
		Jeen Sand C			70°C		42°		



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	DADAMETED	TEST	Т	LC254Y	(Т	LC25L4	Y	TI	_C25M4	Y	UNIT
	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	$V_{O} = 1.4 V,$ $V_{IC} = 0 V,$ $R_{S} = 50 \Omega,$ See Note 6		1.1	10		1.1	10		1.1	10	mV
αVIO	Average temperature coefficient of input offset voltage			1.8			1.1			1.7		μV/°C
IIO	Input offset current (see Note 4)	$V_{O} = V_{DD}/2,$ $V_{IC} = V_{DD}/2$		0.1	60		0.1	60		0.1	60	pА
I _{IB}	Input bias current (see Note 4)	$V_{O} = V_{DD}/2,$ $V_{IC} = V_{DD}/2$		0.6	60		0.6	60		0.6	60	pА
VICR	Common-mode input voltage range (see Note 5)		-0.2 to 4	-0.3 to 4.2		-0.2 to 4	-0.3 to 4.2		-0.2 to 4	-0.3 to 4.2		V
VOH	High-level output voltage	$V_{ID} = 100 \text{ mV},$ $R_L = 100 \text{ k}\Omega$	3.2	3.8		3.2	4.1		3.2	3.9		V
V _{OL}	Low-level output voltage	$V_{ID} = -100 \text{ mV},$ $I_{OL} = 0$		0	50		0	50		0	50	mV
A _{VD}	Large-signal differential voltage amplification	V _O = 0.25 V, See Note 6	5	23		50	520		25	170		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	65	80		65	94		65	91		dB
ksvr	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V _{DD} = 5 V to 10 V, V _O = 1.4 V	65	95		70	97		70	93		dB
I _{DD}	Supply current	$V_O = V_{DD}/2,$ $V_{IC} = V_{DD}/2,$ No load		2.7	6.4		0.04	0.068		0.42	1.12	mA

electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically. 5. This range also applies to each input individually.

6. For low-bias mode, $R_L = 1 M\Omega$, for medium-bias mode, $R_L = 100 k\Omega$, and for high-bias mode, $R_L = 10 k\Omega$.

operating characteristics, $V_{DD} = 5 V$, $T_A = 25^{\circ}C$

	ARAMETER	TEST CO	NDITIONS	Т	LC254Y	,	TI	_C25L4	Y	TLC25M4Y			UNIT
	ARAMETER	TEST CC	INDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
SR	Slew rate at	CL = 20 pF,	V _{I(PP)} = 1 V		3.6			0.03			0.43		V/µs
JA	unity gain	See Note 6	V _{I(PP)} = 2.5 V		2.9			0.03			0.40		ν/μ5
Vn	Equivalent input noise voltage	f = 1 kHz,	R _S = 20 Ω		2.5			70			32		nV/√ Hz
B _{OM}	Maximum output-swing bandwidth	V _O = V _{OH} , R _L = 10 kΩ	C _L = 20 pF,		320			5			55		kHz
В ₁	Unity-gain bandwidth	V _I = 10 mV,	C _L = 20 pF		1.7			0.085			0.525		MHz
[¢] m	Phase margin	f = B ₁ , C _L = 20 pF	V _I = 10 mV,		46°			34°			40°		

NOTE 6: For low-bias mode, $R_L = 1 M\Omega$, for medium-bias mode, $R_L = 100 k\Omega$, and for high-bias mode, $R_L = 10 k\Omega$.

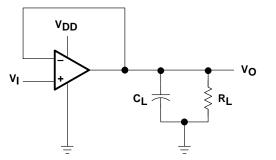
TLC254, TLC254A, TLC254B, TLC254Y, TLC25L4, TLC25L4A, TLC25L4B TLC25L4Y, TLC25M4, TLC25M4A, TLC25M4B, TLC25M4Y Incmost Quad Operational Amplifiers

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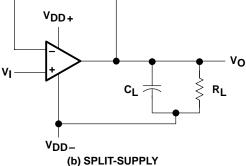
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC25_4, TLC25_4A, and TLC25_4B are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

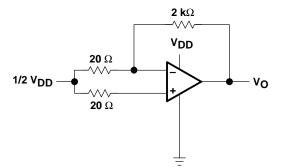


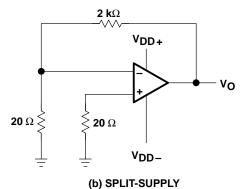
(a) SINGLE-SUPPLY





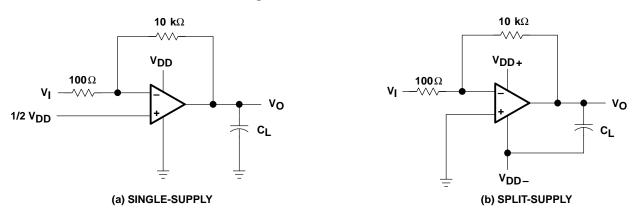


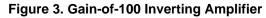




(a) SINGLE-SUPPLY









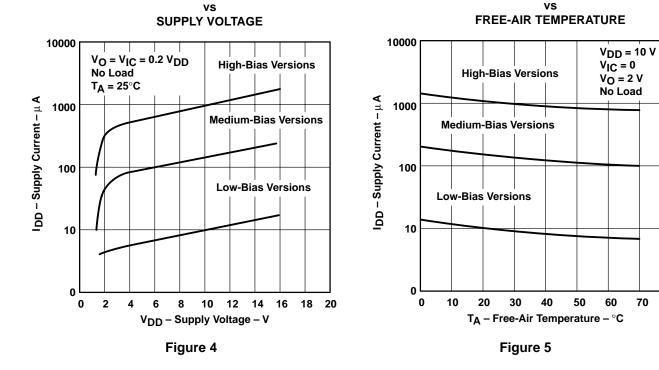
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SUPPLY CURRENT

TYPICAL CHARACTERISTICS

Table of Graphs

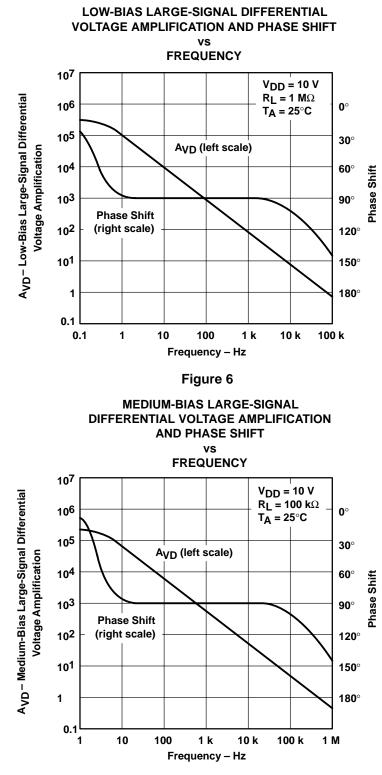
		_		FIGURE
IDD	Supply current		vs Supply voltage vs Free-air temperature	4 5
		Low bias	vs Frequency	6
AVD	Large-signal differential voltage amplification	Medium bias	vs Frequency	7
		High bias	vs Frequency	8
		Low bias	vs Frequency	6
	Phase shift	Medium bias	vs Frequency	7
		High bias	vs Frequency	8



SUPPLY CURRENT

ISTRUMENTS POST OFFICE BOX 655303 • DALLAS, TEXAS 75265 80

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TYPICAL CHARACTERISTICS

Figure 7



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TYPICAL CHARACTERISTICS

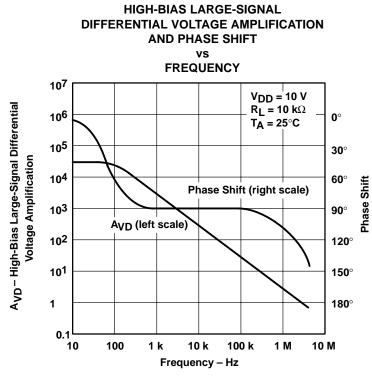


Figure 8



APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifiers supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (VOH) is virtually independent of the IDD selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, VOL is essentially equal to the potential of V_{DD}_/GND.

supply configurations

Even though the TLC25_4C series is are characterized for single-supply operation, they can be used effectively in a split-supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OI} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

Whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup as well as excessive dc leakages.





26-Aug-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TLC254ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC254AC	Samples
TLC254ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC254AC	Samples
TLC254ACN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC254ACN	Samples
TLC254ACNE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC254ACN	Samples
TLC254BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC254BC	Samples
TLC254BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC254BC	Samples
TLC254BCN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC254BCN	Samples
TLC254BCNE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC254BCN	Samples
TLC254CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254C	Samples
TLC254CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC254C	Samples
TLC254CN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	Samples
TLC254CNE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC254CN	Samples
TLC25L4ACN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC25L4ACN	Samples
TLC25L4ACNE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	TLC25L4ACN	Samples
TLC25L4BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	25L4BC	Samples
TLC25L4BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	25L4BC	Samples
TLC25L4BCN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC25L4BCN	Samples



PACKAGE OPTION ADDENDUM

26-Aug-2013

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TLC25L4BCNE4	(1) ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	⁽³⁾ N / A for Pkg Type		TLC25L4BCN	Samples
TLC25L4CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25L4C	Samples
TLC25L4CDB	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI			
TLC25L4CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC25L4C	Samples
TLC25L4CN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC25L4CN	Samples
TLC25L4CNE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC25L4CN	Samples
TLC25M4ACDR	PREVIEW	SOIC	D	14		TBD	Call TI	Call TI			
TLC25M4ACN	OBSOLETE	PDIP	Ν	14		TBD	Call TI	Call TI			
TLC25M4BCD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI			
TLC25M4BCNE4	ACTIVE	PDIP	Ν	14		TBD	Call TI	Call TI		TLC25M4BCN	Samples
TLC25M4CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC25M4C	Samples
TLC25M4CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TLC25M4C	Samples
TLC25M4CN	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC25M4CN	Samples
TLC25M4CNE4	ACTIVE	PDIP	Ν	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TLC25M4CN	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.



PACKAGE OPTION ADDENDUM

26-Aug-2013

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



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