SGS-THOMSON MICROELECTRONICS
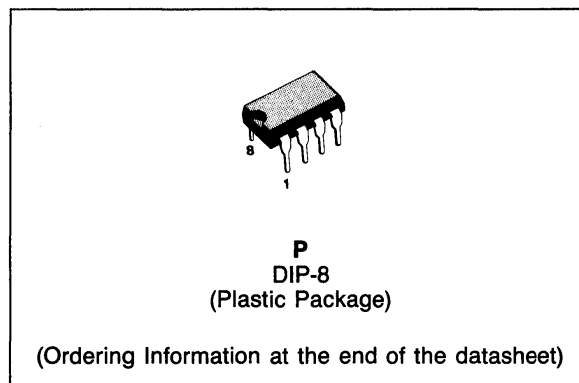
2K BIT SERIAL 2 WIRE BUS CMOS EEPROM

- 256 × 8 SERIAL EEPROM
- SINGLE + 5V ONLY OPERATION
- COMPATIBLE WITH THE INTER-INTEGRATED-CIRCUIT BUS
- FULLY TTL COMPATIBLE INPUTS AND OUTPUTS
- UNLIMITED READ ACCESSES
- ESD PROTECTION: INPUTS ARE DESIGNED TO MEET 2.0 KV PER TEST METHOD 3015, MIL-STD 883
- HIGHLY RELIABLE N-WELL CMOS TECHNOLOGY
- DESIGNED FOR 10 YEAR DATA RETENTION AFTER 10000 ERASE/WRITE CYCLE PER WORD
- 0 TO + 70°C OPERATING AMBIENT TEMPERATURE RANGE.
- − 40 TO + 85°C EXTENDED TEMPERATURE RANGE

P
DIP-8
(Plastic Package)

(Ordering Information at the end of the datasheet)

PIN CONNECTIONS

A O	1	8 (+5V) V_{DD}
A 1	2	7
A 2	3	6 SCL
V_{SS} (GND)	4	5 SDA

S - 10578

DESCRIPTION

The ST24C02 is a 2K EEPROM manufactured in SGS-THOMSON highly reliable CMOS technology. The key features of this device are + 5 volt only operation and inter—integrated circuit bus compatibility. This revolutionnary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of in the bus protocol. Up to eight ST24C02s may be capacitance).

Chip select is accomplished by means of the three address inputs A_0, A_1 and A_2. Each of these inputs must be connected externally to either + 5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input the (SDA) at the appropriate time in the bus protocol. Up to eight TS24C02s may be connected to the serial bus.
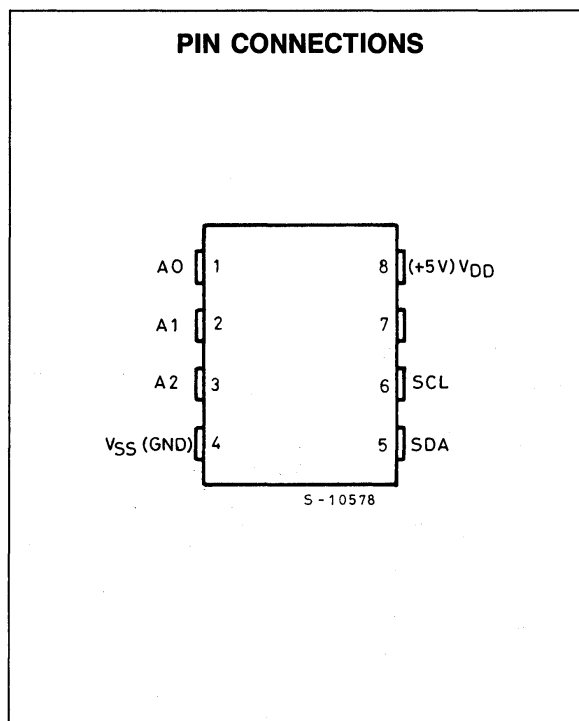
PIN NAMES

A_0-A_1-A_2	CHIP ADDRESS INPUTS
V_{SS}	GROUND
S_{DA}	SERIAL DATA/ADDRESS, INPUT/OUTPUT
S_{CL}	SERIAL CLOCK INPUT, ERASE/WRITE
V_{CC}	+ 5V POWER SUPPLY

BLOCK DIAGRAM

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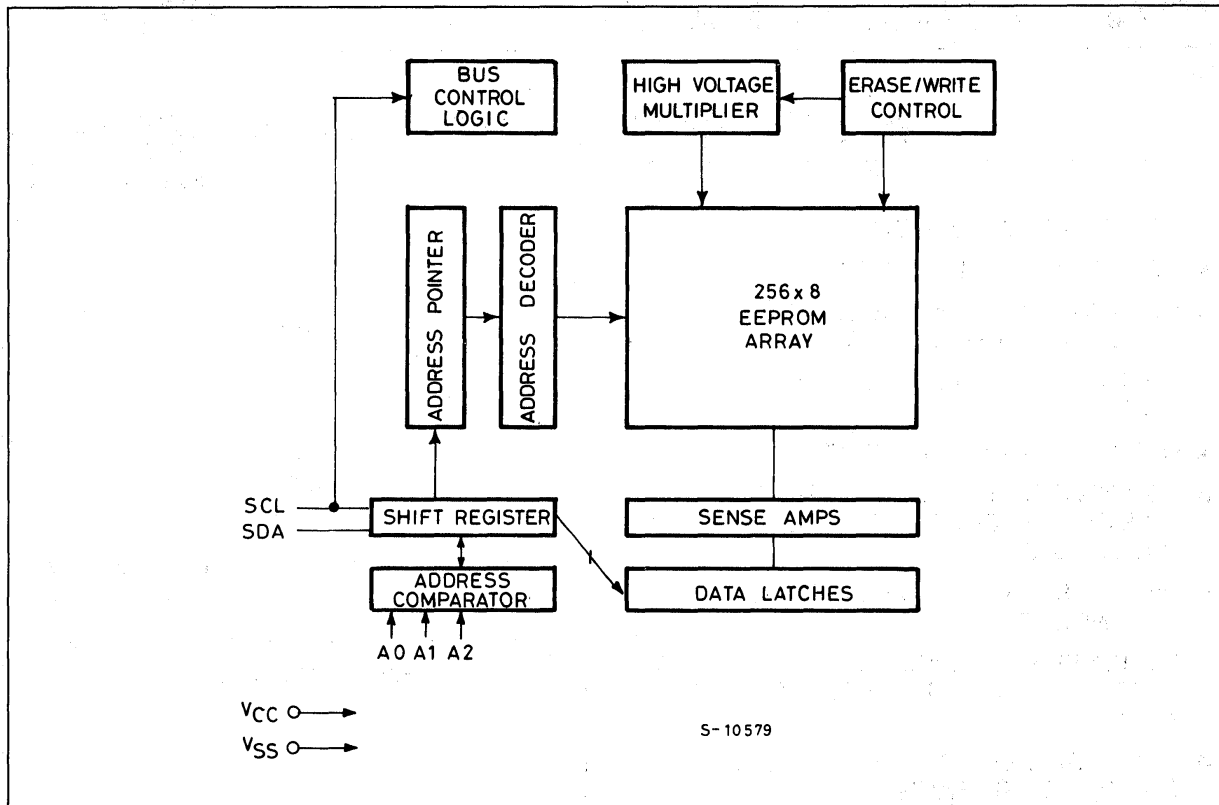
ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristic	Min	Typ	Max	Units
V_{DD}	Power supply voltage	-0.3		7	V
V_I	Voltage on any input pin	$V_{SS} - 0.8$		$V_{DD} + 0.8$	V
T_A[1]	Ambient operating temperature	0		$+70$	°C
I_{SIG}	Storage temperature (unpowered and without data retention)	-65		$+150$	°C
I_I	Current into any input pin			100	μA
I_O	Output current			3	mA (SINK)
	Soldering temperature of leads (10 seconds)			300	°C

Note: 1. $T_A = -40$°C to $+85$°C for extended temperature range

* Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other condition outside those indicated in the operational sections of this specification, is not implied.

CHARACTERISTICS OF THE 2-WIRE BUS

This bus is intended for communication between different ICs. It consists of two bidirectional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pullup resistor.

The following protocol has been defined:
- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpretated as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to eight bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted byte-wise and each receiver acknowledges with a ninth bit.

Whithin the bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The ST 24C02 works in both modes By definition a device that gives out a message is called "transmitter", the receiving device that gets the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clockpulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 1 attached shows the typical manner in which the ST24C02 is interfaced to the bus. For purposes of illustration chip address, A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight ST24C02s can be connected to the bus of a single system. The erase/write cycle time of this device T E/W is determinated internally.
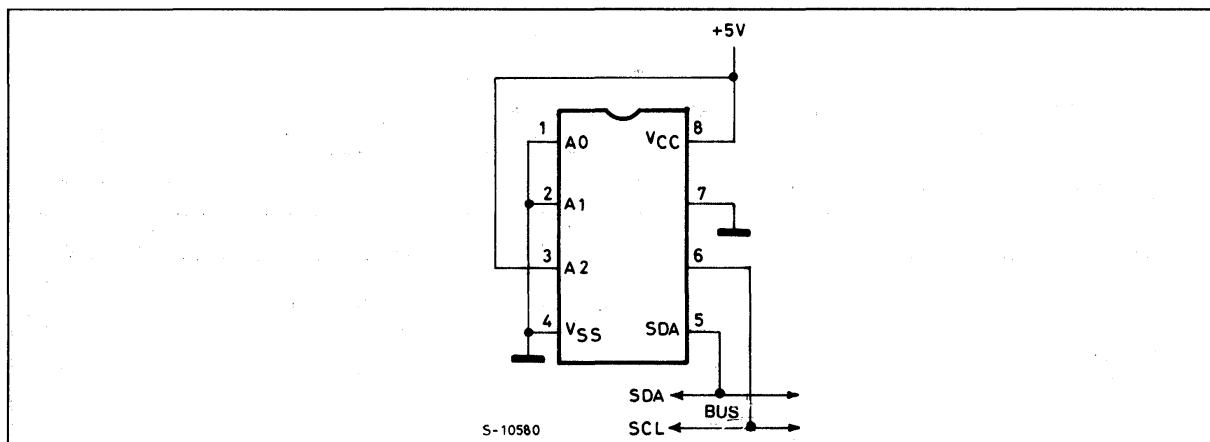
FIG. 1 - TYPICAL INTERFACE

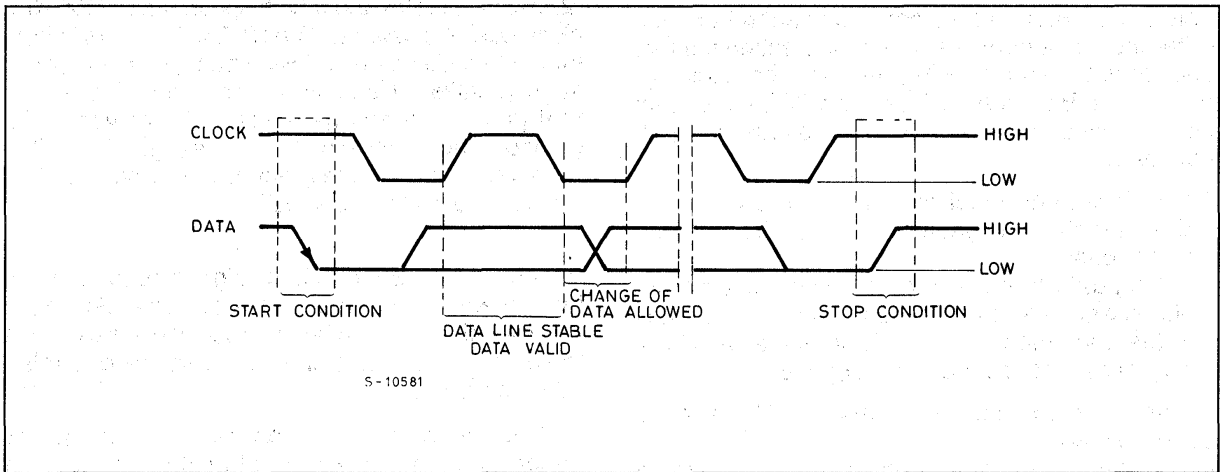## FIG. 2A - DATA TRANSFER SEQUENCE OF THE SERIAL BUS
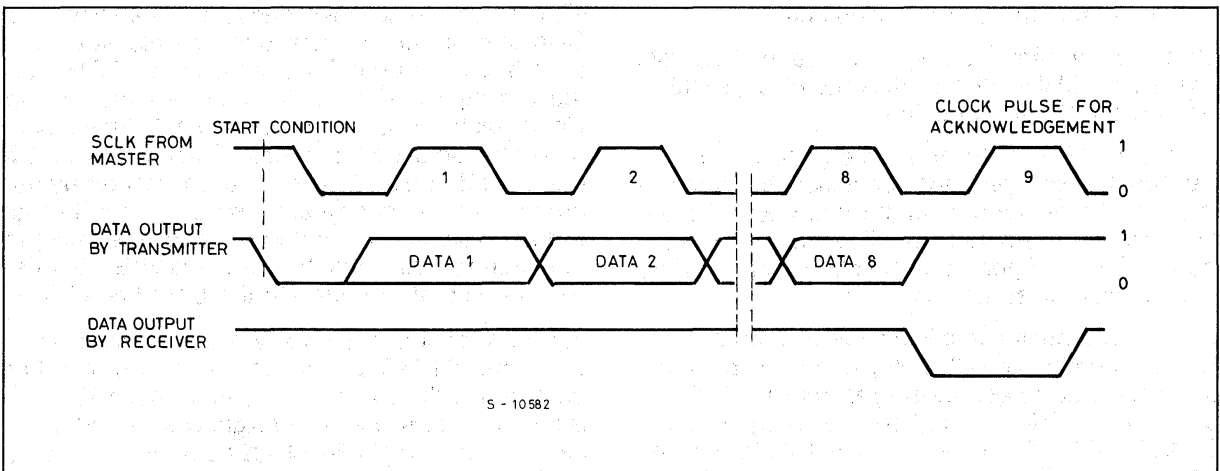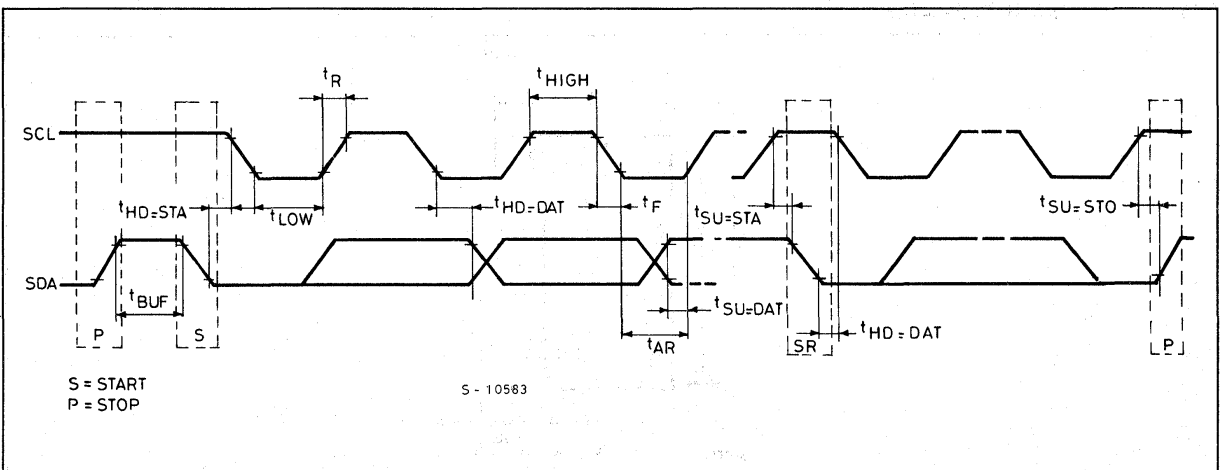

FIG. 2B - ACKNOWLEDGEMENT

FIG. 2C - BUS TIMING REQUIREMENTS

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ELECTRICAL CHARACTERISTICS

Standard conditions (unless otherwise moted)

$V_{SS} = 0V$ (GND)
$V_{CC} = +5 \pm 10\%$ volts
Ambient Operating Temperature (T_A): 0°C to +70°C (commercial) −40°C to +85°C (industrial)

Data labeled "typical" is presented for design guidance only and is not guaranteed.

SGS-THOMSON makes no warranty, expressed or implied, as to the merchantability of fitness for a particular purpose of this device or its software supplied to the customer.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DDR}	Operating supply current READ MODE				1	mA
I_{DDW}	Operating supply current WRITE/ERASE Mode				3	mA
I_{DDO}	Operating supply current STANDBY mode (CMOS input)				0.1	mA
I_{IL}	Input leakage current (A_0, A_1, A_2, SCL pins)				10	μA
I_{OH}	Output leakage current HIGH				10	μA
V_{IH}	SCL input and SDA input/output pins: High level input voltage		3.0		$V_{DD} + 0.8$	V
V_{IL}	Low level input voltage		−0.3		1.5	V
V_{OL}	Low level output voltage	$I_{OL} = 3mA$ $V_{DD} = 4.5V$			0.4	V
V_{IH}	High level input voltage	(A_0, A_1, A_2 pins)	$V_{DD} - 0.5$		$V_{DD} + 0.5$	V
V_{IL}	Low level input voltage	(A_0, A_1, A_2 pins)	−0.3		0.5	V

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
f_{SCL}	SCL clock frequency		0		100	KHz
t_{LOW}	The LOW period of the clock		4.7			μs
t_{HIGH}	The HIGH period of the clock		4.0			μs
t_R	SDA and SCL rise time				1	μs
t_F	SDA and SCL fall time				300	μs
t_{AA}	SCL low to SDA data out		0.3	1.5	3.5	μs
$t_{HD:STA}$	START condition hold time. After this period the first clock pulse is generated		4.0			μs
$t_{SU:STA}$	Setup time for start condition (only relevant for a repeated start condition)		4.7			μs
$t_{SU:DAT}$	Data set-up time		250			ns
$t_{HD:DAT}$	Data hold time		0			μs
$T_{SU:STO}$	STOP condition set-up		4.7			μs
t_{BUF}	Time the bus must be free before a new transmission can start		4.7			μs
$T_{E/W}$	Erase/Write cycle time (per word)				10	ms
$N_{E/W}$	Endurance (number of erase/write cycles)				10000	E/W cycles
t_s	Data retention time		10			Years
C_I	Input capacitance on SCL, SDA				7	pf
T_I	Noise suppresion time constant at SCL and SDA input		0.25	0.5	1.0	μs

Notes: 1. All values referred to V_{IH} and V_{IL} levels
2. Note that a transmitter must internally provide at least time to bridge the undefined region (max. 300 ns) of the edge of SCL.

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INTER INTEGRATED CIRCUIT BUS PROTOCOL

The following is a condensed description of each mode of operation.

Chip address (slave address) allocation: The three chip address inputs of each ST24C02 (A_2, A_1, A_0) must be externally connected to either + 5V (V_{CC}) or ground (V_{SS}) thereby assigning to each ST24C02 a unique three-bit chip address. Up to eight ST24C02s may be connected to the serial bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hard-wired logic levels of the selected ST24C02. The correct bus protocol is shown in figure 3.

Erase/Write Mode:
In this mode the master transmitter transmits to the ST24C02 slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address, a logic 0 (R/W = 0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the data register. Another 7 data bytes may be strobed in following this in the data register. In the erase/write mode no more than 8 successive data bytes may be strobed into the ST24C02 (Fig. 4a). The ST24C02 slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte.

After the STOP condition the Erase/Write cycle starts. Its duration is at most 10 ms per data byte. After the receipt of each word, the three low order address bits are internally incremented by one. The high order five bits of the word address remain constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the by

te write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.
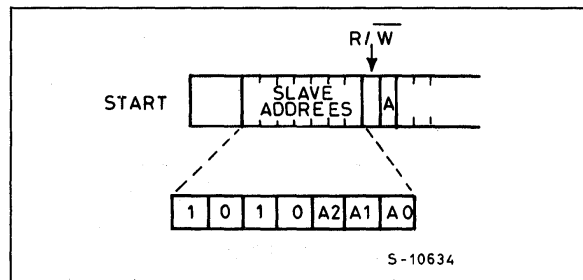
Read mode:

In this mode the master reads the ST24C02 slave after setting the slave address. See figure 5. Following the write mode control bit (R/W = 0) and the acknowledge bit, the word address An is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/W = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The ST24C02 slave transmitter will now place the data byte at address An + 1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An + 2.

This cycle of reading consecutive addresses will continue until the master receiver send a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the ST24C02 slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

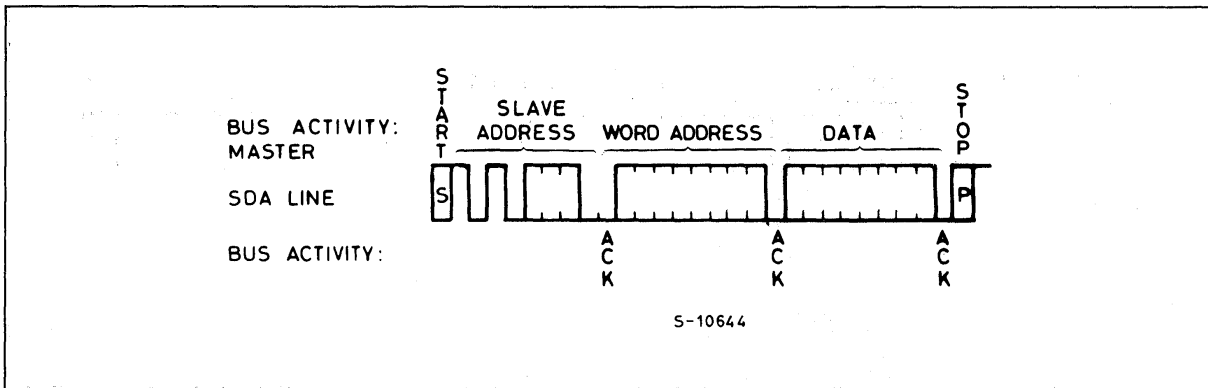### FIG. 3 - SLAVE ADDRESS ALLOCATION

S-10634

FIG. 4 - BYTE WRITE

S-10644

FIG. 4A - PAGE WRITE

S-10633

FIG. 5 - READ MODE

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FIG. 6 - ALTERNATE READ MODE

S-10642

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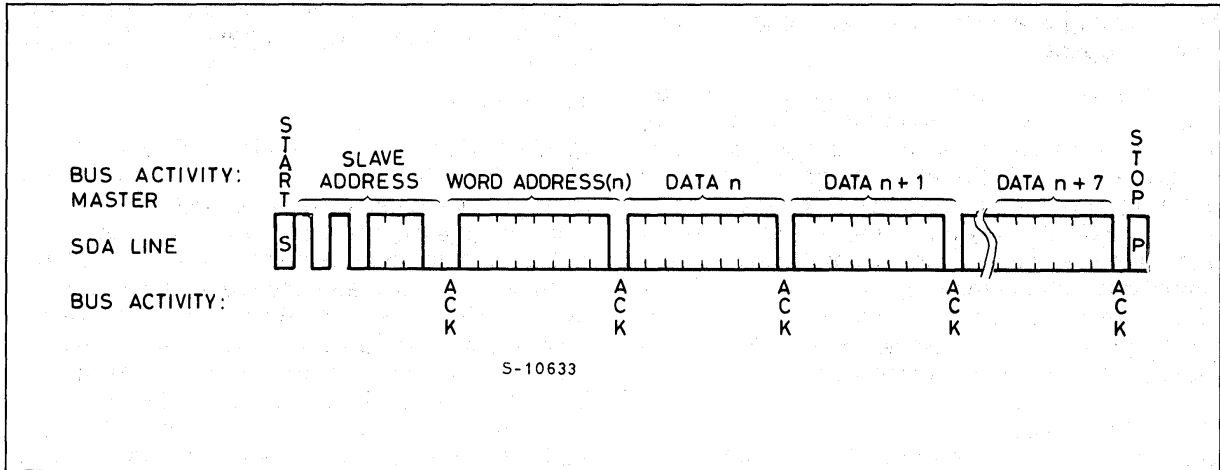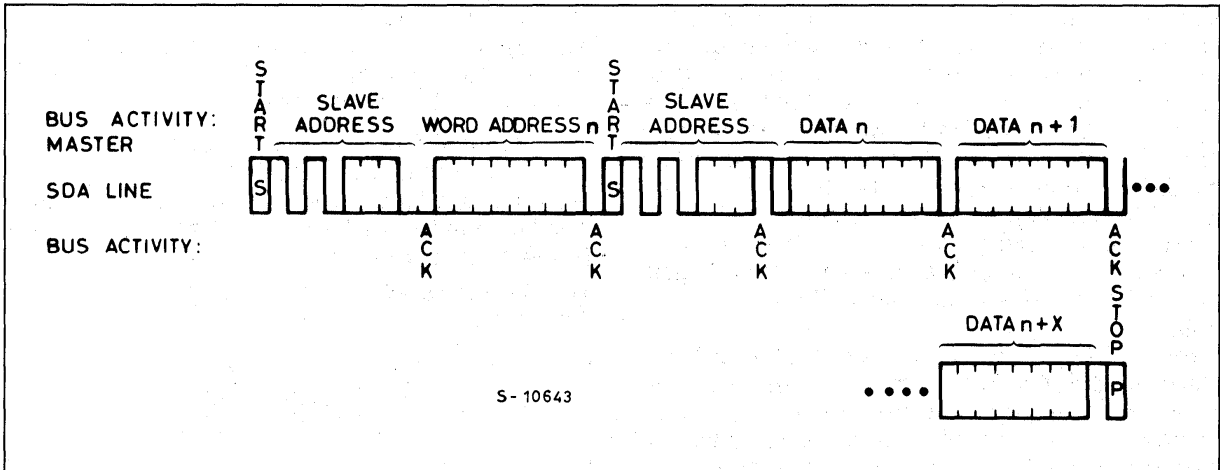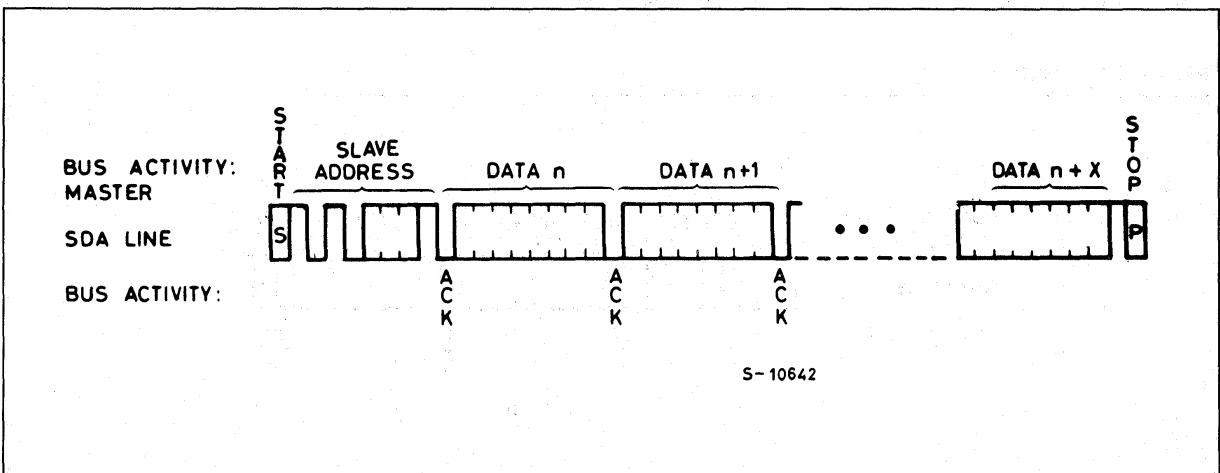
ORDERING INFORMATION

Part Number	Max Frequency	Supply Voltage	Temp. Range	Package
ST24C02CP	100 KHz	5V ± 10%	0 to + 70°C	DIP-8
ST24C02VP	100 KHz	5V ± 10%	− 40 to + 85°C	DIP-8

PACKAGE MECHANICAL DATA
8-PIN PLASTIC DIP

Dim.	mm Min	mm Typ	mm Max	inches Min	inches Typ	inches Max
A						
a1	0.70			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.50			0.02	
b1	0.38		0.50	0.015		0.020
C						
D			9.80			0.386
D1						
E		8.90			0.350	
e		2.54			0.100	
e3		7.62			0.300	
e4						
F			7.10			0.280
I			4.80			0.189
L		3.30			0.130	
N						
Z	0.44		1.60	0.017		0.063

P001-F/6