

# ECG<sup>®</sup> Semiconductors

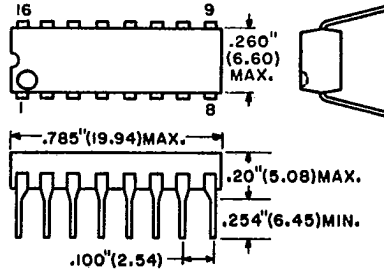
## ECG1272 Phase Locked Loop Frequency Synthesizer

T-45-19-13

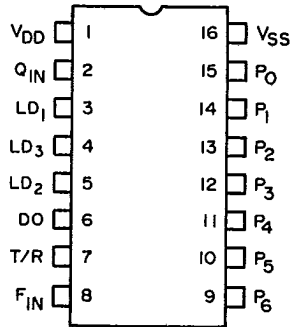
**Features**

- Single crystal application
- Inhibit circuits for illegal frequencies
- Safeguard output for out-of-lock state
- 40-channel binary acceptable program input

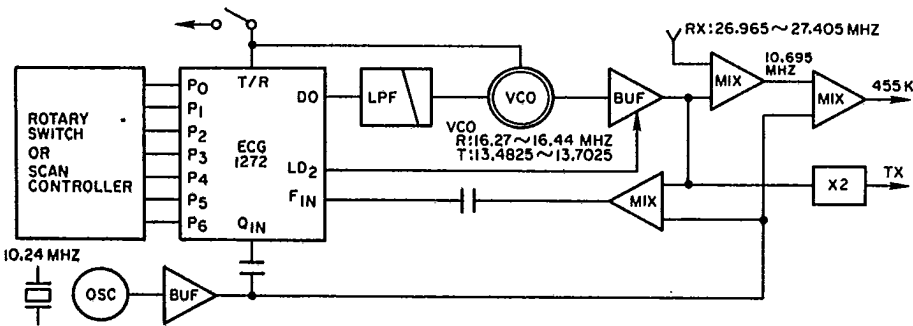
ECG1272 is a CMOS LSI designed for phase locked loop frequency synthesizer circuits and is suited for crystal synthesizer applications.



**Pin Connections**



**Typical Application**



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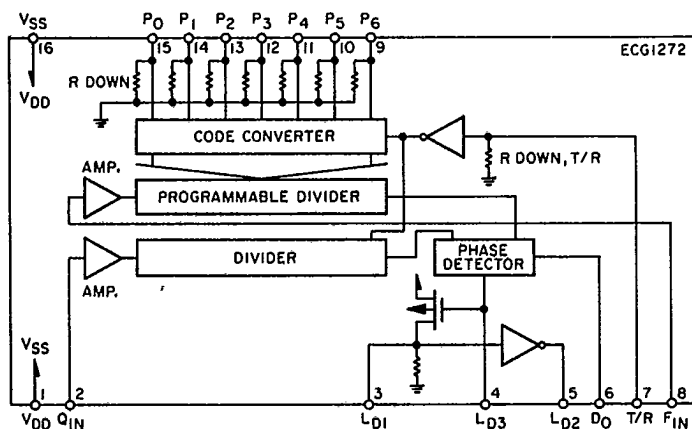
**Absolute Maximum Ratings**

Characteristic	Symbol	Rating	Unit
Voltage Range	V <sub>DD</sub> -V <sub>SS</sub>	-0.3 to +9.0	V
Input Voltage	V <sub>IN</sub>	V <sub>SS</sub> < V <sub>IN</sub> < V <sub>DD</sub>	V
Power Dissipation	P <sub>D</sub>	250	mW
Operating Temperature	T <sub>opg</sub>	-30 to +70	°C
Storage Temperature	T <sub>stg</sub>	-40 to +125	°C
Short Circuit Time	T <sub>sold</sub>	5	sec

**Electrical Characteristics (T<sub>A</sub> = 30 to +70°C, f<sub>osc</sub> = 10.24 MHz, V<sub>SS</sub> = GND, V<sub>DD</sub> = 6.0 to 7.0 V)**

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Circuit Current	I <sub>DD</sub>	--	--	10	15	mA
Saturation Current	I <sub>sat</sub>	D <sub>O</sub> = GND or V <sub>DD</sub>	1	--	--	mA
Damping Resistance	R <sub>D</sub>	--	10	--	120	k
High Level-DC Input Voltage	V <sub>IH</sub>	--	V <sub>DD</sub> - 0.4	--	V <sub>DD</sub>	V
Low Level-DC Input Voltage	V <sub>IL</sub>	--	V <sub>SS</sub>	--	V <sub>SS</sub> + 0.4	V
High Level Output Voltage	V <sub>OH</sub>	I <sub>source</sub> = -0.1 mA	V <sub>DD</sub> - 0.5	--	V <sub>DD</sub>	V
Low Level Output Voltage	V <sub>OL</sub>	I <sub>sink</sub> = +0.1 mA	V <sub>SS</sub>	--	V <sub>SS</sub> + 0.5	V
AC Input Voltage	V <sub>IN</sub>	Peak to Peak	1.5	--	$\frac{V_{DD}}{2}$	V
Bias Voltage	V <sub>bias</sub>	V <sub>DD</sub> = 6.5 V	2	3	4	V

**Block Diagram**



Mode	T/R	Divide Ratio	
		Divider	Programmable Divider
Transmission	High	4096	N
Reception	Low (Open)	2048	N-91

ECG1272

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CB CH No.	Transmit		Receive	
	(MHz)	F IN (MHz)	(MHz)	F IN (MHz)
1	26.965	3.2425	16.27	6.03
2	26.975	3.2475	16.28	6.04
3	26.985	3.2525	16.29	6.05
4	27.005	3.2625	16.31	6.07
5	27.015	3.2675	16.32	6.08
6	27.025	3.2725	16.33	6.09
7	27.035	3.2775	16.34	6.10
8	27.055	3.2875	16.36	6.12
9	27.065	3.2925	16.37	6.13
10	27.075	3.2975	16.38	6.14
11	27.085	3.3025	16.39	6.15
12	27.105	3.3125	16.41	6.17
13	27.115	3.3175	16.42	6.18
14	27.125	3.3225	16.43	6.19
15	27.135	3.3275	16.44	6.20
16	27.155	3.3375	16.46	6.22
17	27.165	3.3425	16.47	6.23
18	27.175	3.3475	16.48	6.24
19	27.185	3.3525	16.49	6.25
20	27.205	3.3625	16.51	6.27
21	27.215	3.3675	16.52	6.28
22	27.225	3.3725	16.53	6.29
23	27.255	3.3875	16.56	6.32
24	27.235	3.3775	16.54	6.30
25	27.245	3.3825	16.55	6.31
26	27.265	3.3925	16.57	6.33
27	27.275	3.3975	16.58	6.34
28	27.285	3.4025	16.59	6.35
29	27.295	3.4075	16.60	6.36
30	27.305	3.4125	16.61	6.37
31	27.315	3.4175	16.62	6.38
32	27.325	3.4225	16.63	6.39
33	27.335	3.4275	16.64	6.40
34	27.345	3.4325	16.65	6.41
35	27.355	3.4375	16.66	6.42
36	27.365	3.4425	16.67	6.43
37	27.375	3.4475	16.68	6.44
38	27.385	3.4525	16.69	6.45
39	27.395	3.4575	16.70	6.46
40	27.405	3.4625	16.71	6.47

CH No.	Div. Ratio	P6	P5	P4	P3	P2	P1	P0
1	330	1	0	0	1	0	1	0
2	329	1	0	0	1	0	0	1
3	328	1	0	0	1	0	0	0
4	326	1	0	0	0	1	1	0
5	325	1	0	0	0	1	0	1
6	324	1	0	0	0	1	0	0
7	323	1	0	0	0	0	1	1
8	321	1	0	0	0	0	0	1
9	320	1	0	0	0	0	0	0
10	319	0	1	1	1	1	1	1
11	318	0	1	1	1	1	1	0
12	316	0	1	1	1	1	0	0
13	315	0	1	1	1	0	1	1
14	314	0	1	1	1	0	1	0
15	313	0	1	1	1	0	0	1
16	311	0	1	1	0	1	1	1
17	310	0	1	1	0	1	1	0
18	309	0	1	1	0	1	0	1
19	308	0	1	1	0	1	0	0
20	306	0	1	1	0	0	1	0
21	305	0	1	1	0	0	0	1
22	304	0	1	1	0	0	0	0
23	301	0	1	0	1	1	0	1
24	303	0	1	0	1	1	1	1
25	302	0	1	0	1	1	1	0
26	300	0	1	0	1	1	0	0
27	299	0	1	0	1	0	1	1
28	298	0	1	0	1	0	1	0
29	297	0	1	0	1	0	0	1
30	296	0	1	0	1	0	0	0
31	295	0	1	0	0	1	1	1
32	294	0	1	0	0	1	1	0
33	293	0	1	0	0	1	0	1
34	292	0	1	0	0	1	0	0
35	291	0	1	0	0	0	1	1
36	290	0	1	0	0	0	1	0
37	289	0	1	0	0	0	0	1
38	288	0	1	0	0	0	0	0
39	287	0	0	1	1	1	1	1
40	286	0	0	1	1	1	1	0