T-45-19-13

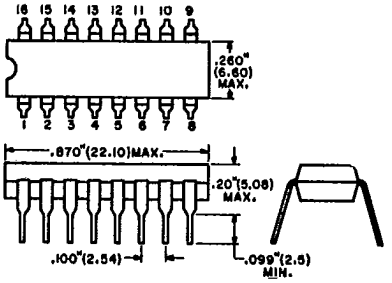
ECG® Semiconductors

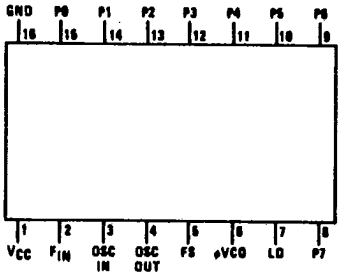
ECG1255

PLL Frequency Synthesizer

Features

- Single power supply
- Low power CMOS technology
- Binary input channel select code
- 5 kHz or 10 kHz output from oscillator divide
- On-chip oscillator
- Pull-down resistors on programmable divider inputs
- Low voltage operation—5 V





The ECG1255 device contains phase locked loop circuits useful for frequency synthesizer applications in CB transceivers. The device operates off a single power supply and contains an oscillator, a 2^{10} or 2^{11} divider chain, a binary input programmable divider, and phase detector circuitry. The device may be used in double I.F. or single I.F. systems. A 10.24 MHz or 5.12 MHz quartz crystal is used to determine the reference frequency. The inputs to the programmable divider are standard binary signals. Selection of a channel is accomplished by mechanical switches or by external electronic programming of the programmable divider.

The øVCO output provides a high level voltage (sources current) when the VCO frequency is lower than the lock frequency, and øVCO provides a low level voltage (sinks current) when the VCO frequency is higher than the lock frequency. The øVCO output goes to a high impedance condition under lock conditions, and the lock detector output LD goes to a high state under lock conditions.

Pin Description

P0-P8	Programmable divider inputs
F_{IN}	Frequency input from VCO (mixed down)
OSC IN	Oscillator amplifier input terminal
OSC OUT	Oscillator amplifier output terminal
LD	Lock detector
øVCO	Output of phase detector for control of the VCO
FS	Frequency division select to kHz or 5 kHz — "1" is 10 kHz, "0" is 5 kHz
5.12 MHz OUT	OSC Frequency divided by 2 output

Absolute Maximum Ratings

Characteristic	Symbol	Rating	Unit
Supply Voltage	V_{cc}	7	V
Operating Temperature	T_{opg}	−30 to +75	°C
Storage Temperature	T_{stg}	−40 to +125	°C

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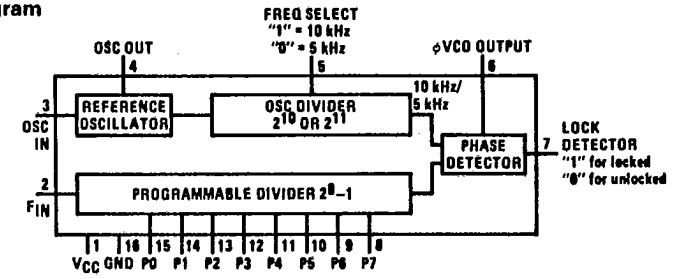
Truth Table

Truth table for binary inputs to programmable divider.

$F_{OUT} = F_{IN}/N$
1 = High voltage level, V_{OH}
0 = Low voltage level, V_{OL}
X = Don't care

N	P8	P7	P6	P5	P4	P3	P2	P1	P0
1	0	0	0	0	0	0	0	0	X
2	0	0	0	0	0	0	0	1	0
511	1	1	1	1	1	1	1	1	1

Block Diagram



Electrical Characteristics (T_A = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	Freq @ Osc In = 10 MHz, @ F_{IN} = 2.5 MHz, All Other I/O Pins Open, V_{CC} = 5 V		3	10	mA
Logical "1" Input Voltage P0-P8, FS, F_{IN}	$V_{IN(1)}$		V_{CC}- 0.4			V
Logical "0" Input Voltage P0-P8, FS, F_{IN}	$V_{IN(0)}$				0.4	V
Logical "1" Output Voltage 5.12 MHz Out, LD øVCO Osc Out		I_O = 0.5 mA I_O = 0.4 mA I_O = 0.25 mA	V_{CC}- 0.5			V
Logical "0" Output Voltage øVCO, 5.12 MHz Out,LD Osc Out		I_O = 0.5 mA I_O = 0.25 mA			0.5	V
Logical "1" Input Current FS (Pull-Up) P0-P8 (Pull-Down)		V_{CC} = 5 V	5	20	1.0 50	µA µA
Logical "0" Input Current P0-P8 (Pull-Down) FS (Pull-Up)		V_{CC} = 5 V	−10	−35	1.0 −100	µA µA
Toggle Frequency @ F_{IN}			3			MHz
Oscillator Frequency @ Osc In			10.24			MHz
Three State Leakage @ øVCO					1.0	µA

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Typical Applications

Introduction to Frequency Synthesis

The components of a frequency synthesizer are shown in Figure 1. The voltage controlled oscillator produces the desired output frequencies spaced f_V Hz apart acording to the relation:

$$f_V = f_r N$$

The reference frequency, fr, must be equal to or less than the (channel) spacing between the frequencies being synthesized.

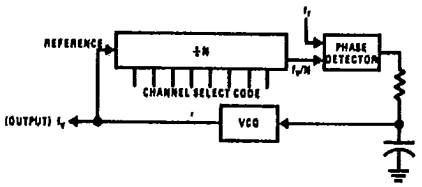

Figure 1. Basic Frequency Synthesizer

Although simple in concept, the circuit of Figure 1 has certain difficulties. In CB, we are synthesizing the following frequencies:

Ch 1	26.965
Ch 2	26.975
.	.
.	.
.	.
Ch 23	27.225

Although the channel spacing is 10 kHz, a reference frequency of 5 kHz would be necessary due to the odd 5 kHz in the assigned channel. This in itself poses no problem; however, present technology limits the counting speed of programmable dividers to something less than 5 MHz, ruling out the approach shown in Figure 1.

Two solutions to this problem are shown in Figure 2.

Frequency prescaling shown in Figure 2 (a) reduces the VCO frequency by M (a fixed number) to a frequency that can be divided by the programmable counter. The reference frequency f_r must also be reduced by M. In the case of CB, if M = 10, f_V = 26.965 MHz, the input to the programmable divider will be 2.6965 MHz, and the 5 kHz reference frequency will be reduced to 500 Hz. This poses problems in speed of response of the phase locked loop.

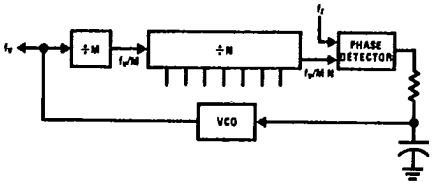

Figure 2 (a). Frequency Prescaling

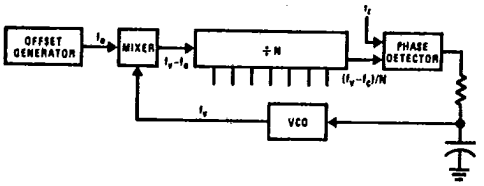

Figure 2 (b). Frequency Offset

The second technique mixes the output frequency of the VCO with a stable fixed frequency to obtain a related reference frequency.

$$f_V = Nf_r + f_o$$

This technique has the advantage of allowing a 10 kHz reference frequency in the loop instead of 5 kHz.

Further complexity arises when one considers that the synthesizer must also generate a local oscillator signal as well as a transmitter input signal for the radio (Figure 3). A system which provides these frequencies, as well as the proper offset to allow the programmable divider to operate within its limits is shown in the typical applications diagrams (Figure 4). The only departure from the ideal situation shown in Figure 3 is that the first IF frequency of 10.7 MHz must be changed to 10.695 MHz (a change of 5 kHz).

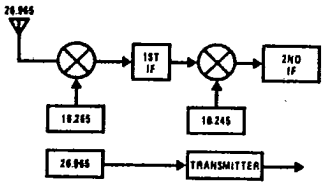

Figure 3. Signals Needed to Transmit and Receiver Ch 1

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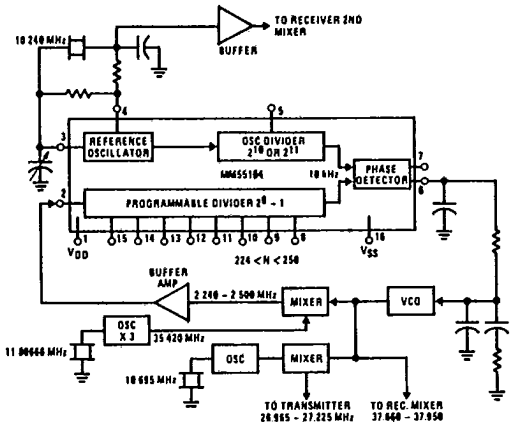

Figure 4. 3-Crystal Application

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