

ECG799, ECG802, ECG803
FOUR CHANNEL SQ LOGIC
DECODER SYSTEM

SQ LOGIC DECODER SYSTEM

... a matrix system designed to decode SQ encoded program material into four separate channels. This system conforms to specifications for decoding quadraphonic records produced by the largest record companies in the world.

ECG799 - DECODER

... consists of two high input impedance preamplifiers which are fed with left total, L_T , and right total, R_T , signals. The preamplifiers each feed two all-phase networks which generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left front, left back, right front, and right back signals (L_F' , L_B' , R_F' , R_B').

ECG802 - VOLTAGE CONTROLLED ATTENUATOR

... a gain control and balance adjustment unit for use with any quadraphonic system. It has four channels whose gain can be varied by an external dc voltage. In addition, the relative gain between channels can be set by 3 external dc voltages. Thus with four variable resistors the master volume L_F/R_F , L_B/R_B and F/B balance may be controlled.

ECG803 - LOGIC CIRCUIT

... provides the basic logic function to enhance the front to back separation in the SQ four channel decoding system. This device is designed to interface with the ECG799 decoder and ECG802. The ECG803 provides dc logic enhancement control signals which extends the performance of the basic SQ system to the levels desired for top-of-the-line systems.

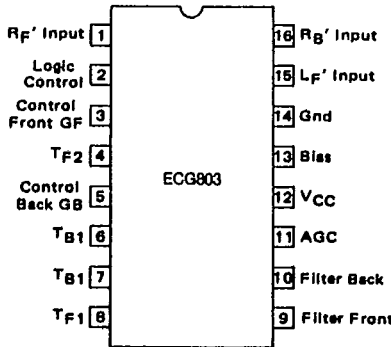
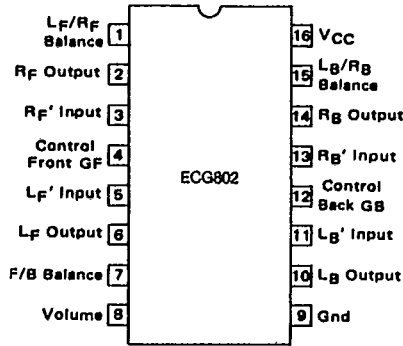
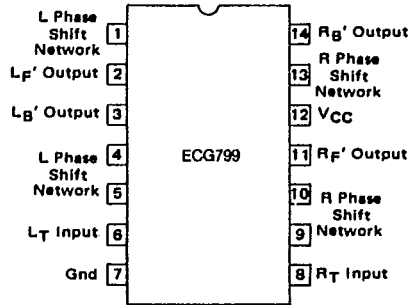
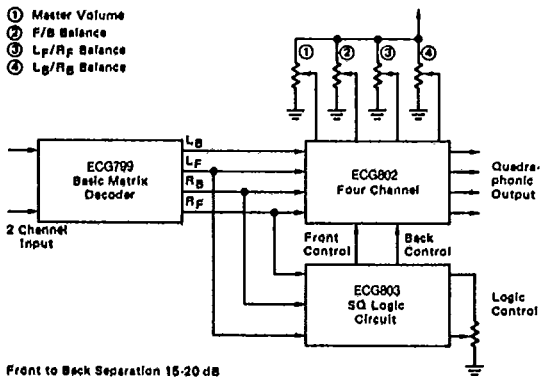


FIGURE 1 - SQ LOGIC DECODER SYSTEM



Front to Back Separation 15-20 dB

ECG799 • SQ DECODER UNIT

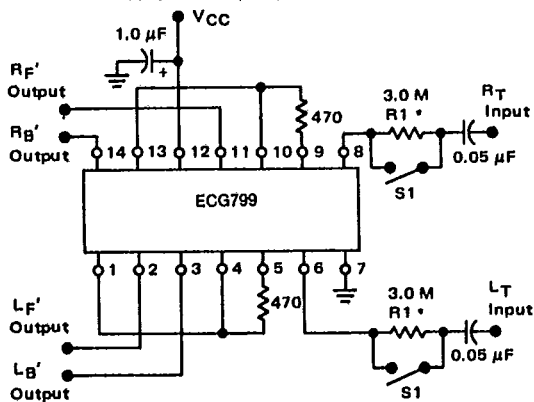
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	25	Vdc
Power Dissipation @ T _A = 25°C	750	mW
Derate above +25°C	6.7	mW/°C
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, V_{in} = 0.5 V(RMS) @ 1 kHz, T_A = +25°C unless otherwise noted.)

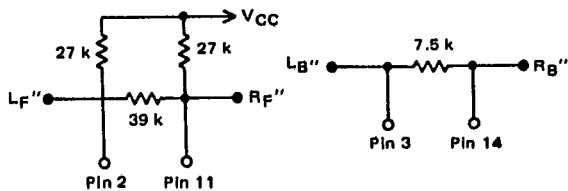
Characteristic	Min	Typ	Max	Unit
Supply Current Drain	11	16	21	mA
Input Impedance	1.8	3.0	—	MΩ
Output Impedance	—	5.0	—	kΩ
Channel Balance (L _F /R _F)	-1.0	0	+1.0	dB
Voltage Gain L _F /L _T or R _F /R _T	-1.0	0	+1.0	dB
Relative Voltage Gain L _B /L _F , R _B /L _F , L _B /R _F , R _B /R _F L _F ' measurements made with L _T input, R _F ' measurements made with R _T input.	-2.0	-3.0	-4.0	dB
Maximum Input Voltage for 1%THD at Output R _T or L _T	2.0	—	—	V(RMS)
Total Harmonic Distortion R _T or L _T	—	0.1	—	%
Signal to Noise Ratio (Short-Circuit Input V _O = 0.5 V(RMS) with Output Noise Referenced to Output Voltage, V _O) (BW = 20 Hz to 20 kHz)	—	80	—	dB

FIGURE 2 — ECG799 TEST CIRCUIT



* R1 is used for input impedance measurement.
S1 is normally closed.

FIGURE 3 — EIA STANDARD BLEND

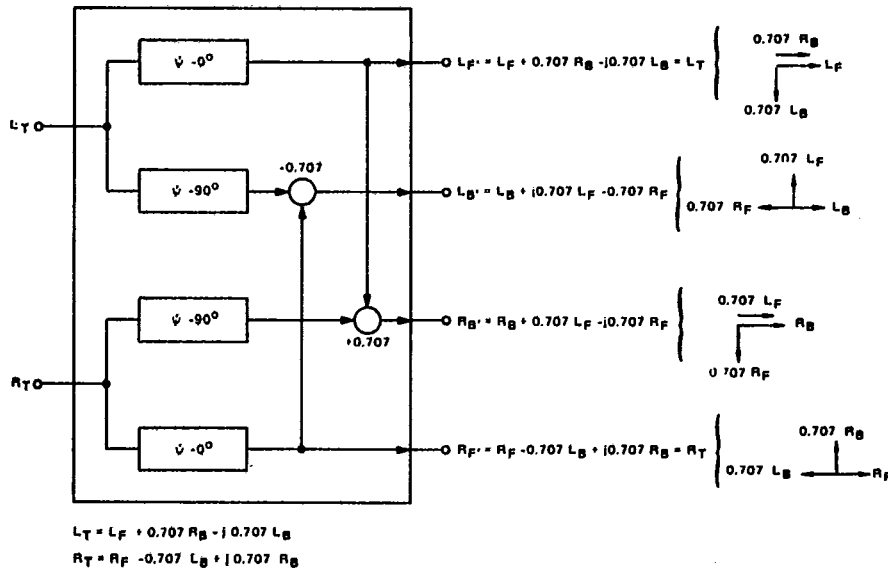


Note: In applications where tone arm pick-up is connected directly to the ECG799 inputs, a 300 k resistor should be inserted in series with R_T (Pin 8), and L_T (Pin 6) inputs.

ECG799 • SQ DECODER UNIT

APPLICATIONS INFORMATION

FIGURE 4 - DECODING PROCESS DIAGRAM



L_T and R_T are composite signals from SQ encoded records or SQ broadcast.

The decoding process is shown schematically in Figure 4. The ECG799 circuits that perform this function consists of two preamplifiers which are fed with left total, L_T, and right total, R_T, signals. The preamplifiers each feed two all-pass* networks that are used to generate two L_T signals in quadrature and two R_T signals in quadrature. The four signals are matrixed to yield left-front, left-back, right-front, and right-back signals (L_F', L_B', R_F', R_B').

The all-pass networks are of the Wein bridge form with the resistive arms realized in the integrated circuit and the RC arms formed by external components. The values shown in Figure 1 are for a 100-Hz to 10-kHz bandwidth and a phase ripple of ±8.5° on a 90° phase difference.

It is generally desirable to enhance center-front to center-back separation. This is accomplished by connecting a resistor between pins 2 and 11 (front outputs) and a resistor between pins 3 and 14 (back outputs). For a 10% front channel blending† and a 40% back channel blending†, 47 kilohms between pins 2 and 11 and

7.5 kilohms between pins 3 and 14 is required and results in the following equations:

$$\begin{aligned}
 R_F'' &= 0.912 L_T + 0.088 R_T \\
 L_F'' &= 0.912 R_T + 0.088 L_T \\
 R_B'' &= \frac{\sqrt{2}}{2} \{0.714 (J R_T - L_T) + 0.286 (R_T - J L_T)\} \\
 L_B'' &= \frac{\sqrt{2}}{2} \{0.714 (J L_T - R_T) + 0.286 (L_T - J R_T)\}
 \end{aligned}$$

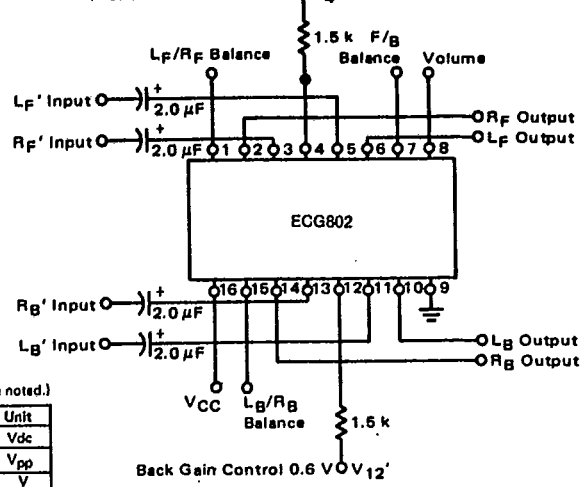
To meet the EIA matrix standards with 10/40 blend use the circuit of Figure 5, which results in the following equations:

$$\begin{aligned}
 R_F'' &= 0.772 (0.995 R_T + 0.0972 L_T) \\
 L_F'' &= 0.772 (0.995 L_T + 0.0972 R_T) \\
 R_B'' &= \frac{\sqrt{2}}{2} (0.769) [0.928 (J R_T - L_T) + 0.372 (R_T - J L_T)] \\
 L_B'' &= \frac{\sqrt{2}}{2} (0.769) [0.928 (J L_T - R_T) + 0.372 (L_T - J R_T)]
 \end{aligned}$$

*An all-pass network produces phase shift without amplitude variations.

ECG802 • GAIN CONTROL AND BALANCE ADJUSTMENT UNIT

FIGURE 5 - ECG802 TEST CIRCUIT
Front Gain Control 0.6 V @ V₄'



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	28	Vdc
Input Voltage Swing	±6.0	V _{pp}
Volume Control Range	-0.3 to +8.0	V
Balance Control Voltage	-4.0 to +10	V
Output Current Sinking (dc)	0	mA
Output Current Sourcing (dc)	1.0	mA
Power Dissipation @ T _A = +25°C	750	mW
Derate above +25°C	6.7	mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 V, V₄' = V₁₂' = 0.60 Vdc, T_A = +25°C, V_{IN} = 1.0 V(rms) @ 1.0 kHz, balance control pins open, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Maximum Gain (V _g = 6 V)	-1.0	1.0	+3.0	dB
Minimum Gain (V _g = 0 V)	-60	-	-	dB
Gain Spread @ Gain = Max	-	1.0	3.0	dB
@ Gain = -20 dB	-	-	3.0	dB
@ Gain = -40 dB	-	-	3.0	dB
Signal Handling (THD < 1%)	1.3	-	-	V _{rms}
Signal Handling (V ₄ ' = V ₁₂ ' = 0.42 Vdc balance controls set for max gain in channel under test THD < 1%)	0.4	-	-	V _{rms}
Total Harmonic Distortion (V _{IN} = 0.4 V _{rms} , max gain)	-	0.2	-	%
Signal/Noise Ratio (20 Hz - 15 kHz Bandwidth) Note 1, V _{IN} = 0.4 V _{rms} (ref)	-	80	-	dB
Channel Separation Note 2	-	60	-	dB
Balance Control Range - 20 dB gain	-	20	-	dB
V _g = 6.0 V (≈ Max Gain)	-	20	-	dB
V _g = 3.0 V (≈ 6.0 dB Gain)	18	26	-	dB
V _g = 1.0 V (≈ 20 dB Gain)	-	32	-	dB
Gain Enhancement (V ₄ ' = V ₁₂ ' = 0.42 Vdc compared to V ₄ ' = V _g ' = 0.60 Vdc)	2.0	-	4.0	dB
Gain Reduction (V ₄ ' = V ₁₂ ' = 1.86 Vdc compared to V ₄ ' = V ₁₂ ' = 0.60 Vdc)	7.0	-	11	dB
Gain Reduction (V ₄ ' = V ₁₂ ' = 3.12 Vdc compared to V ₄ ' = V ₁₂ ' = 0.60 Vdc, V _{CC} = 26 Vdc)	-	14	-	dB
Supply Current (max gain) (V _{IN} = 0 V)	-	19	26	mA
(min gain) (V _{IN} > 0 V)	-	9.0	15	mA
Input Impedance	-	13	-	kΩ
Output Impedance	-	2.0	-	kΩ
Control Current I ₄ or I ₁₂	-	-20	-	µA
Balance Control Reference Voltage (relative to V _{CC})	-	15	-	%
Lp/Rf & Lb/Rf Controls (V ₁₄ /V _{CC} & V _{15q} /V _{CC})	-	13	-	%
F/B Control (V _{7q} /V _{CC})	-	-	-	%
Intermodulation Distortion (f ₁ = 7 kHz, f ₂ = 60 Hz)	-	0.6	-	%

Note 1: All inputs ac shorted
Note 2: Input to 3-Channels driven, 4th Channel open.

ECG802 • TYPICAL CHARACTERISTICS

FIGURE 6 - ATTENUATION versus CONTROL VOLTAGE

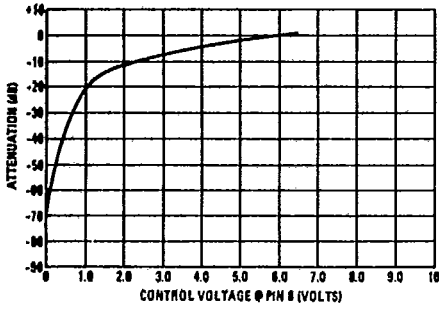
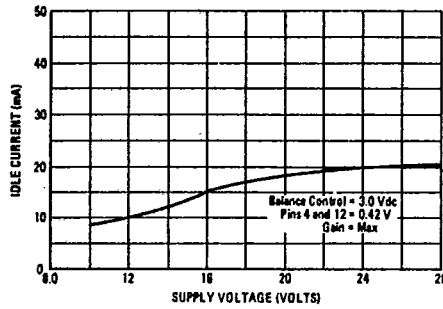


FIGURE 7 - IDLE CURRENT versus SUPPLY VOLTAGE



DISTORTION CHARACTERISTICS

FIGURE 8 - TOTAL HARMONIC DISTORTION versus ATTENUATION

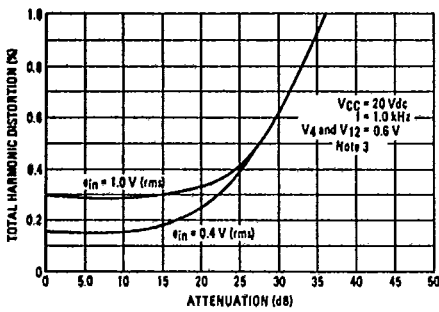


FIGURE 9 - INTERMODULATION DISTORTION versus INPUT VOLTAGE

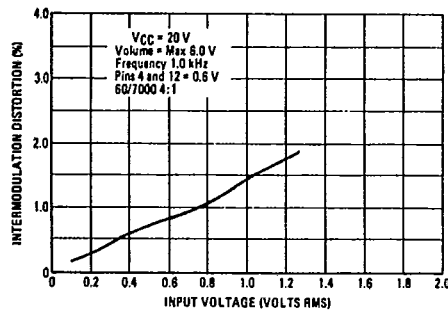


FIGURE 10 - TOTAL HARMONIC DISTORTION versus INPUT VOLTAGE

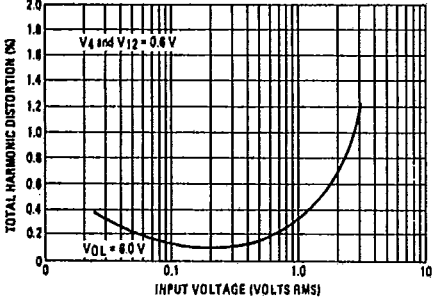
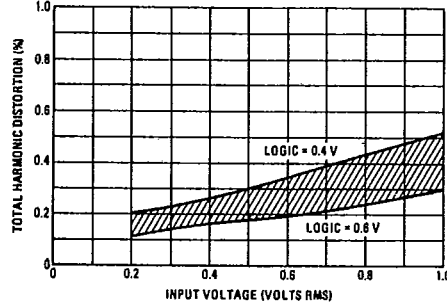


FIGURE 11 - LOGIC VOLTAGE EFFECTS ON TOTAL HARMONIC DISTORTION



Note 3: Major component of THD beyond 20 dB attenuation is noise.

ECG803 • DC LOGIC ENHANCEMENT CONTROL UNIT

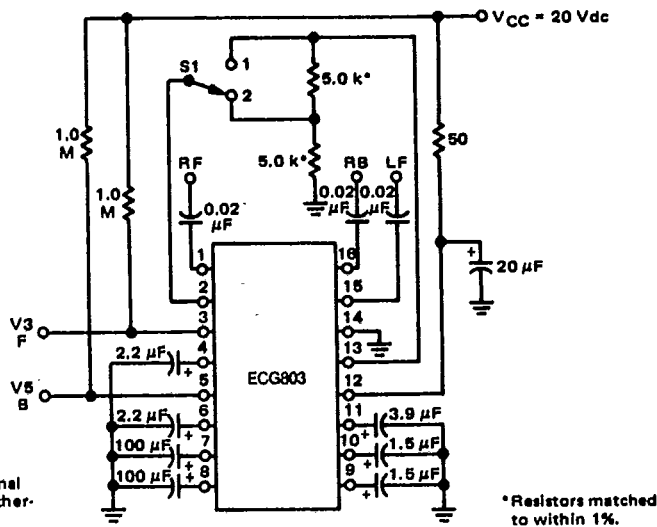
MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Value	Unit
Supply Voltage (Note 1)	26	V
Input Signal Voltage	±4.0	V _{pk}
Bias Terminal Current	±2.0	mA
Output Current	±2.0	mA
Power Dissipation @ T _A = 25°C	750	mW
Derate above +25°C	0.7	mW/°C
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 20 Vdc, Logic Control = 50%, V_{IN} = 0.5 Vrms, f = 2.0 kHz, unless otherwise noted, Note 1).

Characteristic	Min	Typ	Max	Unit
Supply Current (Pin 12) @ V _{IN} = 0	-	7.0	13	mA
@ V _{IN} = 1.4 Vrms	-	15	-	mA
Input Resistance @ Pin 1, 15, 16	-	20	-	kΩ
Output Resistance @ Pin 3, 5	-	1.5	-	kΩ
Paraphase Filter Resistance @ Pin 9, 10	-	4.0	-	kΩ
Front-Back Logic Discharge Resistance @ Pin 7, 8	-	5.0	-	kΩ
Bias Voltage (10 k to ground) @ Pin 13	-	1.4	-	Vdc
Logic Control Input Current @ Pin 2 (V ₂ = V ₁₃ or V ₂ = 0)	-	±0.5	-	mA
Quiescent Input Voltage (V _{IN} = 0) @ Pin 1, 15, 16	-	7.0	-	Vdc
Quiescent Output Voltage (V _{IN} = 0)	0.48	-	0.72	Vdc
Quiescent Output Offset (V _{IN} = 0)	-	±0.02	±0.1	Vdc
Relative Output Change				
Front output with L _B or R _B inputs or back output with L _F or R _F inputs	2.1	2.8	5.0	V/V
	7.5	9.0	14	dB
Back output with C _F input	1.9	2.5	3.5	V/V
	5.5	8.0	11	dB
Front output with L _F , C _F or R _F inputs or back output with L _B or R _B input	0.8	0.87	0.56	V/V
	2.2	3.5	5.0	dB
AGC Leveling - V _{IN} = 1.4 Vrms to V _{IN} = 50 mVrms (Note 2) Figure 8 (AGC1, AGC2)	-	1.0	3.0	dB
Quiescent Output Voltage at Max Logic (S ₁ in Position 1, Figure 12) (V _{IN} = 0, V ₂ = V ₁₃)	0.45	-	0.83	Vdc
Max Logic Relative Output Change (V ₂ = V ₁₃)				
Front output with L _B or R _B inputs or back outputs with L _F , C _F or R _F inputs	-	5.0	-	V/V
	-	14	-	dB
Front output with L _F , C _F or R _F inputs or back outputs with L _B or R _B inputs	-	0.87	-	V/V
	-	3.5	-	dB

FIGURE 12 — ECG803 TEST CIRCUIT



S₁ shown in normal position unless otherwise specified.

*Resistors matched to within 1%.

ECG803 • DC LOGIC ENHANCEMENT CONTROL UNIT

TABLE 1 - DEFINITION OF INPUT SIGNALS: (f = 2.0 kHz)

V _i Name	Signal Description	Apply To Pin	V _i Name	Signal Description	Apply To Pin
RF	0.5 V rms $\angle 0^\circ$	1	CF	0.35 V rms $\angle 0^\circ$	1
	0.35 V rms $\angle -90^\circ$	16		0.35 V rms $\angle -45^\circ$	16
	(1)	15		0.35 V rms $\angle 0^\circ$	15
LF	(1)	1			
	0.35 V rms $\angle 0^\circ$	16			
	0.5 V rms $\angle 0^\circ$	15			
LB	0.35 V rms $\angle 180^\circ$	1	AGC1	(1)	15
	(1)	16		1.0 V rms $\angle -90^\circ$	16
	0.35 V rms $\angle -90^\circ$	15		1.4 V rms $\angle 0^\circ$	1
RB	0.35 V rms $\angle 90^\circ$	1	AGC2	(1)	15
	0.5 V rms $\angle 0^\circ$	16		35 mV rms $\angle -90^\circ$	16
	0.35 V rms $\angle 0^\circ$	15		50 mV rms $\angle 0^\circ$	1

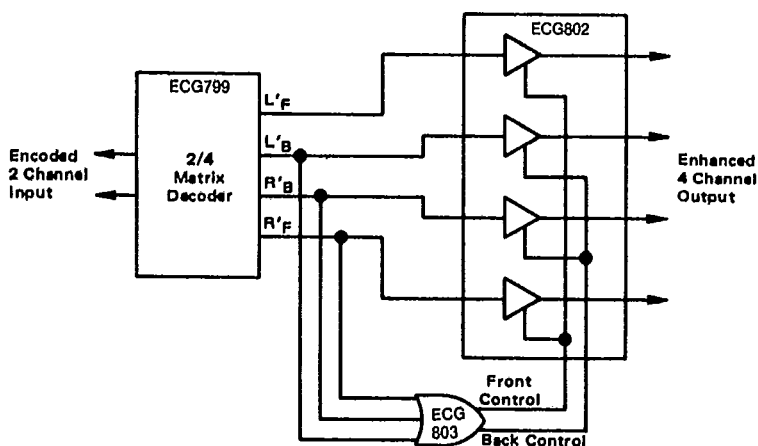
- (1) All unused inputs shall be ac grounded.
- (2) This signal not used at present.

WHY LOGIC?

Enhances front to back separation from 6 dB to 20 dB.

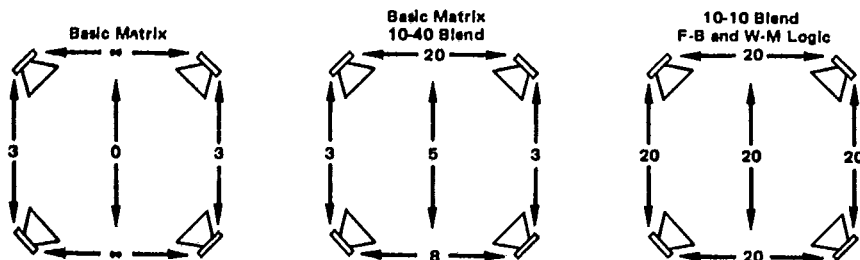
Front-to-back separation of SQ material can be enhanced by the ECG803 logic circuit which detects the presence of dominant front or back signals and adjusts the front-back gain relationship of the ECG802 to enhance the relative gain of the dominant channels.

LOGIC DECODER



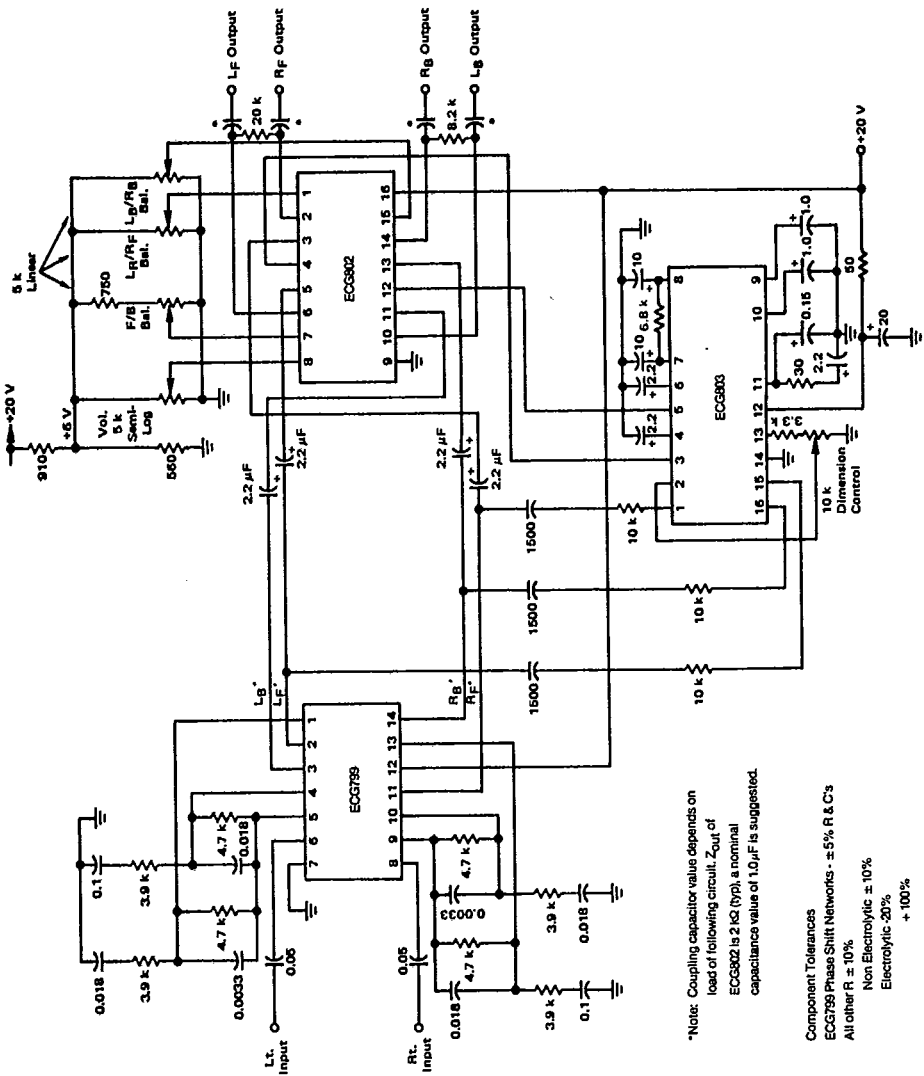
Front and back control voltages (from the ECG803) are connected to the ECG802. Although the relative gains of the front and back channels are altered with these control signals, they vary in a complementary manner to maintain constant power output from the ECG802.

CHANNEL SEPARATION



Numbers indicate Channel Separation in dB

FIGURE 13—SQ LOGIC SYSTEM (#1A)



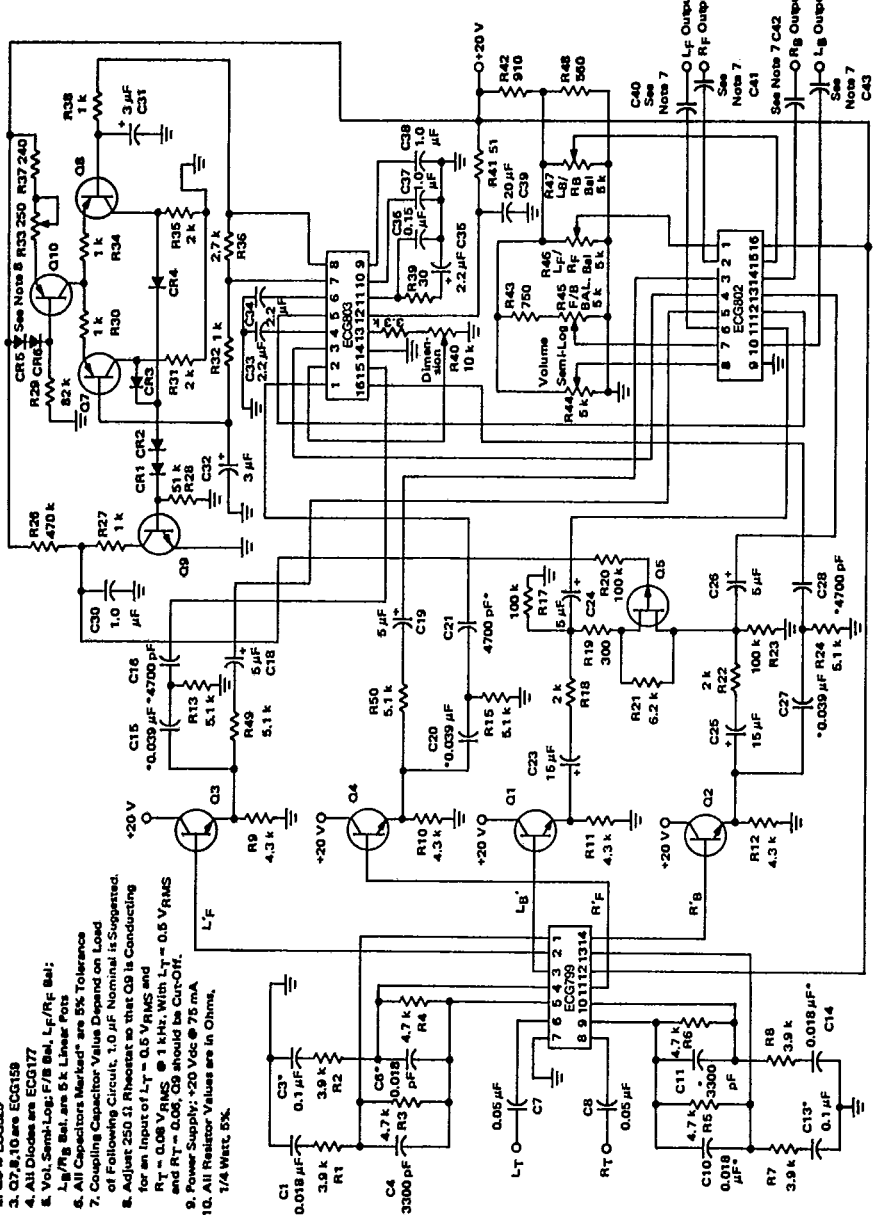
*Note: Coupling capacitor value depends on load of following circuit. Z_{out} of ECG802 is 2 kΩ (typ), a nominal capacitance value of 1.0 μF is suggested.

Component Tolerances
 ECG799 Phase Shift Networks - ±5% R & C's
 All other R - ±10%
 Non Electrolytic ±10%
 Electrolytic -20%
 +100%

FIGURE 14 - LOGIC SYSTEM WITH VARIABLE BLEND (2A)

NOTES: (Unless otherwise specified)

1. Q1, Q2, Q3, Q9 are ECG189
2. Q8 is ECG328
3. Q7, Q10 are ECG159
4. All Diodes are ECG177
5. Vol. Semi-Log. F/B Bal., L_p/R_f Bal.; L_p/R_f Bal. are 5k Linear Pots
6. All Capacitors Marked* are 5% Tolerance
7. Coupling Capacitor Value Depends on Load of Following Circuit, 1.0 μF Nominal is Suggested.
8. Adjust 250 Ω Rheostat so that Q9 is Conducting for an Input of L_T = 0.5 VRMS and R_T = 0.08 VRMS @ 1 kHz; With L_T = 0.5 VRMS and R_T = 0.05 VRMS should be Cut-Off.
9. Power Supply: +20 Vdc @ 75 mA
10. All Resistor Values are in Ohms, 1/4 Watt, 5%.



TYPICAL SYSTEM PERFORMANCE CHARACTERISTICS

Power Supply Requirements:	60 mA (L1a), 75 mA (L2a) @ 20 V
Nominal Signal Level:	0.5 V
Maximum Input Voltage:	1.9 V
Input Impedance:	2 MΩ
Output Impedance:	2 kΩ
Total Harmonic Distortion:	0.2% at nominal input
at 1 Hz	1.0% at maximum input
Voltage Gain (at quiescent):	1.0
4 Channel Volume Control	Range - 70 dB
	Tracking - within 3 dB
4 Channel Balance Control:	-35 dB at -20 dB gain

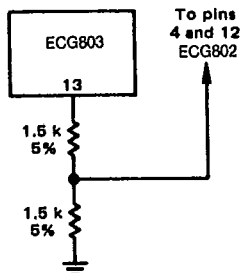
NOTES

ECG802

1. If volume control is not used, connect Pin 8 to +6.0 V.
2. If balance controls are not used, open Pins 1, 7 and 15.
3. L_F/R_F and L_B/R_B balance controls can be ganged by connecting Pins 1 and 15.
4. Signal handling capability is reduced at maximum logic (20 dB front to back separation) unless V_{CC} = 25 V on ECG802.

ECG803

1. The logic control will provide enhancement of front to back separation from 6 dB typical to 20 dB max (15 dB typical at the recommended operating level of 60% control).
2. To defeat the logic use the circuit connections as shown on right.



SYSTEM CHARACTERISTICS

FIGURE 15 - GAIN versus F/B BALANCE

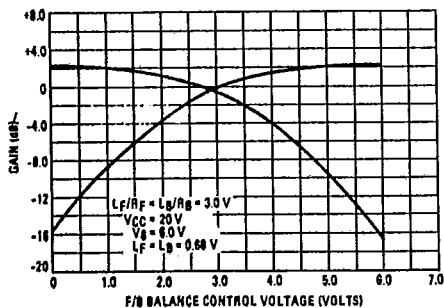
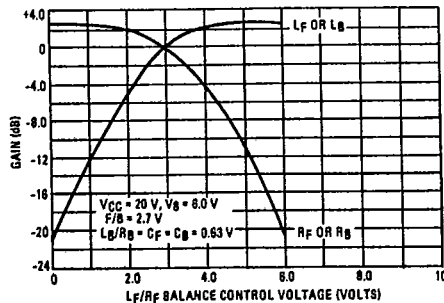


FIGURE 16 - GAIN versus L_F/R_F BALANCE CONTROL



Signal Definitions for Total System

Test signals shall have the following relative phase and amplitude characteristics.

Source Location	Input Signals	
	L _T	R _T
L _F	1	0
C _F	.71	.71
R _F	0	1
L _B	.71/-90°	.71/180°
R _B	.71	.71/90°

Where L_F is left front, R_B is right back, C_F is center front, etc.

1. System Tests: ECG799, ECG802, ECG803 I

- a) L_F source - connect signal to L_T input, ac ground R_T input of ECG799.
- b) R_F source - apply signal to R_T , ac ground L_T .
- c) C_F source - apply equal signals to L_T and R_T inputs.

NOTES: Balance control inputs of ECG802 may be opened for convenience or set for perfect balance with C_F and C_B inputs; set logic control to 50%. Max signal should be limited to 1.6 Vrms L_T or R_T : ECG802 outputs give system performance, typically 15 dB front back separation for corners, 12 dB for center front, center back.

2. Logic Circuit Tests: ECG803

- a) L_F source - apply $L_F' = \sqrt{2} R_B'$, $R_F' = 0$; dc voltage at Pin 3 should decrease by 3 dB, at Pin 5 should increase by 9 dB.
- b) R_B source - apply $R_F' = \sqrt{2} R_B'$, $R_F' = 0$; dc voltage at Pin 3 should increase by 9 dB, at Pin 5 should decrease by 3 dB.

3. Voltage Controlled Amplifier Tests: ECG802

- a) Volume control - with balance controls open or balanced, gain should be +0.5 dB at 6 V on Pin 8 and less than -60 dB at 0 V.
- b) Balance controls - with balance controls at Pins 1 and 15 at 16% of supply and Pin 7 at 13% of supply, system is nominally balanced. Taking Pin 1 to ground should increase L_F gain by 3 dB and decrease R_F gain by greater than 12 dB at maximum volume and 30 dB at lower volume levels.