HM511000A Series
HM511000AL Series

1048576-Word x 1-Bit CMOS Dynamic RAM

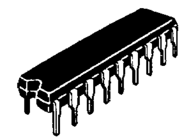
■ DESCRIPTION

The Hitachi HM511000A/AL series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000A/AL has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000A/AL offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM511000A/AL to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

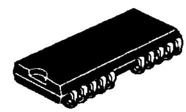
HM511000A/ALP Series



3DDP18C

(DP-18C)

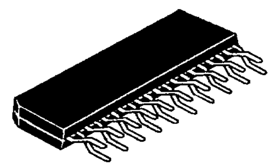
HM511000A/ALJP Series



3DCP20D

(CP-20D)

HM511000A/ALZP Series



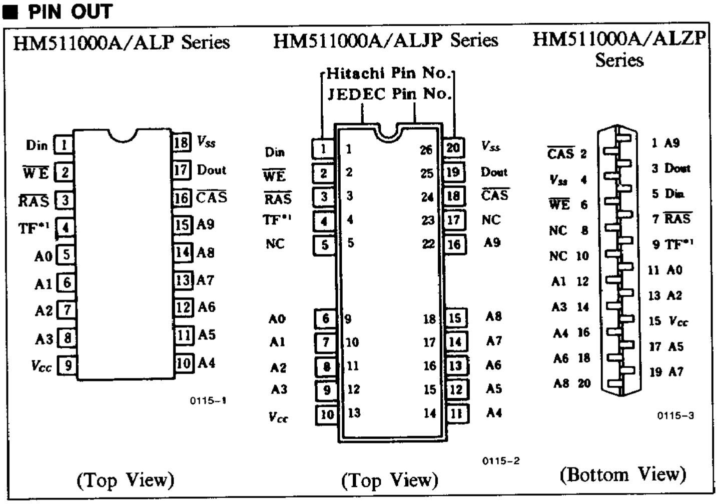
3DZP20

(ZP-20)

■ FEATURES

- High Speed
  - Access Time ....60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode ....495 mW/440 mW/385 mW/330 mW/275 mW (max)
  - Standby Mode ....11 mW (max)
- Single 5V Supply (±10%)
- Fast Page Mode Capability
- 512 Refresh Cycles ....(8 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh

■ PIN OUT



■ PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_8	Refresh Address Input
D_{in}	Data-in
D_{out}	Data-out
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
TF[1]	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground

Note: 1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

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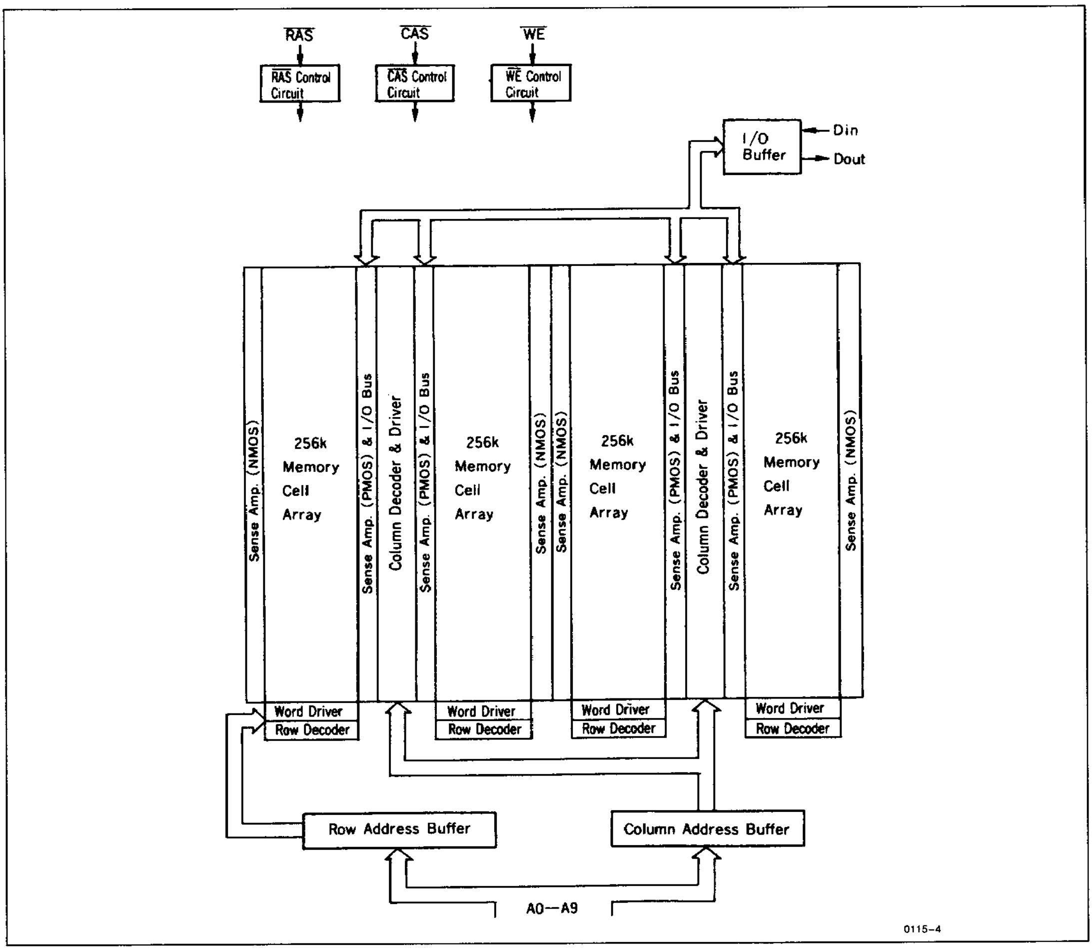
■ ORDERING INFORMATION

Part No.	Access Time	Package
HM511000AP-6	60 ns	300 mil 18-pin Plastic DIP (DP-18C)
HM511000AP-7	70 ns	
HM511000AP-8	80 ns	
HM511000AP-10	100 ns	
HM511000AP-12	120 ns	
HM511000AJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM511000AJP-7	70 ns	
HM511000AJP-8	80 ns	
HM511000AJP-10	100 ns	
HM511000AJP-12	120 ns	
HM511000AZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM511000AZP-7	70 ns	
HM511000AZP-8	80 ns	
HM511000AZP-10	100 ns	
HM511000AZP-12	120 ns	

Part No.	Access Time	Package
HM511000ALP-6	60 ns	300 mil 18-pin Plastic DIP (DP-18C)
HM511000ALP-7	70 ns	
HM511000ALP-8	80 ns	
HM511000ALP-10	100 ns	
HM511000ALP-12	120 ns	
HM511000ALJP-6	60 ns	300 mil 20-pin Plastic SOJ (CP-20D)
HM511000ALJP-7	70 ns	
HM511000ALJP-8	80 ns	
HM511000ALJP-10	100 ns	
HM511000ALJP-12	120 ns	
HM511000ALZP-6	60 ns	400 mil 20-pin Plastic ZIP (ZP-20)
HM511000ALZP-7	70 ns	
HM511000ALZP-8	80 ns	
HM511000ALZP-10	100 ns	
HM511000ALZP-12	120 ns	

■ BLOCK DIAGRAM



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■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	−2.0	—	0.8	V

Note: All voltages referenced to V_{SS}.

• DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000 /A-8		HM511000 /A-10		HM511000 /A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	1	—	1	—	1	—	1	—	1	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V D_{out} = High-Z	
		—	300	—	300	—	300	—	300	—	300	μA	CMOS Interface L-Version	
Refresh Current	I_{CC3}	—	90	—	80	—	60	—	50	—	45	mA	$\overline{RAS}$ Only Refresh, t_{RC} = Min	2
Battery Back Up Current (Only for L-Version)	I_{CC4}	—	300	—	300	—	300	—	300	—	300	μA	t_{RC} = 125 μs, $\overline{CAS}$ Before $\overline{RAS}$ Cycling	4
Standby Current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{out} = Enable	1
Refresh Current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CAS}$ Before $\overline{RAS}$ Refresh t_{RC} = Min	
Fast Page Mode Current	I_{CC7}	—	80	—	70	—	50	—	50	—	40	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = Min	1, 3

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• **DC Electrical Characteristics** (V_{CC} = 5V ±10%, V_{SS} = 0V, T_A = 0 to +70°C) (continued)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000 /A-8		HM511000 /A-10		HM511000 /A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Input Leakage	I_{L1}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{in} = 0 to +7V	
Output Leakage	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	V_{out} = 0 to +7V, D_{out} = Disable	
Output Levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once while $\overline{CAS}$ = V_{IH}.
4. t_{RAS} = t_{RAS} (min) to 1 μs
Input voltage: All pins: $V_{IH} \geq V_{CC} - 0.2V$ or $V_{IL} \leq 0.2V$.

• **Capacitance** (V_{CC} = 5V ±10%, T_A = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input Capacitance	Address, Data Input	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7	pF	1
Output Capacitance	Data Output	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ±10%)

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8V, 2.4V (Including scope and jig)
Output load: 2 TTL Gate + C_L (100 pF)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	
Refresh Period (Only for L-Version)	t_{REF}	—	64	—	64	—	64	—	64	—	64	ms	

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Read Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	10
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-Write Cycle Time	t_{RWC}	145	—	155	—	190	—	220	—	255	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	—	70	—	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	—	20	—	25	—	25	—	30	—	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30	—	35	—	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	0	—	0	—	ns	

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Fast Page Mode Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	70	—	75	—	85	—	85	—	100	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. An initial pause of 100 μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycle.
14. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

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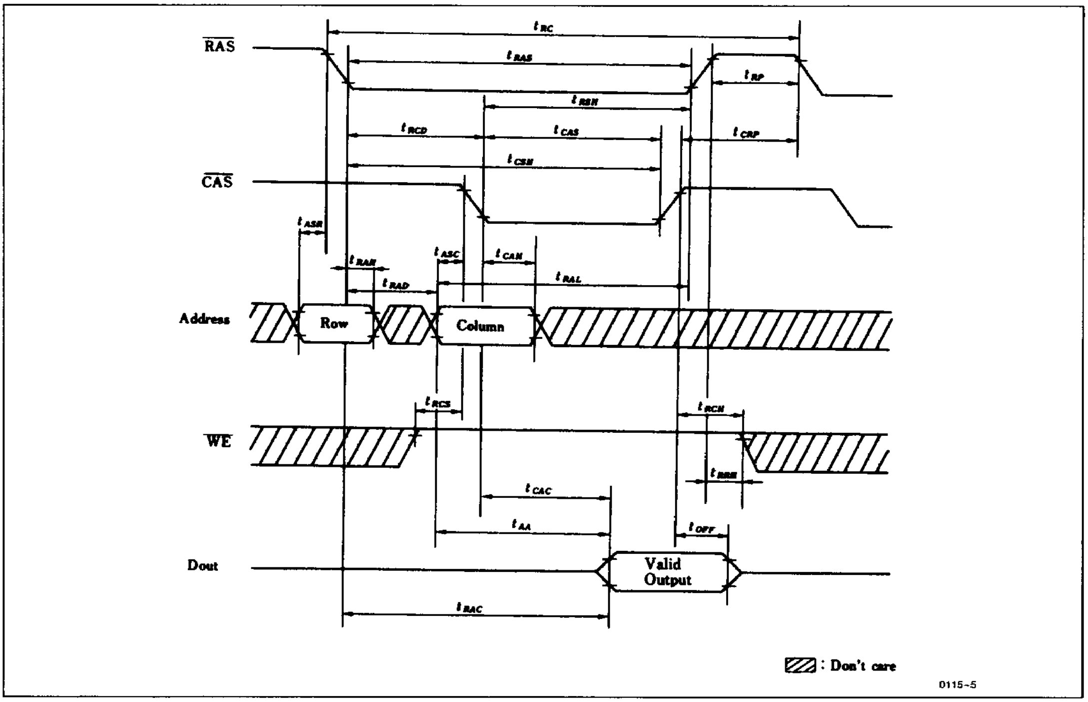
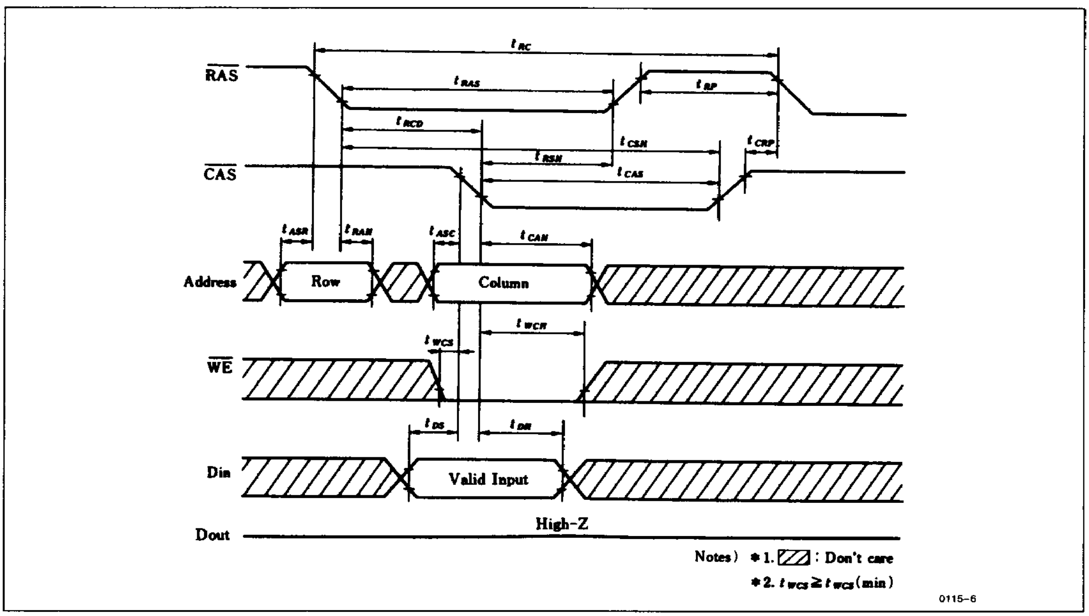
■ TIMING WAVEFORMS

• **Read Cycle**



• **Early Write Cycle**



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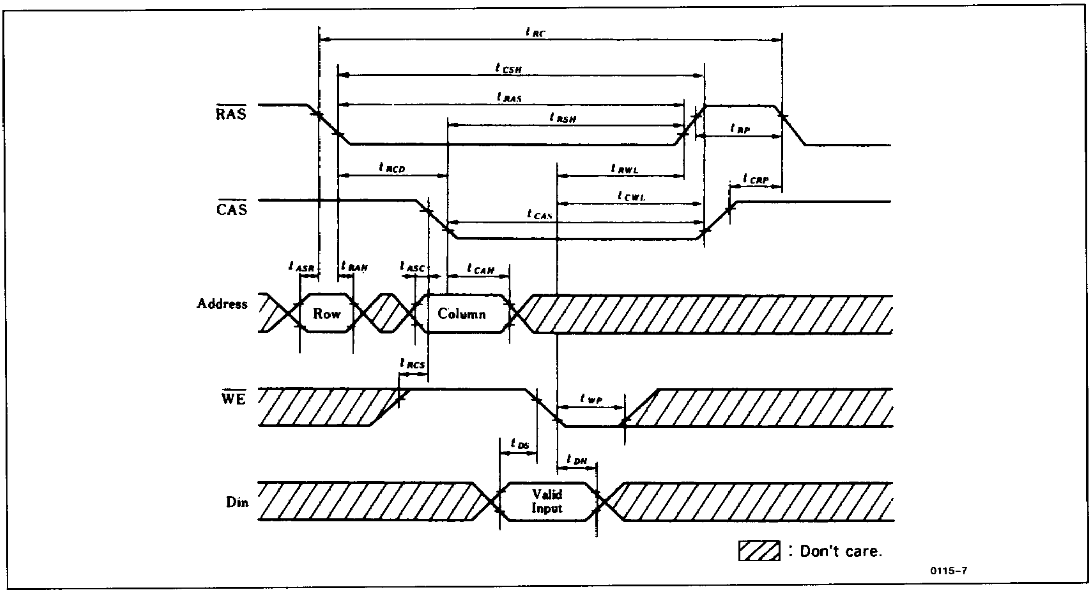
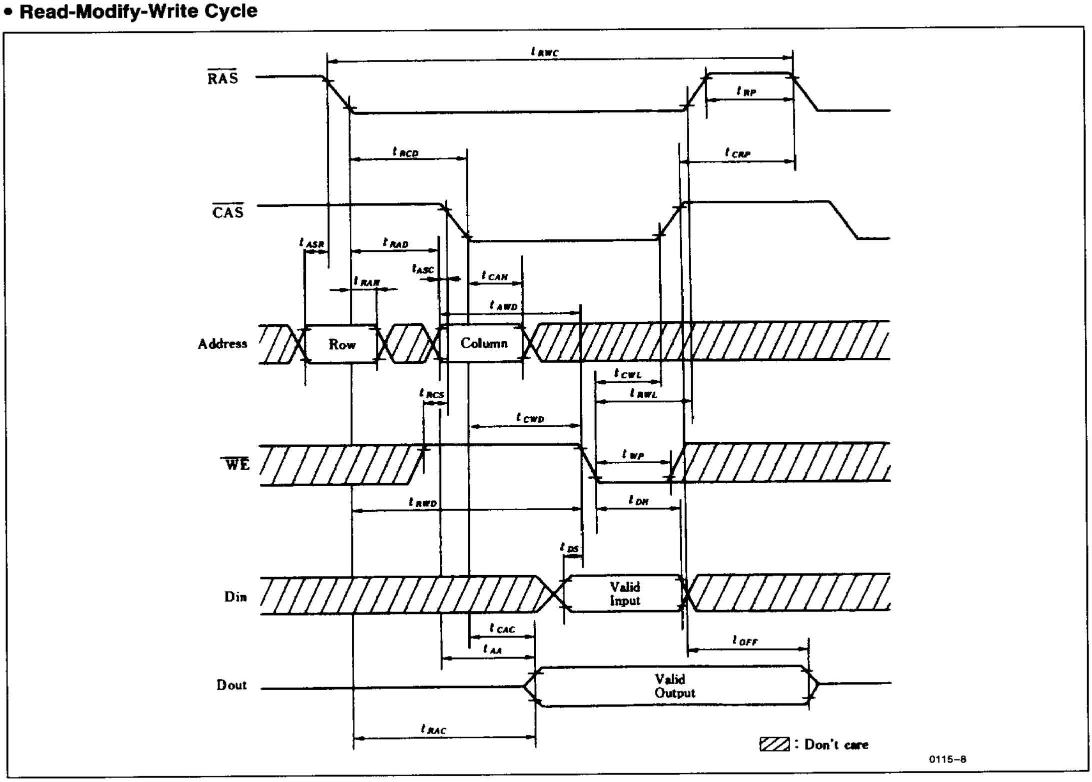
- **Delayed Write Cycle**



- **Read-Modify-Write Cycle**



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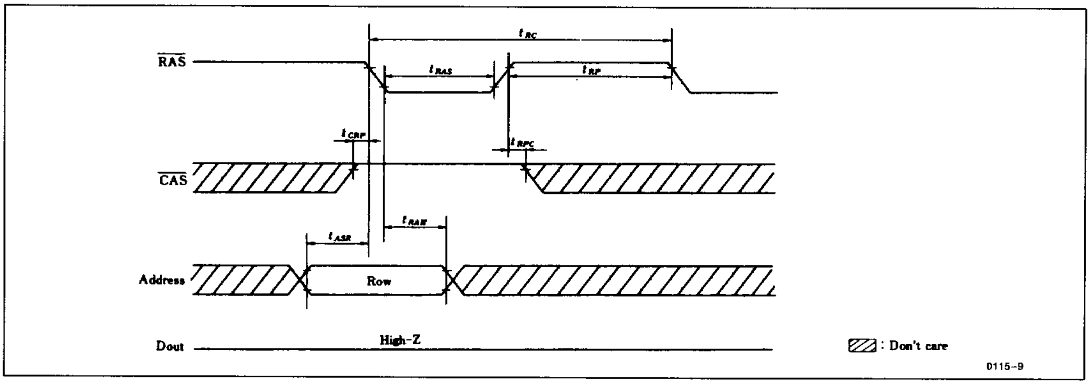
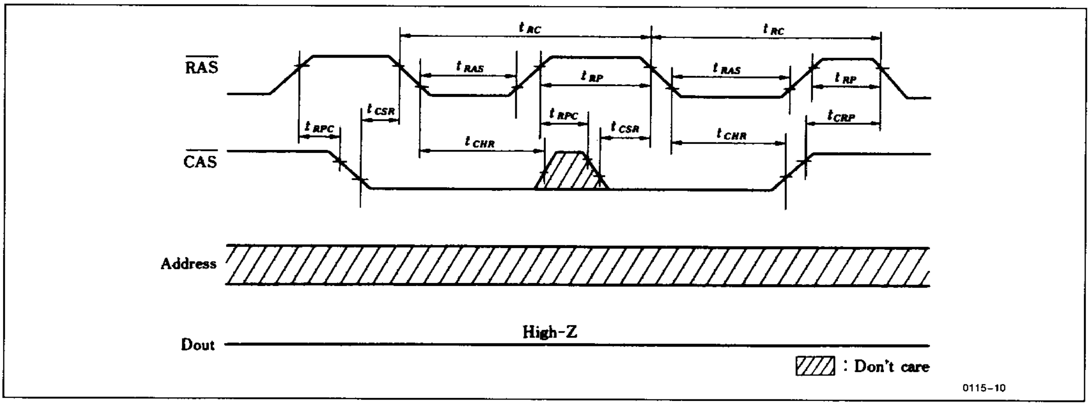
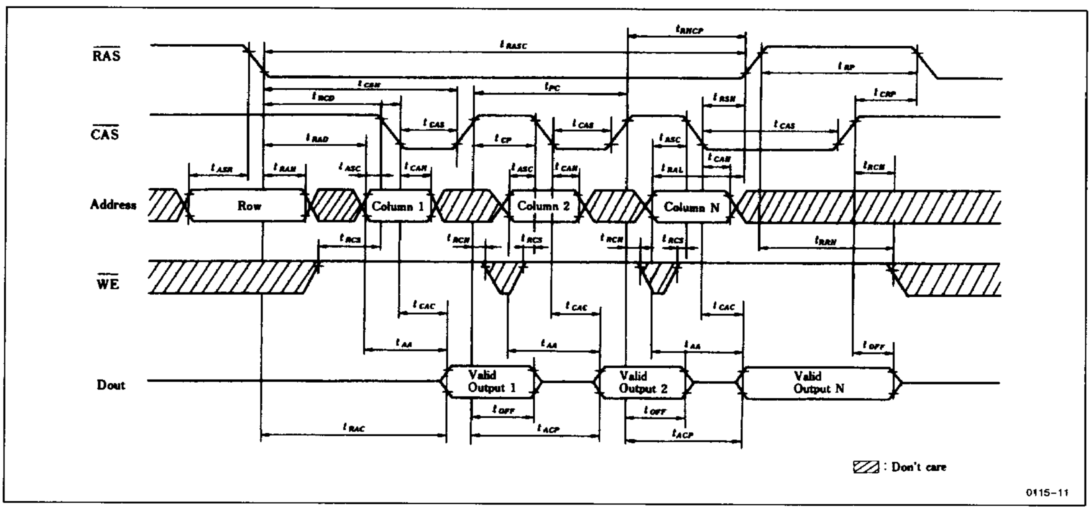
- **$\overline{RAS}$ Only Refresh Cycle**



- **$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle**



- **Fast Page Mode Read Cycle**



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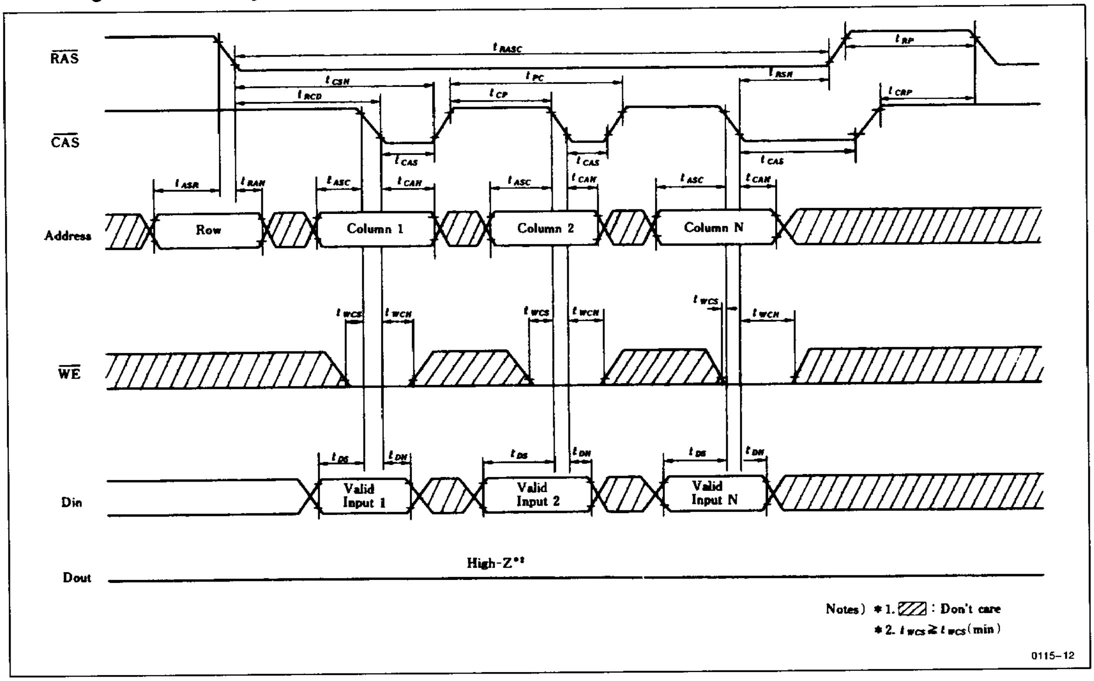
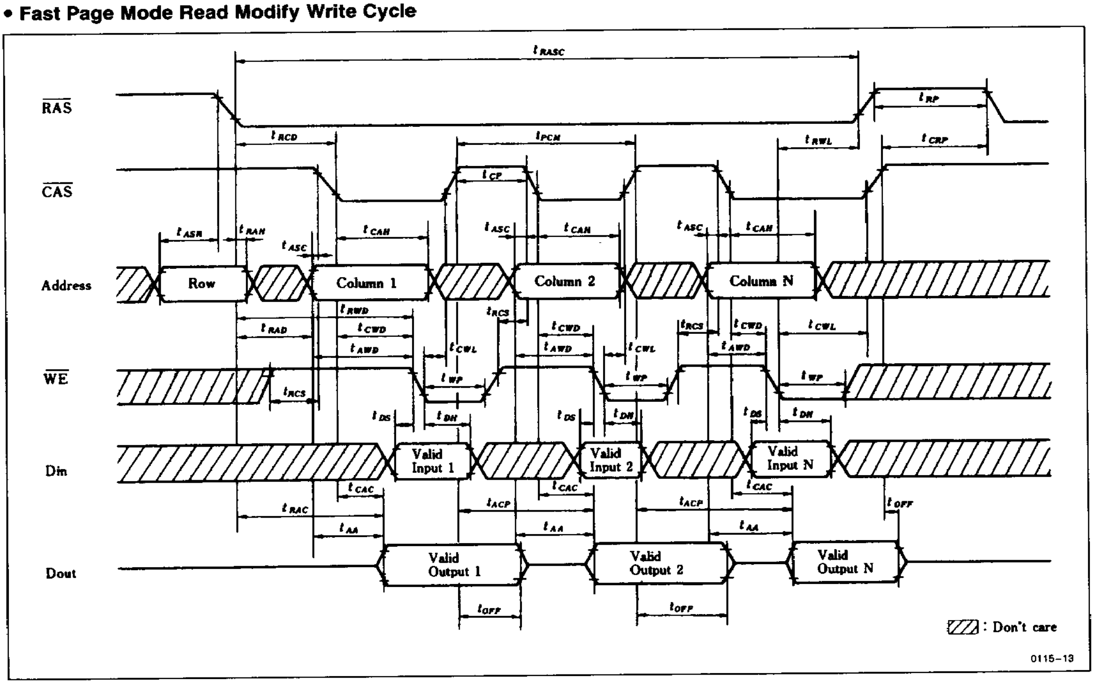
- **Fast Page Mode Write Cycle**



- **Fast Page Mode Read Modify Write Cycle**



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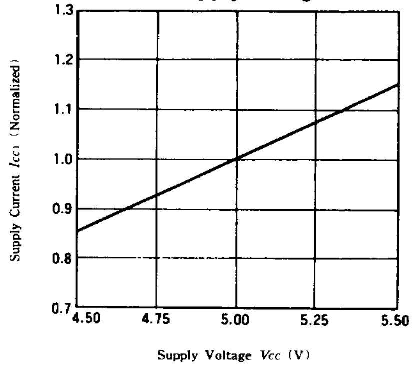
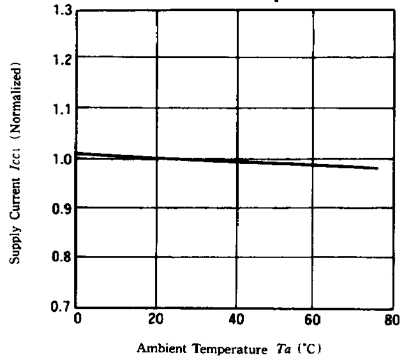
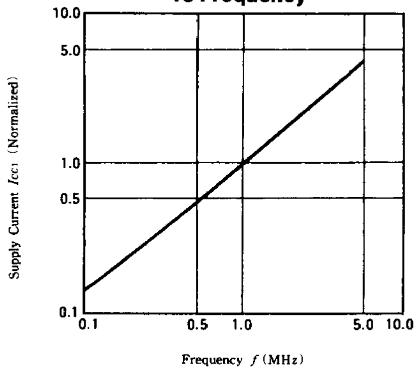
Supply Current (Active) vs Supply Voltage



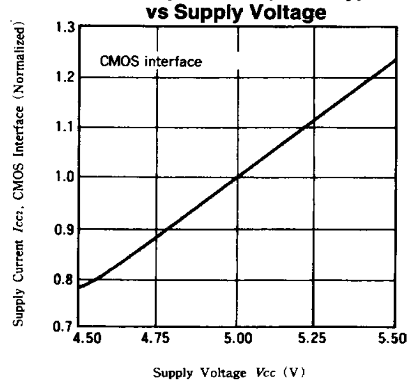
Supply Current (Active) vs Ambient Temperature



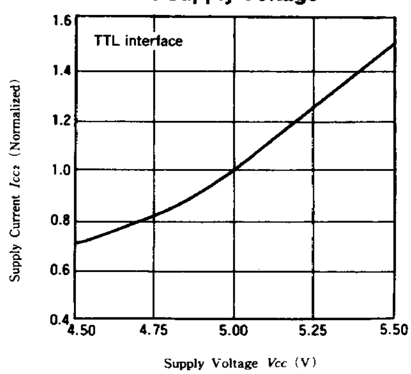
Supply Current (Active) vs Frequency



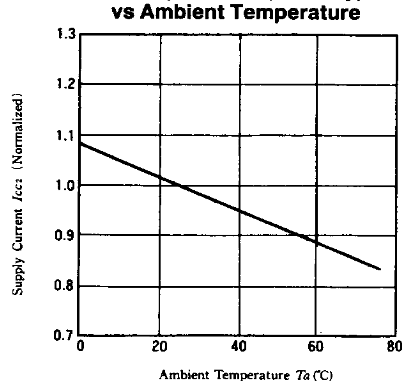
Supply Current (Standby) vs Supply Voltage



Supply Current (Standby) vs Supply Voltage



Supply Current (Standby) vs Ambient Temperature



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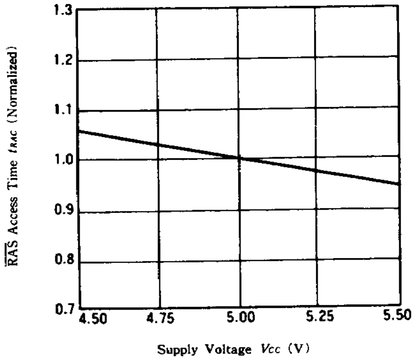
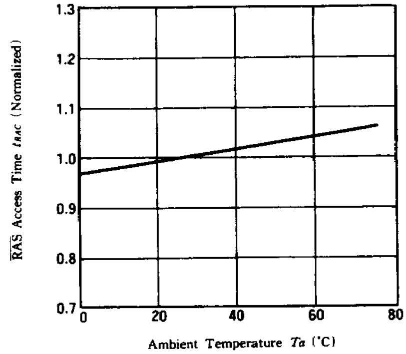
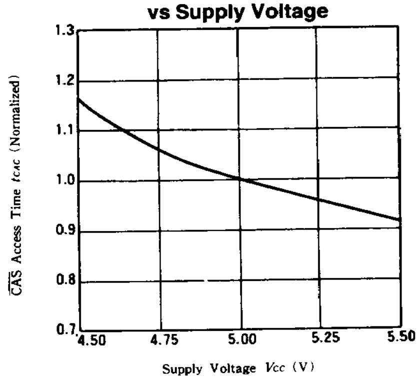
$\overline{RAS}$ Access Time vs Supply Voltage



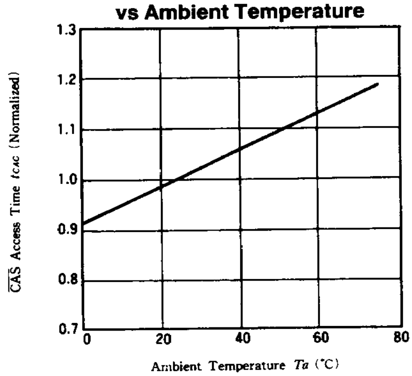
$\overline{RAS}$ Access Time vs Ambient Temperature



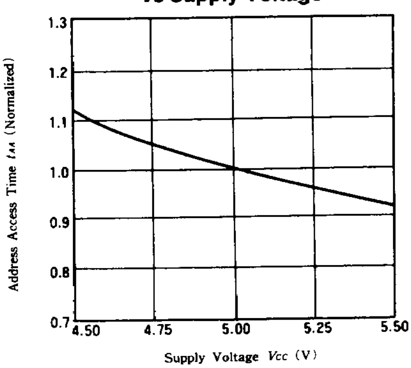
$\overline{CAS}$ Access Time vs Supply Voltage



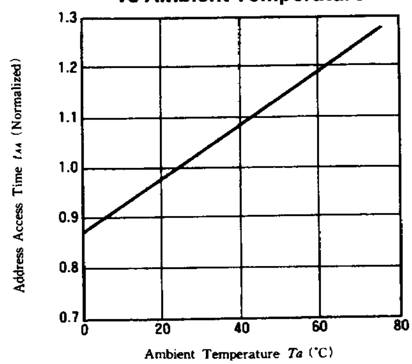
$\overline{CS}$ Access Time vs Ambient Temperature



Address Access Time vs Supply Voltage



Address Access Time vs Ambient Temperature



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