SILICON DIFFUSED POWER TRANSISTORS

High-voltage, high-speed, glass-passivated npn power transistors in a SOT93 envelope intended for use in power supplies and deflection circuits for colour receivers and monitors.

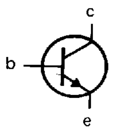
QUICK REFERENCE DATA

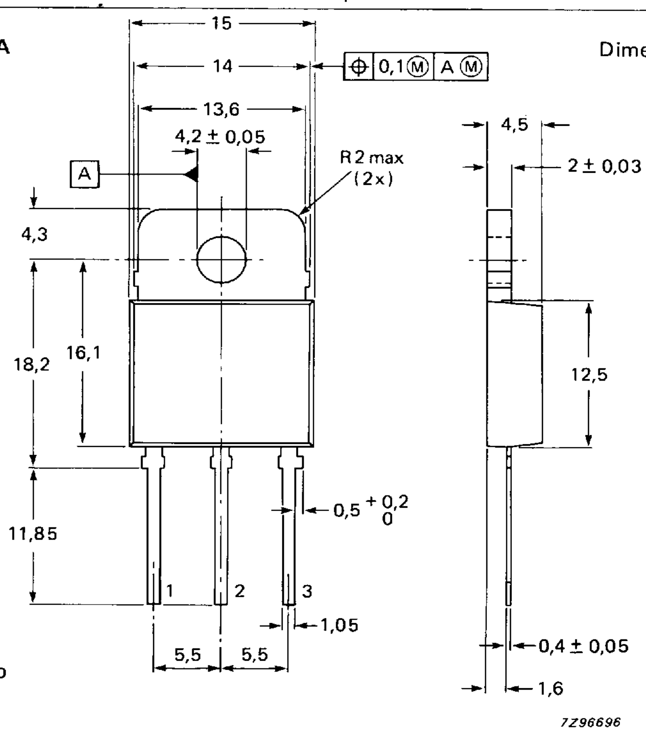
Collector-emitter voltage			
peak value; $V_{BE} = 0$	V_{CESM}	max.	1350 V
open base	V_{CEO}	max.	550 V
Saturation voltages	V_{CEsat}	max.	2.0 V
	V_{BEsat}	max.	1.5 V
Collector current			
saturation	I_{Csat}	max.	3.2 A
DC	I_C	max.	6.0 A
peak value	I_{CM}	max.	8.0 A
Total power dissipation			
up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	125 W
DC current gain			
$I_C = 3.2$ A; $V_{CE} = 2$ V	h_{FE}	min.	6.0
Switching times; resistive load			
fall time	t_f	max.	0.7 μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT93.





Pinning:

1 = base
2 = collector
3 = emitter

Collector connected to mounting base.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage			
peak value; $V_{BE} = 0$	V_{CESM}	max.	1350 V
open base	V_{CEO}	max.	550 V
Emitter-base voltage	V_{EBO}	max.	6.0 V
Collector current			
DC	I_C	max.	6.0 A
peak value	I_{CM}	max.	8.0 A
Base current			
DC	I_B	max.	2.0 A
peak value	I_{BM}	max.	4.0 A
Emitter current			
DC	I_E	max.	8.0 A
peak value	I_{EM}	max.	12 A
Total power dissipation			
up to $T_{mb} = 25\ ^oC$	P_{tot}	max.	125 W
Storage temperature range	T_{stg}		−65 to + 150 ^oC
Junction temperature	T_j	max.	150 ^oC

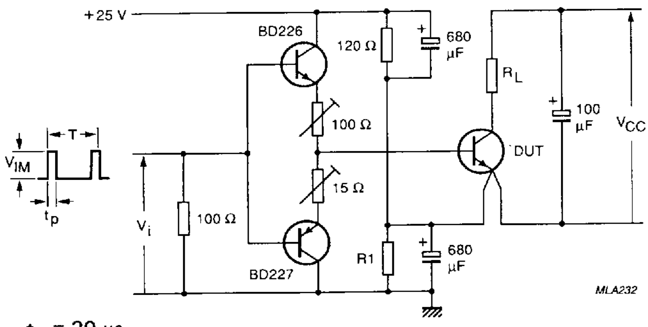
THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1.0 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current			
$V_{BE} = 0$; $V_{CE} = V_{CESmax}$	I_{CES}	max.	1.0 mA
$V_{BE} = 0$; $V_{CE} = V_{CESmax}$; T_j = 125 °C	I_{CES}	max.	2.0 mA
Emitter cut-off current			
$I_C = 0$; V_{EB} = 6 V	I_{EBO}	max.	1.0 mA
Collector-emitter breakdown voltage			
I_C = 100 mA; $I_B = 0$	V_{CEO}	min.	550 V
Saturation voltage			
I_C = 3.2 A; I_B = 0.53 A	V_{CEsat}	max.	2.0 V
I_C = 6.0 A; I_B = 2.0 A	V_{CEsat}	max.	1.8 V
DC current gain			
I_C = 10 mA; V_{CE} = 5 V	h_{FE}	min.	6.0
I_C = 1.5 A; V_{CE} = 5 V	h_{FE}	min.	8.0
I_C = 3.2 A; V_{CE} = 2 V	h_{FE}	min.	6.0
I_C = 4.0 A; V_{CE} = 3 V	h_{FE}	min.	5.5
Switching times; resistive load (Figs 2 and 3)			
I_{Con} = 3.2 A; $I_{Bon} = -I_{Boff}$ = 0.53 A			
turn-on	t_{on}	max.	0.5 µs
turn-off; storage time	t_s	max.	6.0 µs
fall time	t_f	max.	0.7 µs
Switching times; inductive load (Figs 4 and 5)			
I_{Con} = 3.2 A; I_{Bon} = 0.53 A			
turn-off; storage time	t_s	max.	2.5 µs
fall time	t_f	max.	0.8 µs



t_p = 20 µs
T = 2 ms
V_{IM} = 15 V

Fig. 2 Test circuit resistive load;
V_{CC} = 240 V; R_L = 75 Ω; R1 = 33 Ω.

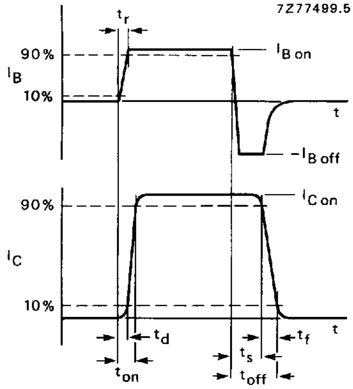


Fig. 3 Switching times waveforms with resistive load; $t_r \leqslant 30$ ns.

V_{CL} = 450 V
V_{CC} = 30 V
$-V_{BE}$ = −5 V
L_B = 2.5 µH
L_C = 200 µH

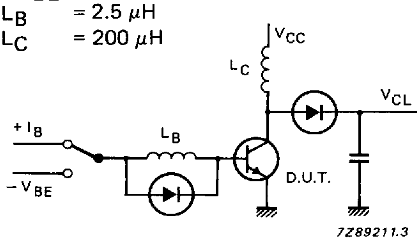


Fig. 4 Test circuit inductive load.

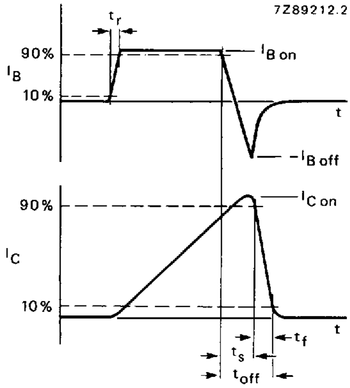


Fig. 5 Switching times waveforms with inductive load.

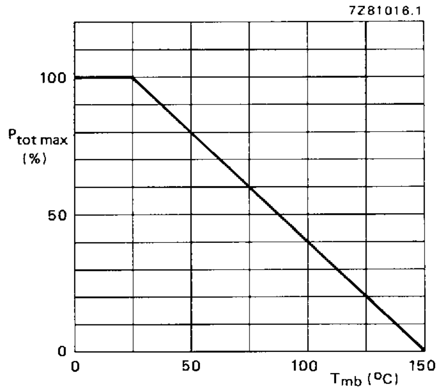
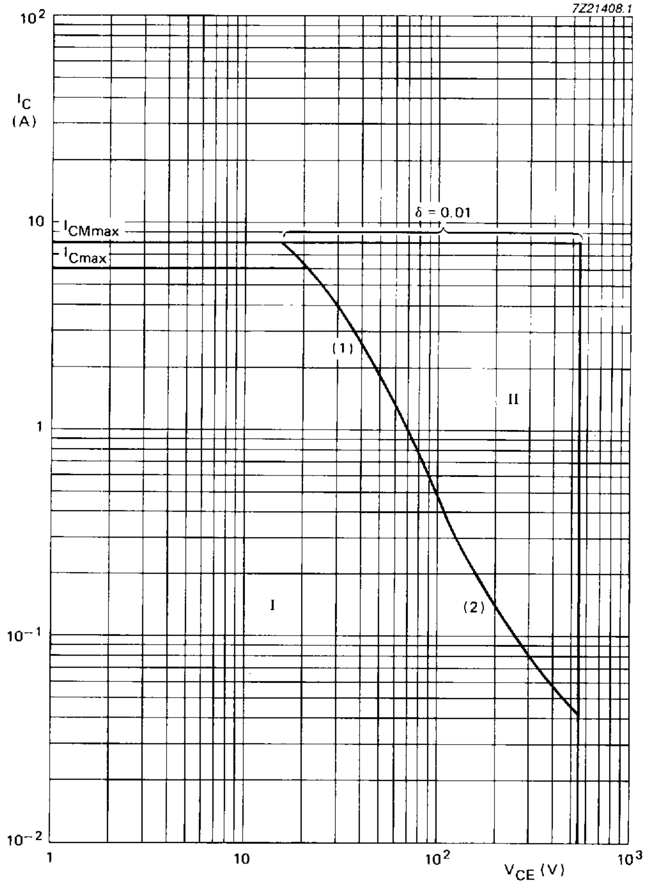


Fig. 6 Power derating curve.



(1) $P_{tot\,max}$ line.
(2) Second-breakdown limits (independent of temperature).

I Region of permissible DC operation.
II Permissible extension for repetitive pulse operation.

Fig. 7 Forward bias SOAR.

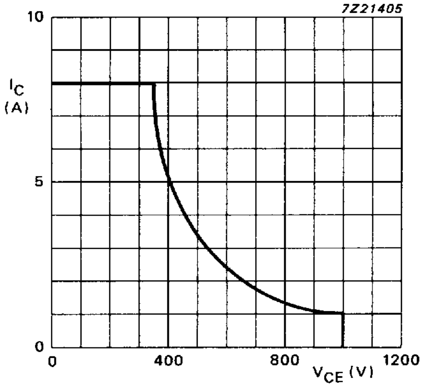


Fig. 8 Reverse bias SOAR; $-V_{BE} = 5$ V; $I_C/I_B \leq 4$; $T_j \leq 100$ °C.

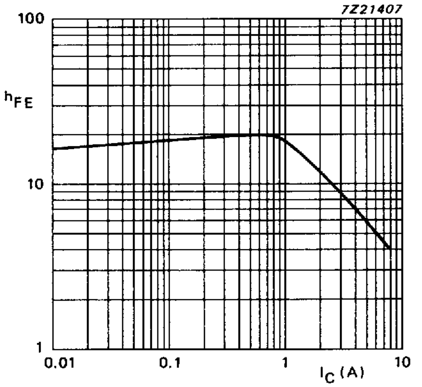


Fig. 9 Typical values DC current gain; $V_{CE} = 5$ V.

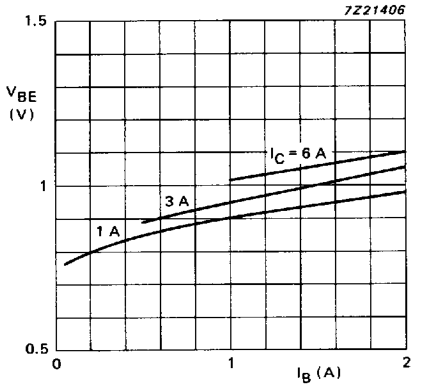


Fig. 10 Base-emitter voltage as a function of base current.

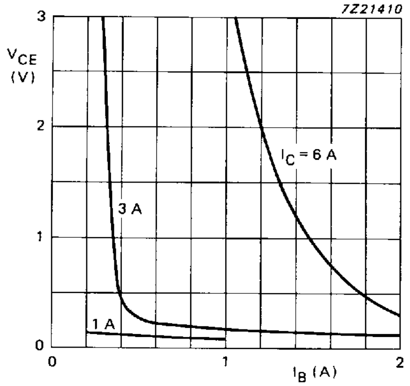


Fig. 11 Collector-emitter voltage as a function of base current.

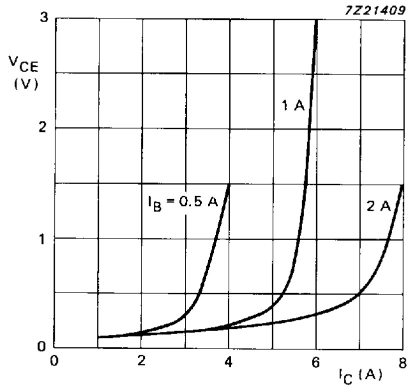


Fig. 12 Collector-emitter voltage as a function of collector current.

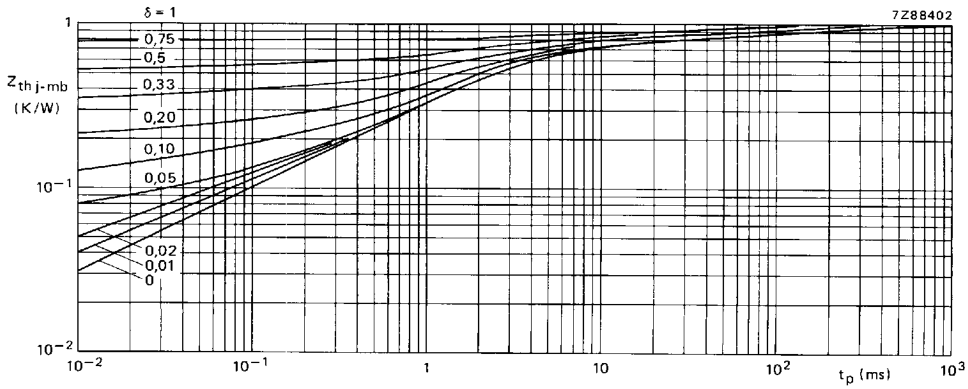


Fig. 13 Pulse power rating chart.