

DATA SHEET

BSS89

**N-channel enhancement mode
vertical D-MOS transistor**

Product specification
Supersedes data of 1997 Jun 20
File under Discrete Semiconductors, SC13b

1998 Apr 24

N-channel enhancement mode vertical D-MOS transistor

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FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

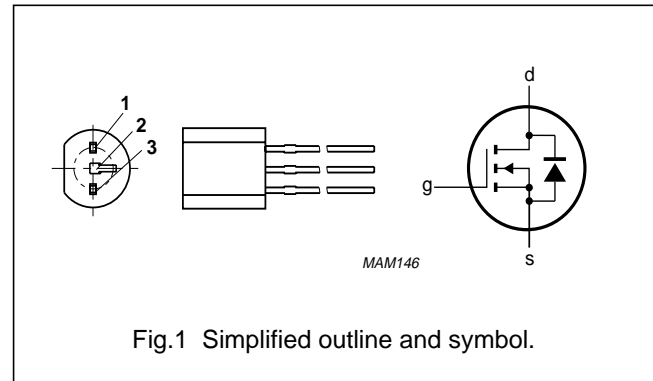
- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	± 20	V
I_D	drain current (DC)		–	–	300	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$	–	–	1	W
R_{DSon}	drain-source on-state resistance	$I_D = 400\text{ mA}; V_{GS} = 10\text{ V}$	–	4.5	6	Ω
$ y_{fs} $	forward transfer admittance	$I_D = 400\text{ mA}; V_{DS} = 25\text{ V}$	140	350	–	mS

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	200	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)		–	300	mA
I_{DM}	peak drain current		–	1.2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

- Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10×10 mm.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 250\ \mu\text{A}$	200	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\ \text{mA}$	0.8	–	2.8	V
I_{DSS}	drain-source leakage current	$V_{DS} = 60\ \text{V}$; $V_{GS} = 0$	–	–	200	nA
		$V_{DS} = 200\ \text{V}$; $V_{GS} = 0$	–	0.1	60	μA
I_{GSS}	gate leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20\ \text{V}$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 400\ \text{mA}$	–	4.5	6	Ω
$ y_{fs} $	forward transfer admittance	$I_D = 400\ \text{mA}$; $V_{DS} = 25\ \text{V}$	140	350	–	mS
C_{iss}	input capacitance	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0$; $f = 1\ \text{MHz}$	–	45	–	pF
C_{oss}	output capacitance	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0$; $f = 1\ \text{MHz}$	–	15	–	pF
C_{rss}	reverse transfer capacitance	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0$; $f = 1\ \text{MHz}$	–	3.5	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$V_{GS} = 0$ to $10\ \text{V}$; $V_{DD} = 50\ \text{V}$; $I_D = 250\ \text{mA}$	–	5	–	ns
t_{off}	turn-off time	$V_{GS} = 10$ to $0\ \text{V}$; $V_{DD} = 50\ \text{V}$; $I_D = 250\ \text{mA}$	–	15	–	ns

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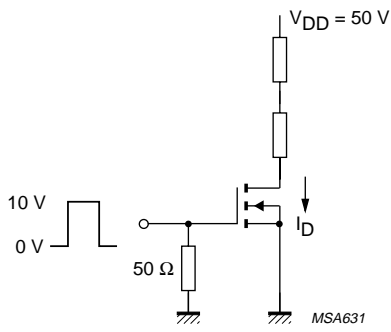


Fig.2 Switching time test circuit.

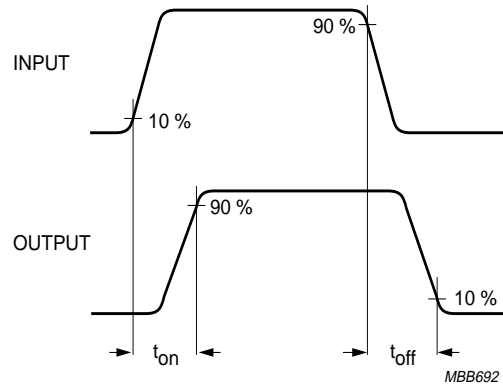


Fig.3 Input and output waveforms.

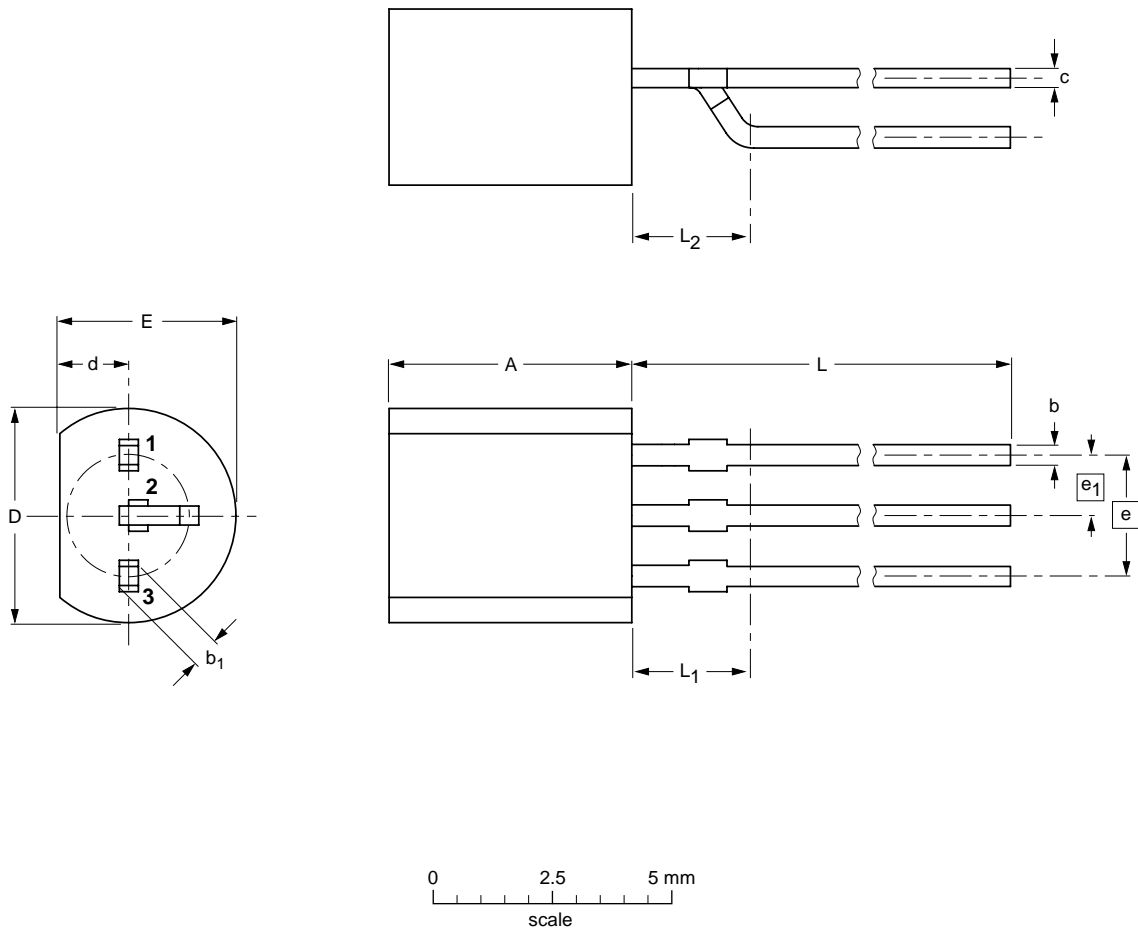
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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max	L ₂ max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92 variant	SC-43		98-03-26

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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