

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55470/75470

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
✓ SN55470	AND [†]	J
✓ SN55471	AND	JG
✓ SN55472	NAND	JG
✓ SN55473	OR	JG
✓ SN55474	NOR	JG
✓ SN75470	AND [†]	J, N
✓ SN75471	AND	JG, P
✓ SN75472	NAND	JG, P
✓ SN75473	OR	JG, P
✓ SN75474	NOR	JG, P

[†]With output transistor base connected externally to output of gate.

description

Series 55470/75470 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 55450B/75450B (limits are the same as Series 55460/75460). Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55470 drivers are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 75470 drivers are characterized for operation from 0°C to 70°C .

The SN55470 and SN75470 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55471/SN75471, SN55472/SN75472, SN55473/SN75473, and SN55474/SN75474 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

CONTENTS	PAGE
Maximum Ratings and Recommended Operating Conditions	98
Definitive Specifications	
Types SN55470, SN75470	99
Types SN55471, SN75471	101
Types SN55472, SN75472	102
Types SN55473, SN75473	103
Types SN55474, SN75474	104
Switching Time Test Circuits and Voltage Waveforms	105

SERIES 55470/75470 DUAL PERIPHERAL DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55470		SN75470		UNIT
	SN55471	SN55472 SN56473 SN55474	SN75471	SN75472 SN75473 SN75474	
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	5.5	5.5	V
V_{CC} -to-substrate voltage	40		40		V
Collector-to-substrate voltage	70		70		V
Collector-base voltage	70		70		V
Collector-emitter voltage (see Note 3)	70		70		V
Collector-emitter voltage (see Note 4)	40		40		V
Emitter-base voltage	5		5		V
Off-state output voltage		70		70	V
Continuous collector or output current (see Note 5)	400	400	400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 5)	500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	J package	1375	1025		mW
	JG package		1050	825	
	N package			1150	
	P package			1000	
Operating free-air temperature range	-55 to 125	-55 to 125	0 to 70	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	°C

- NOTES:
1. Voltage values are with respect to network ground terminal unless otherwise specified.
 2. This is the voltage between two emitters of a multiple-emitter transistor.
 3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
 4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
 5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
 6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN55470 through SN55474 chips are alloy-mounted; SN75470 through SN75474 chips are glass-mounted.

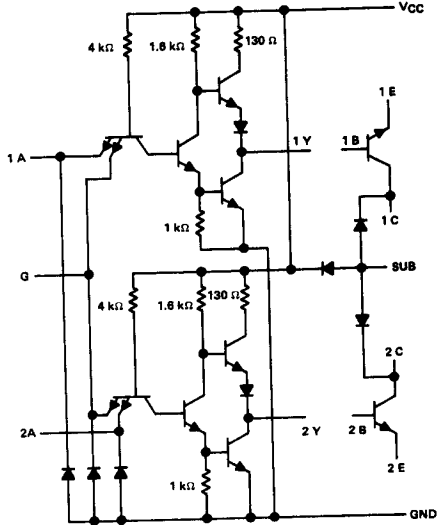
recommended operating conditions (see Note 7)

	SERIES 55470			SERIES 75470			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 7: For SN55470 and SN75470 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

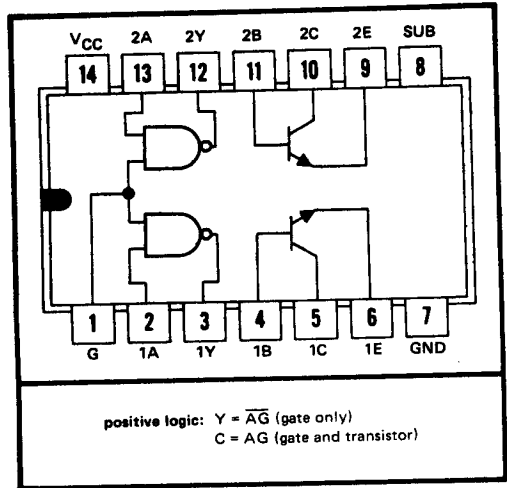
TYPES SN55470, SN75470 DUAL PERIPHERAL POSITIVE-AND DRIVERS

schematic



Resistor values shown are nominal.

SN55470...J
SN75470...J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER	TEST CONDITIONS†	SN55470			SN75470			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-1.2	-1.5		-1.2	-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = -400 μA	2.4	3.3		2.4	3.3		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I _I Input current at maximum input voltage	input A			1			1	mA
	input G			2			2	
I _{IH} High-level input current	input A			40			40	μA
	input G			80			80	
I _{IL} Low-level input current	input A			-1.6			-1.6	mA
	input G			-3.2			-3.2	
I _{QS} Short-circuit output current§	V _{CC} = MAX	-18	-35	-55	-18	-35	-55	mA
I _{CCH} Supply current, outputs high	V _{CC} = MAX, V _I = 0		2.8	4		2.8	4	mA
I _{CCL} Supply current, outputs low	V _{CC} = MAX, V _I = 5 V		7	11		7	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

TYPES SN55470, SN75470

DUAL PERIPHERAL POSITIVE-AND DRIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER	TEST CONDITIONS†	SN55470		SN75470		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V(BR)CBO	Collector-Base Breakdown Voltage $I_C = 100 \mu\text{A}$, $I_E = 0$	70			70		V
V(BR)CEO	Collector-Emitter Breakdown Voltage $I_C = 10 \text{ mA}$, $I_B = 0$, See Note 8	40			40		V
V(BR)CER	Collector-Emitter Breakdown Voltage $I_C = 100 \mu\text{A}$, $R_{BE} = 500 \Omega$	70			70		V
V(BR)EBO	Emitter-Base Breakdown Voltage $I_E = 100 \mu\text{A}$, $I_C = 0$	5			5		V
h _{FE}	Static Forward Current Transfer Ratio	$V_{CE} = 3 \text{ V}$, $I_C = 100 \text{ mA}$, $T_A = 25^\circ\text{C}$	See Note 8	25	25		
		$V_{CE} = 3 \text{ V}$, $I_C = 300 \text{ mA}$, $T_A = 25^\circ\text{C}$		30	30		
		$V_{CE} = 3 \text{ V}$, $I_C = 100 \text{ mA}$, $T_A = \text{MIN}$		10	20		
		$V_{CE} = 3 \text{ V}$, $I_C = 300 \text{ mA}$, $T_A = \text{MIN}$		15	25		
V _{BE}	Base-Emitter Voltage $I_B = 10 \text{ mA}$, $I_C = 100 \text{ mA}$	See Note 8	0.85	1.2	0.85	1	V
		$I_B = 30 \text{ mA}$, $I_C = 300 \text{ mA}$	1	1.4	1	1.2	
V _{CE(sat)}	Collector-Emitter Saturation Voltage $I_B = 10 \text{ mA}$, $I_C = 100 \text{ mA}$	See Note 8	0.25	0.5	0.25	0.4	V
		$I_B = 30 \text{ mA}$, $I_C = 300 \text{ mA}$	0.45	0.8	0.45	0.7	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 8: These parameters must be measured using pulse techniques. $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

TTL gates

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output $C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1		22		ns
t _{PHL}	Propagation delay time, high-to-low-level output		8		ns

output transistors

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t _d	Delay time $I_C = 200 \text{ mA}$, $I_B(1) = 20 \text{ mA}$, $I_B(2) = -40 \text{ mA}$		10		ns
t _r	Rise time $V_{BE(\text{off})} = -1 \text{ V}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$		16		ns
t _s	Storage time See Figure 2		23		ns
t _f	Fall time		14		ns

‡ Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output $I_C \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$	45	65		ns
t _{PHL}	Propagation delay time, high-to-low-level output $R_L = 50 \Omega$, See Figure 3	35	50		ns
t _{TLLH}	Transition time, low-to-high-level output	10	20		ns
t _{TTHL}	Transition time, high-to-low-level output	10	20		ns
V _{OH}	High-level output voltage after switching $V_S = 55 \text{ V}$, $I_C \approx 300 \text{ mA}$, $R_{BE} = 500 \Omega$, See Figure 4	$V_S - 18$			mV

TYPES SN55471, SN75471 DUAL PERIPHERAL POSITIVE-AND DRIVERS

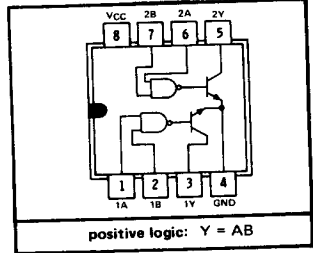
logic

FUNCTION TABLE
(EACH DRIVER)

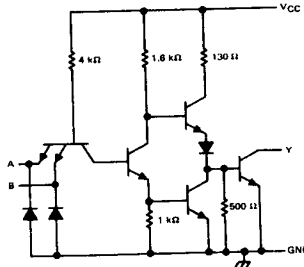
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

SN55471 . . . JG
SN75471 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55471		SN75471		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V_{IH} High-level input voltage		2		0.8		V	
V_{IL} Low-level input voltage				-1.2	-1.5	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.2	-1.5	V	
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{OH} = 70 \text{ V}$			300		μA	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 100 \text{ mA}$		0.25	0.5	0.25	0.4	V
	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OL} = 300 \text{ mA}$		0.5	0.8	0.5	0.7	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1		1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40		40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1	-1.6	-1	-1.6	mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}, V_I = 5 \text{ V}$		8	11	8	11	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}, V_I = 0$		56	76	56	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50 \Omega,$ See Figure 3		30	55	ns
t_{PHL} Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH} Transition time, low-to-high-level output			8	20	ns
t_{THL} Transition time, high-to-low-level output			10	20	ns
V_{OH} High-level output voltage after switching	$V_S = 55 \text{ V}, I_O \approx 300 \text{ mA},$ See Figure 4	$V_S - 18$			mV

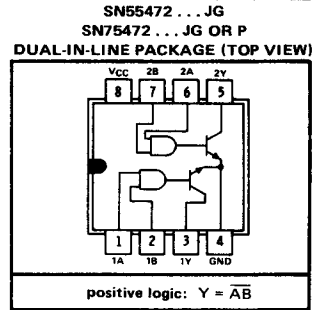
TYPES SN55472, SN75472 DUAL PERIPHERAL POSITIVE-NAND DRIVERS

logic

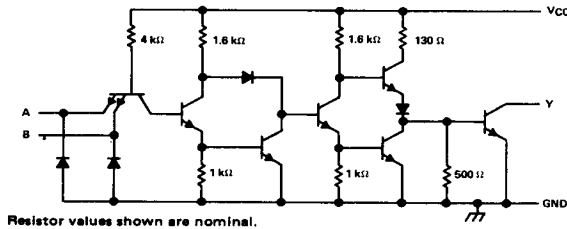
FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level



schematic (each driver)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN55472		SN75472		UNIT
		MIN	TYP†	MAX	MIN	
V_{IH} High-level input voltage		2		0.8		V
V_{IL} Low-level input voltage				0.8		V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2		-1.5		V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 70 \text{ V}$			300		μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 100 \text{ mA}$	0.25		0.5		V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 300 \text{ mA}$	0.5		0.8		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1		1 mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40		40 μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1.1		-1.6		-1.1 mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$	13		17		13 mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	61		76		61 mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 3		45	65	ns	
t_{PHL} Propagation delay time, high-to-low-level output			30	50	ns	
t_{TLH} Transition time, low-to-high-level output				13	25	ns
t_{THL} Transition time, high-to-low-level output				10	20	ns
V_{OH} High-level output voltage after switching	$V_S = 55 \text{ V}$, See Figure 4	$I_O \approx 300 \text{ mA}$, $V_S - 18$			mV	

TYPES SN55473, SN75473 DUAL PERIPHERAL POSITIVE-OR DRIVERS

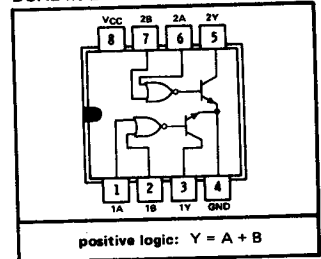
logic

**FUNCTION TABLE
(EACH DRIVER)**

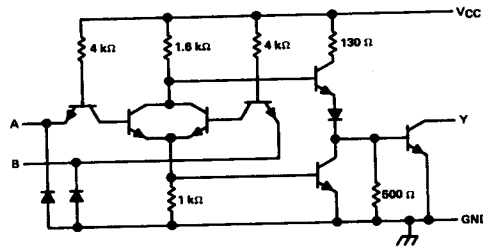
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

SN55473 ... JG
SN75473 ... JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55473			SN75473			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			2			V
V _{IL} Low-level input voltage				0.8			0.8	V
V _{IK} Input clamp voltage				-1.2 -1.5			-1.2 -1.5	V
I _{OH} High-level output current	V _{CC} = MIN, I _I = -12 mA V _{OH} = 70 V			300			100	μA
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 100 mA		0.25	0.5		0.25	0.4	V
	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 300 mA		0.5	0.8		0.5	0.7	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.4 V			40			40	μA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V		-1	-1.6		-1	-1.6	mA
I _{CCH} Supply current, outputs high	V _{CC} = MAX, V _I = 5 V		8	11		8	11	mA
I _{CCL} Supply current, outputs low	V _{CC} = MAX, V _I = 0		58	76		58	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{PLH} Propagation delay time, low-to-high-level output	I _O ≈ 200 mA, C _L = 15 pF, R _L = 50 Ω, See Figure 3		30	55	ns	
t _{PHL} Propagation delay time, high-to-low-level output			25	40	ns	
t _{TLH} Transition time, low-to-high-level output				8	25	ns
t _{THL} Transition time, high-to-low-level output				10	25	ns
V _{OH} High-level output voltage after switching	V _S = 55 V, I _O ≈ 300 mA, See Figure 4	V _S -18			mV	

TYPES SN55474, SN75474

DUAL PERIPHERAL POSITIVE-NOR DRIVERS

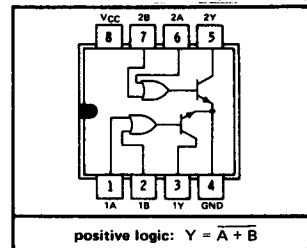
logic

FUNCTION TABLE
(EACH DRIVER)

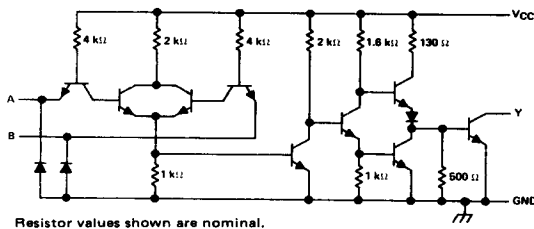
A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = High level, L = Low level

SN55474 ... JG
SN75474 ... JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55474			SN75474			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2		0.8	2		0.8	V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2		-1.5	-1.2		-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{OH} = 70 \text{ V}$, $V_{IL} = 0.8 \text{ V}$			300			100	μA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 100 \text{ mA}$		0.25	0.5		0.25	0.4	V
	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $I_{OL} = 300 \text{ mA}$		0.5	0.8		0.5	0.7	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1			-1	-1.6
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 0 \text{ V}$		14	19		14	19	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$		67	85		67	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

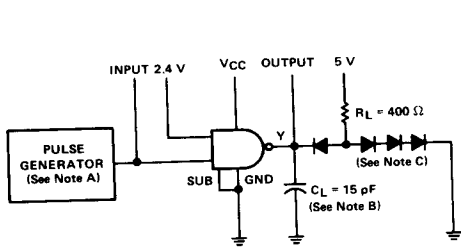
‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

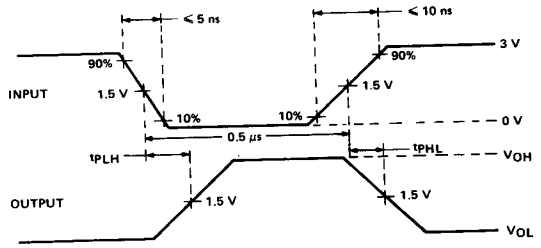
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 3		40	65	ns	
t_{PHL} Propagation delay time, high-to-low-level output			30	50	ns	
t_{TLH} Transition time, low-to-high-level output				8	20	ns
t_{THL} Transition time, high-to-low-level output				10	20	ns
V_{OH} High-level output voltage after switching	$V_S = 55 \text{ V}$, $I_O \approx 300 \text{ mA}$, See Figure 4	$V_S - 18$			mV	

SERIES 55470/75470 DUAL PERIPHERAL DRIVERS

PARAMETER MEASUREMENT INFORMATION



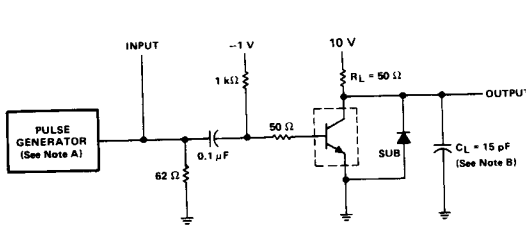
TEST CIRCUIT



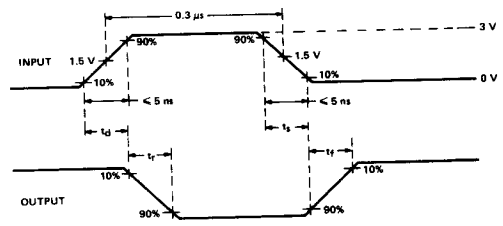
VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50 \Omega$.
 B. C_L include probe and jig capacitance.
 C. All diodes are 1N3064.

FIGURE 1—PROPAGATION DELAY TIMES, EACH GATE (SN55470 AND SN75470 ONLY)



TEST CIRCUIT



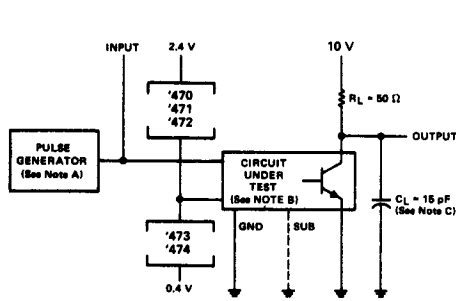
VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: duty cycle < 1%, $Z_{out} \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.

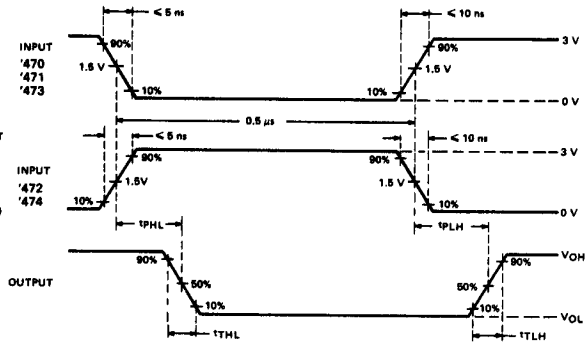
FIGURE 2—SWITCHING TIMES, EACH TRANSISTOR (SN55470 AND SN75470 ONLY)

SERIES 55470/75470 DUAL PERIPHERAL DRIVERS

PARAMETER MEASUREMENT INFORMATION



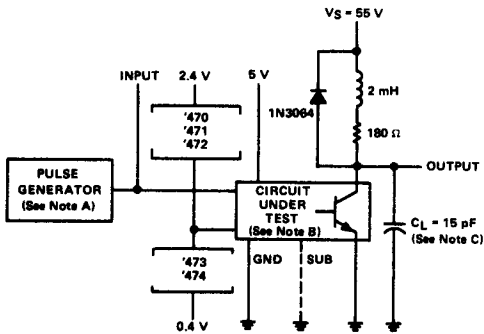
TEST CIRCUIT



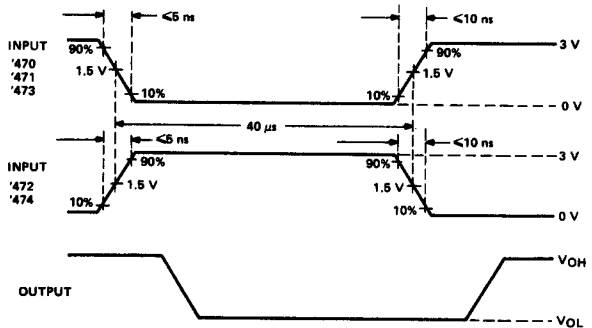
VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
 B. When testing SN55470 or SN75470, connect output Y to transistor base and ground the substrate terminal.
 C. C_L includes probe and jig capacitance.

FIGURE 3—SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{out} = 50\ \Omega$.
 B. When testing SN55470 or SN75470, connect output Y to transistor base with a 500- Ω resistor from there to ground, and ground the substrate terminal.
 C. C_L includes probe and jig capacitance.

FIGURE 4—LATCH-UP TEST OF COMPLETE DRIVERS