National Semiconductor

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# 74LVQ240
# Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

## General Description

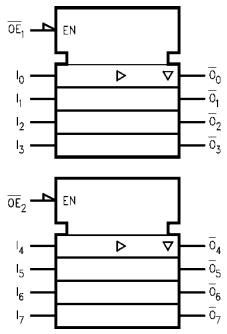
The LVQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

## Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

## Logic Symbol

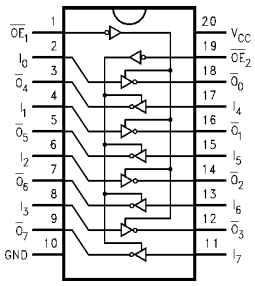
IEEE/IEC




TL/F/11611–1

## Connection Diagram

Pin Assignment, SOIC and QSOP




TL/F/11611–2

## Truth Tables

| Inputs | | Outputs (Pins 12, 14, 16, 18) |
|---|---|---|
| $\overline{OE}_1$ | $I_n$ | |
| L | L | H |
| L | H | L |
| H | X | Z |

| Inputs | | Outputs (Pins 3, 5, 7, 9) |
|---|---|---|
| $\overline{OE}_2$ | $I_n$ | |
| L | L | H |
| L | H | L |
| H | X | Z |

H = HIGH Voltage Level  X = Immaterial
L = LOW Voltage Level  Z = High Impedance

| Pin Names | Description |
|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$ | TRI-STATE Output Enable Inputs |
| $I_0$–$I_7$ | Inputs |
| $\overline{O}_0$–$\overline{O}_7$ | Outputs |

| | SOIC JEDEC | SOIC EIAJ | SSOP JEDEC |
|---|---|---|---|
| Order Number | 74LVQ240SC<br>74LVQ240SCX | 74LVQ240SJ<br>74LVQ240SJX | 74LVQ240QSC<br>74LVQ240QSCX |
| See NS Package Number | M20B | M20D | MQA20 |

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## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| $V_I$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source or Sink Current ($I_O$) | ±50 mA |
| DC $V_{CC}$ or Ground Current ($I_{CC}$ or $I_{GND}$) | ±400 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| DC Latch-Up Source or Sink Current | ±300 mA |

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation*.

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| LVQ | 2.0V to 3.6V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | |
| 74LVQ | −40°C to +85°C |
| Minimum Input Edge Rate ΔV/Δt | |
| $V_{IN}$ 0.8V to 2.0V | |
| $V_{CC}$ @ 3.0V | 125 mV/ns |

## DC Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | 74LVQ240 | | 74LVQ240 | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C | | $T_A$ = −40°C to +85°C | | |
| | | | Typ | Guaranteed Limits | | | |
| $V_{IH}$ | Minimum High Level Input Voltage | 3.0 | 1.5 | 2.0 | 2.0 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{IL}$ | Maximum Low Level Input Voltage | 3.0 | 1.5 | 0.8 | 0.8 | V | $V_{OUT}$ = 0.1V or $V_{CC}$ − 0.1V |
| $V_{OH}$ | Minimum High Level Output Voltage | 3.0 | 2.99 | 2.9 | 2.9 | V | $I_{OUT}$ = −50 μA |
| | | 3.0 | | 2.58 | 2.48 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ $I_{OH}$ = −12 mA |
| $V_{OL}$ | Maximum Low Level Output Voltage | 3.0 | 0.002 | 0.1 | 0.1 | V | $I_{OUT}$ = 50 μA |
| | | 3.0 | | 0.36 | 0.44 | V | *$V_{IN}$ = $V_{IL}$ or $V_{IH}$ $I_{OL}$ = 12 mA |
| $I_{IN}$ | Maximum Input Leakage Current | 3.6 | | ±0.1 | ±1.0 | μA | $V_I$ = $V_{CC}$, GND |

*All outputs loaded; thresholds on input associated with output under test.

## DC Characteristics (Continued)

| Symbol | Parameter | $V_{CC}$ (V) | 74LVQ240 $T_A = +25°C$ | | 74LVQ240 $T_A = -40°C$ to $+85°C$ | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Typ | Guaranteed Limits | | | |
| $I_{OLD}$ | †Minimum Dynamic Output Current | 3.6 | | | 36 | mA | $V_{OLD}$ = 0.8V Max (Note 1) |
| $I_{OHD}$ | | 3.6 | | | −25 | mA | $V_{OHD}$ = 2.0V Min (Note 1) |
| $I_{CC}$ | Maximum Quiescent Supply Current | 3.6 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND |
| $I_{OZ}$ | Maximum TRI-STATE Leakage Current | 3.6 | | ±0.25 | ±2.5 | μA | $V_I$(OE) = $V_{IL}$, $V_{IH}$<br>$V_I = V_{CC}$, GND<br>$V_O = V_{CC}$, GND |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | 0.4 | 0.8 | | V | (Notes 2, 3) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | −0.4 | −0.8 | | V | (Notes 2, 3) |
| $V_{IHD}$ | Maximum High Level Dynamic Input Voltage | 3.3 | 1.6 | 2.0 | | V | (Notes 2, 4) |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | 3.3 | 1.6 | 0.8 | | V | (Notes 2, 4) |

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note 1:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 2:** Worst case package.

**Note 3:** Max number of outputs defined as (n). Data Inputs are driven 0V to 3.3V. One output @ GND.

**Note 4:** Max number of Data Inputs (n) switching. n−1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f = 1 MHz.

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | 74LVQ240 $T_A = +25°C$, $C_L = 50$ pF | | | 74LVQ240 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PHL}$, $t_{PLH}$ | Propagation Delay Data to Output | 2.7<br>3.3 ±0.3 | 2.0<br>2.0 | 8.4<br>7.0 | 14.0<br>10.0 | 2.0<br>2.0 | 15.0<br>10.5 | ns |
| $t_{PZL}$, $t_{PZH}$ | Output Enable Time | 2.7<br>3.3±0.3 | 2.5<br>2.5 | 9.6<br>8.0 | 16.9<br>12.0 | 2.5<br>2.5 | 18.0<br>12.5 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time | 2.7<br>3.3 ±0.3 | 1.0<br>1.0 | 10.2<br>8.5 | 19.0<br>13.5 | 1.0<br>1.0 | 20.0<br>14.0 | ns |
| $t_{OSHL}$, $t_{OSLH}$ | Output to Output Skew *Data to Output | 2.7<br>3.3 ±0.3 | | 1.0<br>1.0 | 1.5<br>1.5 | | 1.5<br>1.5 | ns |

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ($t_{OSHL}$) or LOW to HIGH ($t_{OSLH}$). Parameter guaranteed by design.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = Open |
| $C_{PD}$ (Note 1) | Power Dissipation Capacitance | 70 | pF | $V_{CC}$ = 3.3V |

**Note 1:** $C_{PD}$ is measured at 10 MHz.

## 74LVQ240 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74LVQ 240 S C X

Temperature Range Family
74LVQ = Commercial

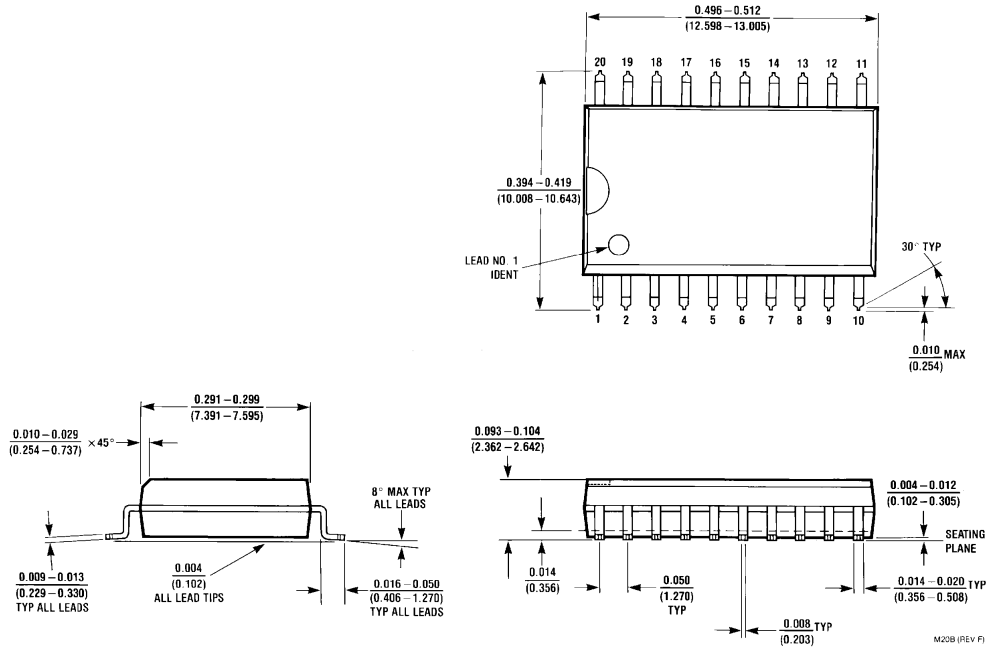
Device Type

Package Code
S = (0.300″ Wide) Molded Small Outline Package, JEDEC
SJ = (0.300″ Wide) Molded Small Outline Package, EIAJ
QS = Shrink Small Outline Package, JEDEC
(also known as QSOP)

Special Variations
"X" = Tape and Reel
" " = Rail/Tube

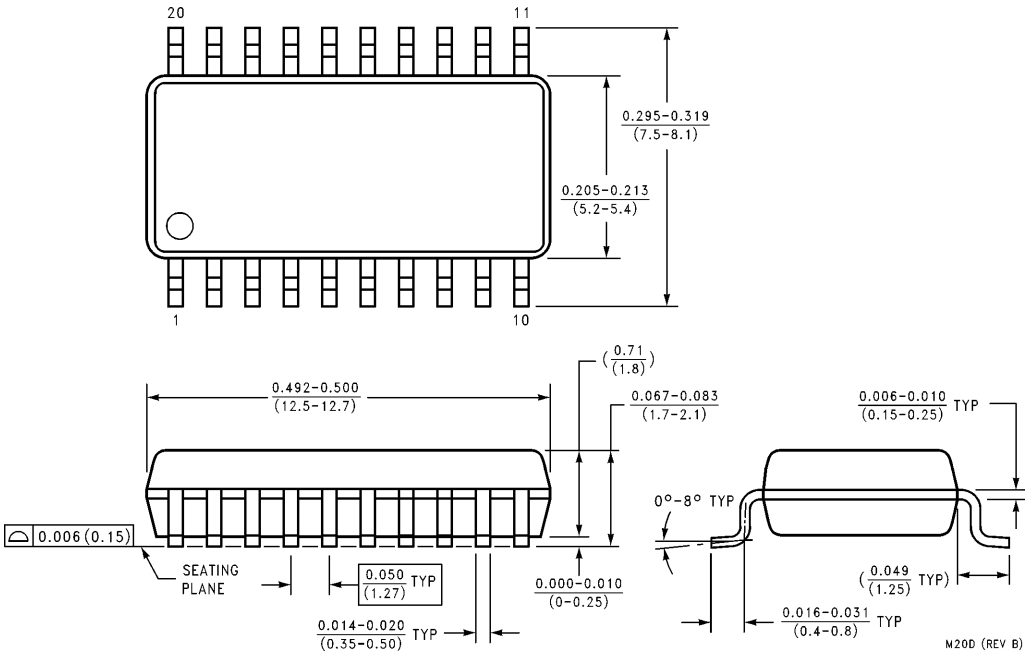
Temperature Range
C = Commercial (−40°C to +85°C)

## Physical Dimensions inches (millimeters) unless otherwise noted



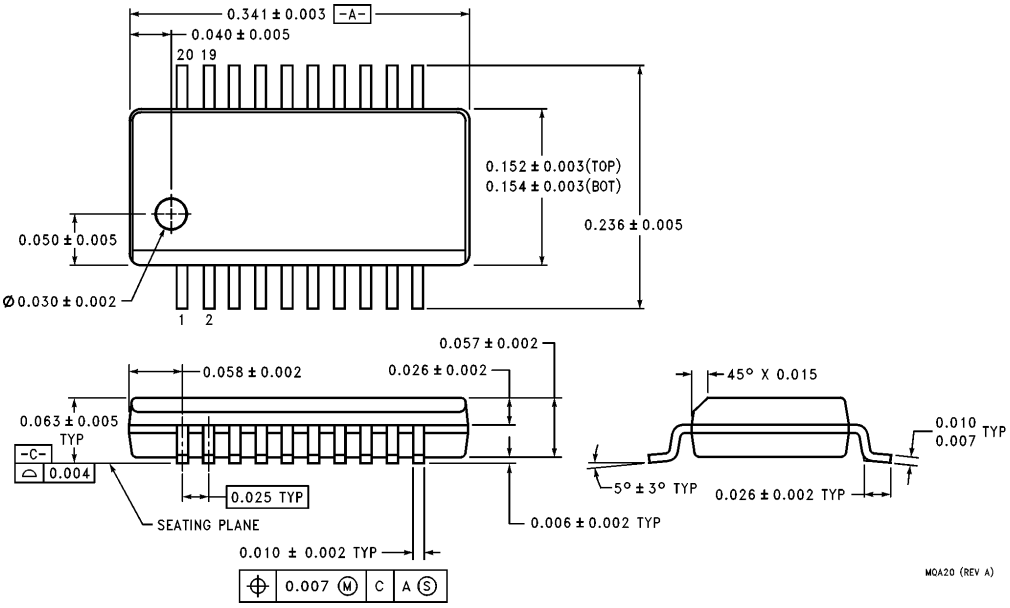

**20-Lead Small Outline Integrated Circuit (S)**
**Order Number 74LVQ240SC or 74LVQ240SCX**
**NS Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Small Outline Package EIAJ SOIC (SJ)**
**Order Number 74LVQ240SJ or 74LVQ240SJX**
**NS Package Number M20D**

## Physical Dimensions inches (Continued)




**20-Lead (0.150″ Wide) Shrink Small Outline Package, JEDEC**
**(also known as QSOP)**
**Order Number 74LVQ240QSC or 74LVQ240QSCX**
**NS Package Number MQA20**

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