TC74LVQ157F/FN/FS

Quad 2 - Channel Multiplexer

The TC74LVQ157 is a high speed CMOS MULTIPLEXER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and strobe inputs.

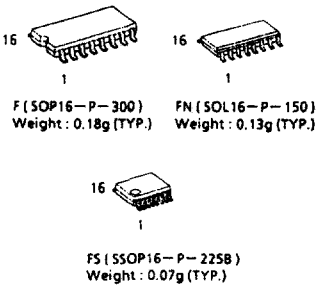
When the $\overline{\text{STROBE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

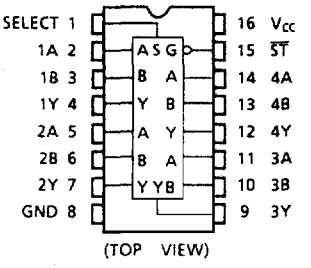
- High Speed: t_{pd} = 5.6ns (Typ.) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4μA (Max.) at Ta = 25°C
- Input Voltage Level:
  - V_{IL} = 0.8V (Max.) at V_{CC} = 3V
  - V_{IH} = 2.0V (Min.) at V_{CC} = 3V
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 12mA (Min.)
- Balanced Propagation Delays: $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74HC157



F (SOP16-P-300)
Weight : 0.18g (TYP.)

FN (SOL16-P-150)
Weight : 0.13g (TYP.)

FS (SSOP16-P-225B)
Weight : 0.07g (TYP.)

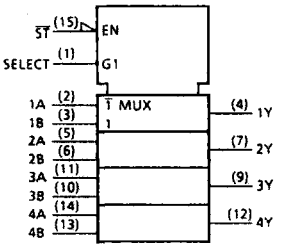


Pin Assignment

Truth Table

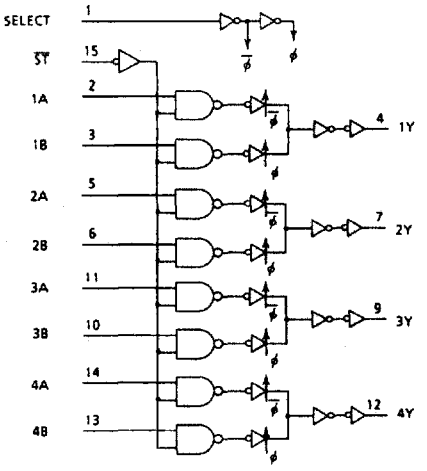
Inputs				Outputs
$\overline{\text{ST}}$	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X: Don't Care



IEC Logic Symbol

System Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7.0	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2.0 ~ 3.6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	dt/dv	0 ~ 100	ns/V

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IN}	–		3.0	2.0	–	–	2.0	–	V
Low-Level Input Voltage	V_{IL}	–		3.0	–	–	0.8	–	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	3.0	2.9	3.0	–	2.9	–	V
			I_{OH} = -12mA	3.0	2.58	–	–	2.48	–	V
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	3.0	–	0.0	0.1	–	0.1	V
			I_{OL} = 12mA	3.0	–	–	0.36	–	0.44	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		3.6	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		3.6	–	–	4.0	–	40.0	μA

AC Electrical Characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max.	Min.	Max.	
Propagation Delay Time (A, B-Y)	t_{pLH} t_{pHL}		2.7 3.3±0.3	– –	7.8 6.5	12.7 9.0	1.0 1.0	15.0 10.0	ns
Propagation Delay Time (SELECT-Y)	t_{pLH} t_{pHL}		2.7 3.3±0.3	– –	8.9 7.4	17.3 12.3	1.0 1.0	20.0 14.0	
Propagation Delay Time ($\overline{ST}$ - Y)	t_{pLH} t_{pHL}		2.7 3.3±0.3	– –	8.9 7.4	17.3 12.3	1.0 1.0	20.0 14.0	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7 3.3±0.3	– –	– –	1.5 1.5	– –	1.5 1.5	
Input Capacitance	C_{IN}	(Note 2)		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)		–	41	–	–	–	

Note (1) Parameter guaranteed by design. $t_{osLH} = | t_{pLHm} - t_{pLHn} |$, $t_{osHL} = | t_{pHLm} - t_{pHLn} |$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption. Average operating current can be obtained by the equation:

$I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per bit)

And the total C_{PD} when n pcs. of Bit operate can be gained by the following equation:

$C_{PD}(total) = 13 + 7 \bullet n$

Noise Characteristics (Input $t_r = t_f = 3ns$, $C_L = 50pF$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition	Ta = 25°C		Unit
		V_{CC}	Typ.	Max.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	3.3	0.3	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	3.3	-0.3	-0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	3.3	–	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	3.3	–	0.8	V