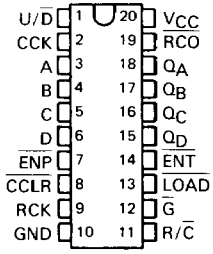
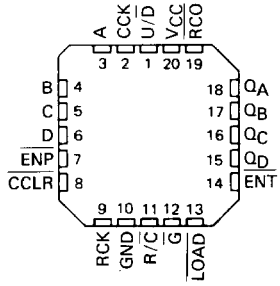
- **4-Bit Counters/Registers**
- **Multiplexed Outputs for Counter or Latched Data**
- **3-State Outputs Drive Bus Lines Directly**
- **'LS696 . . Decade Counter, Direct Clear**
  'LS697 . . Binary Counter, Direct Clear
  'LS698 . . Decade Counter, Synchronous Clear
  'LS699 . . Binary Counter, Synchronous Clear

SN54LS696 THRU SN54LS699 . . . J PACKAGE
SN74LS696 THRU SN74LS699 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS696 THRU SN54LS699 . . . FK PACKAGE
SN74LS696 THRU SN74LS699 . . . FN PACKAGE
(TOP VIEW)



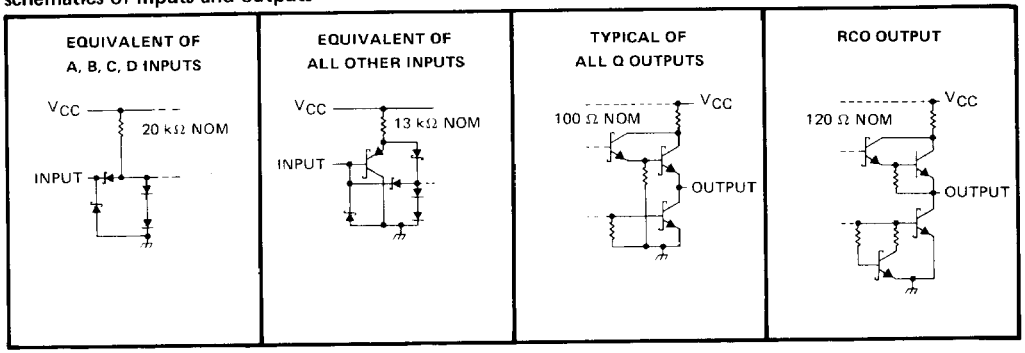
description

These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three state outputs in a single 20-pin package. The up/down counters are programmable from the data inputs and feature enable $\overline{P}$ and enable $\overline{T}$ and a ripple-carry output for easy expansion. The register/counter select input $R/\overline{C}$, selects the counter when low and the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus driving performance.

Both the counter clock CCK and register clock $\overline{RCK}$ are positive-edge triggered. The counter clear $\overline{CCLR}$ is active low and is a synchronous on the 'LS696 and 'LS697, synchronous on the 'LS698 and 'LS699. Loading of the counter is accomplished when $\overline{LOAD}$ is taken low and a positive transition occurs on the counter clock CCK.

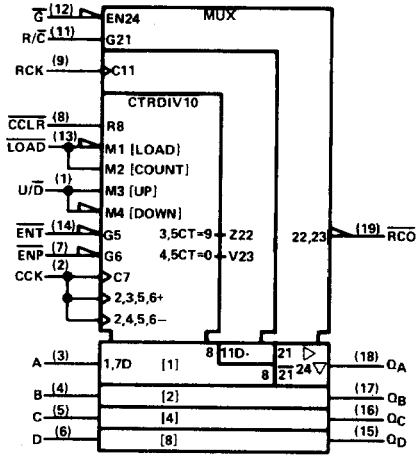
Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to $\overline{ENT}$ of the second stage, etc. All $\overline{ENP}$ inputs can be tied common and used as a master enable or disable control.

schematics of inputs and outputs

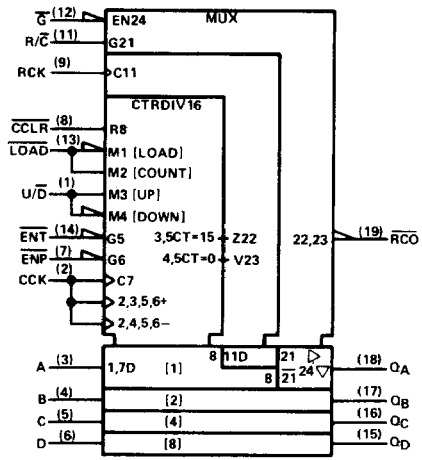


logic symbols

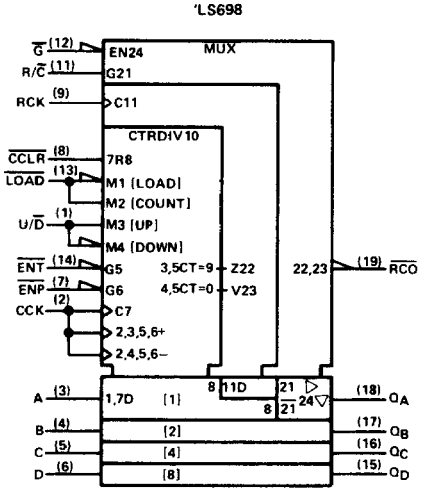
'LS696



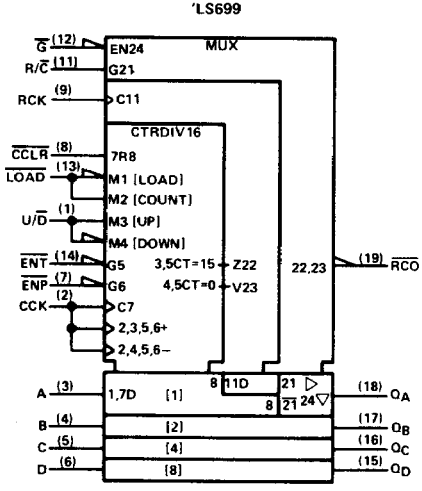
'LS697



'LS698



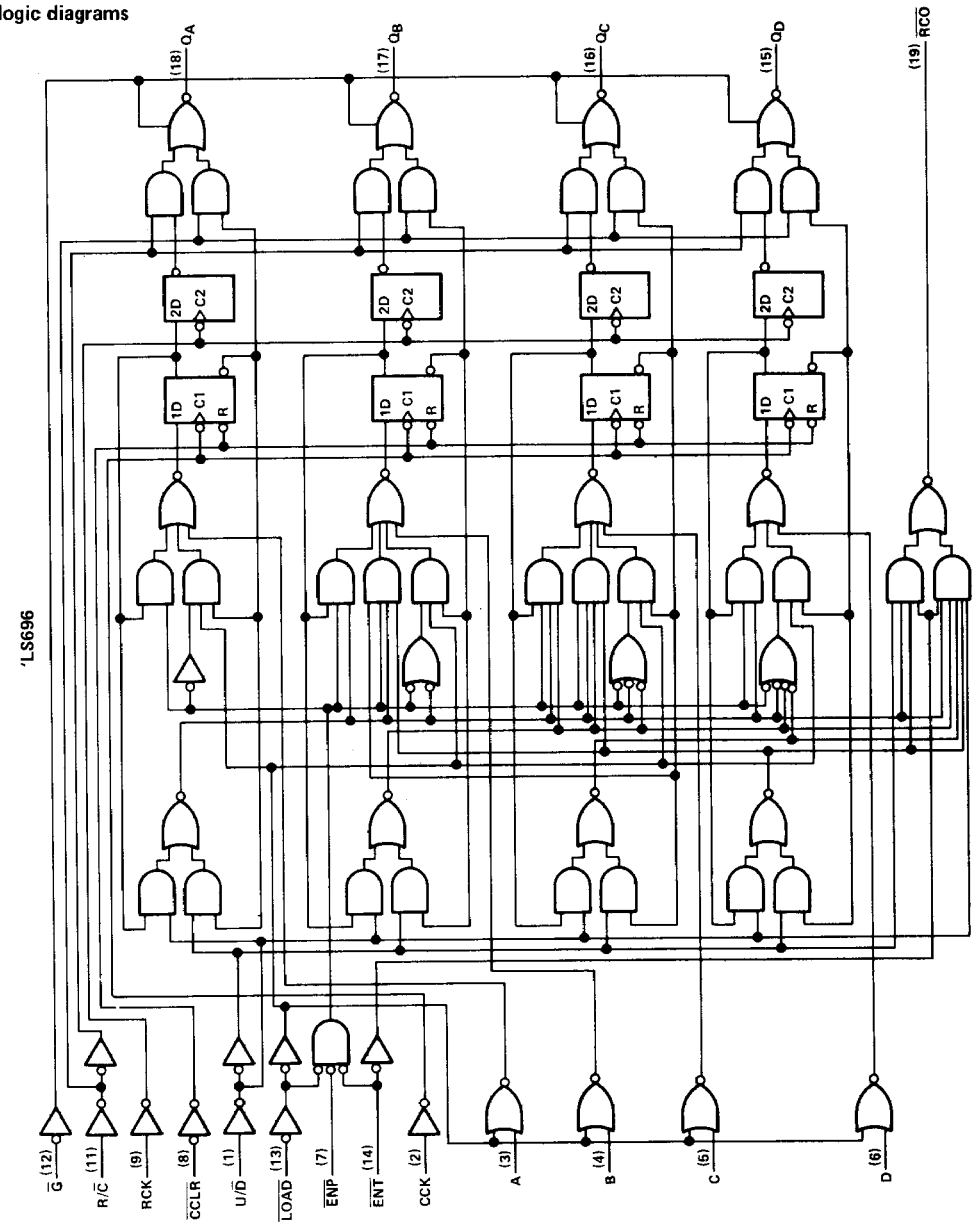
'LS699



Pin numbers shown on logic notation are for DW, J or N packages.

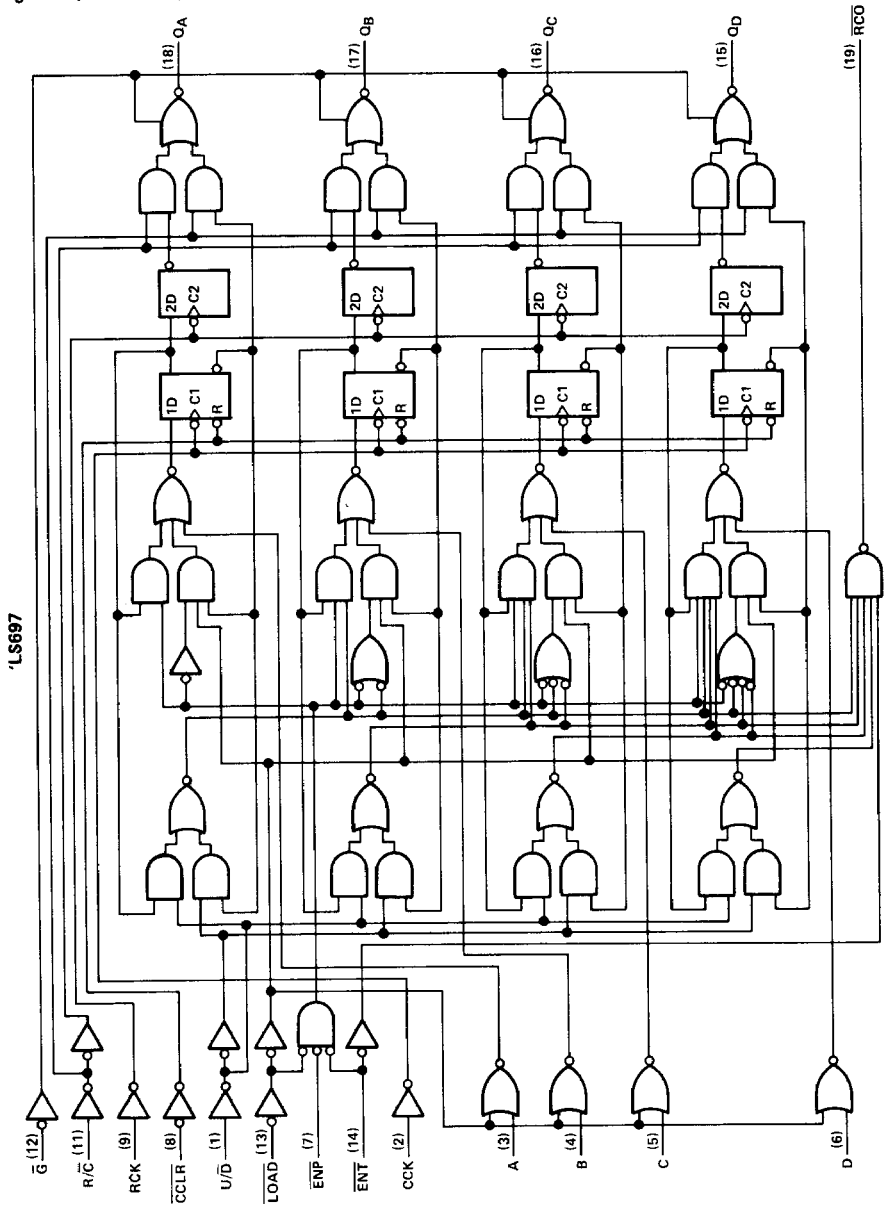
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagrams



Pin numbers shown on logic notation are for DW, J or N packages.

logic diagrams (continued)

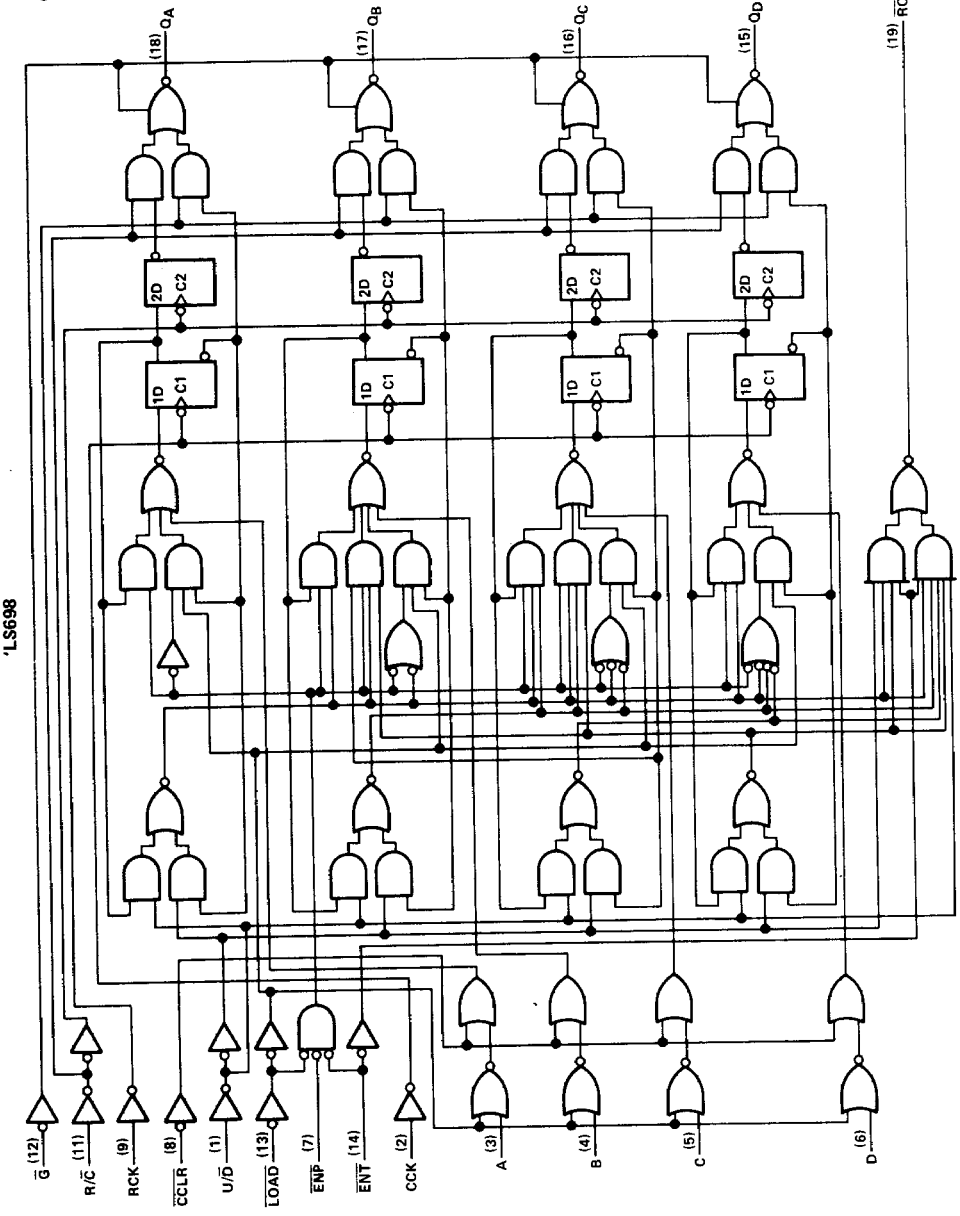


Pin numbers shown on logic notation are for DW, J or N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

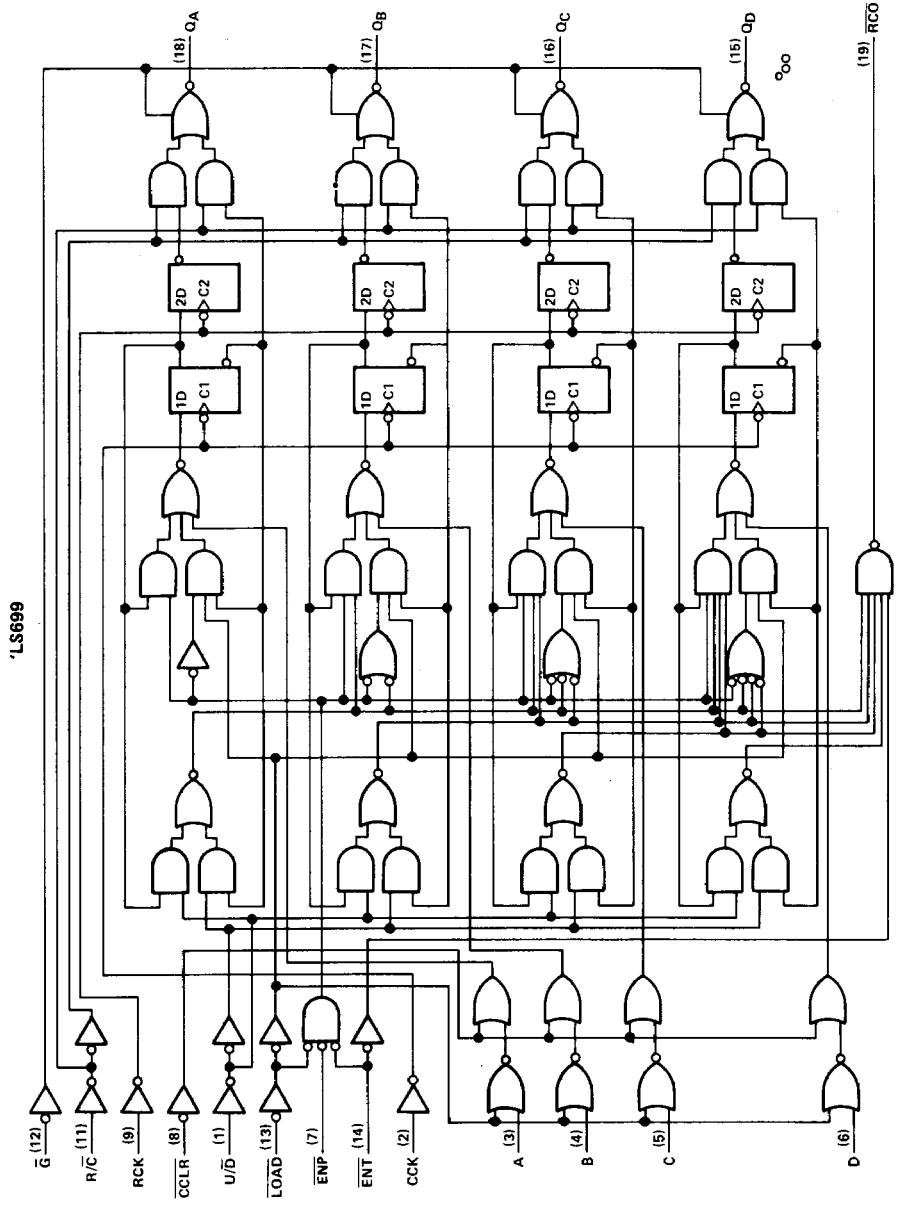
logic diagrams (continued)

'LS698



Pin numbers shown on logic notation are for DW, J or N packages.

logic diagrams (continued)



Pin numbers shown on logic notation are for DW, J or N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS696 thru SN54LS699 . . . . . −55°C to 125°C
SN74LS696 thru SN74LS699 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current	Q			−1			−2.6	mA
		$\overline{RCO}$			−0.4			−0.4	
I_{OL}	Low-level output current	Q			12			24	mA
		$\overline{RCO}$			4			8	
f_{clock}	Clock frequency	CCK	0		20	0		20	MHz
		RCK	0		20	0		20	
t_w	Pulse duration	CCK high or low	25			25			ns
		RCK high or low	25			25			
		'LS696, 'LS697 $\overline{CCLR}$ low	20			20			
t_{su}	Setup time before CCK ↑	A thru D	30			30			ns
		$\overline{ENP}$ or $\overline{ENT}$	30			30			
		$\overline{LOAD}$	30			30			
		U/$\overline{D}$	35			35			
		'LS696, 'LS697, $\overline{CCLR}$ inactive	25			25			
		'LS698, 'LS699, $\overline{CCLR}$	30			30			
t_{su}	Setup time CCK ↑ before RCK ↑ (see Note 2)		30			30			ns
t_h	Hold time		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.1					V
		Any Q		I_{OH}=−2.6 mA				2.4	3.1		
		$\overline{RCO}$		I_{OH}=−400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
		Any Q		I_{OL}=24 mA					0.35	0.5	
		$\overline{RCO}$		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
		$\overline{RCO}$		I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V, V_O=2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V, V_O=0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current	A thru D	V_{CC}=MAX, V_I=0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	Any Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high		V_{CC}=MAX, All outputs open	See Note 3		46	65		46	65	mA
I_{CCL}	Supply current, outputs low			See Note 4		48	70		48	70	
I_{CCZ}	Supply current, outputs off			See Note 5		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CCH} is measured after two 4.5 V to 0 V to 4.5 V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.
4. I_{CCL} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while all other inputs are grounded.
5. I_{CCZ} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

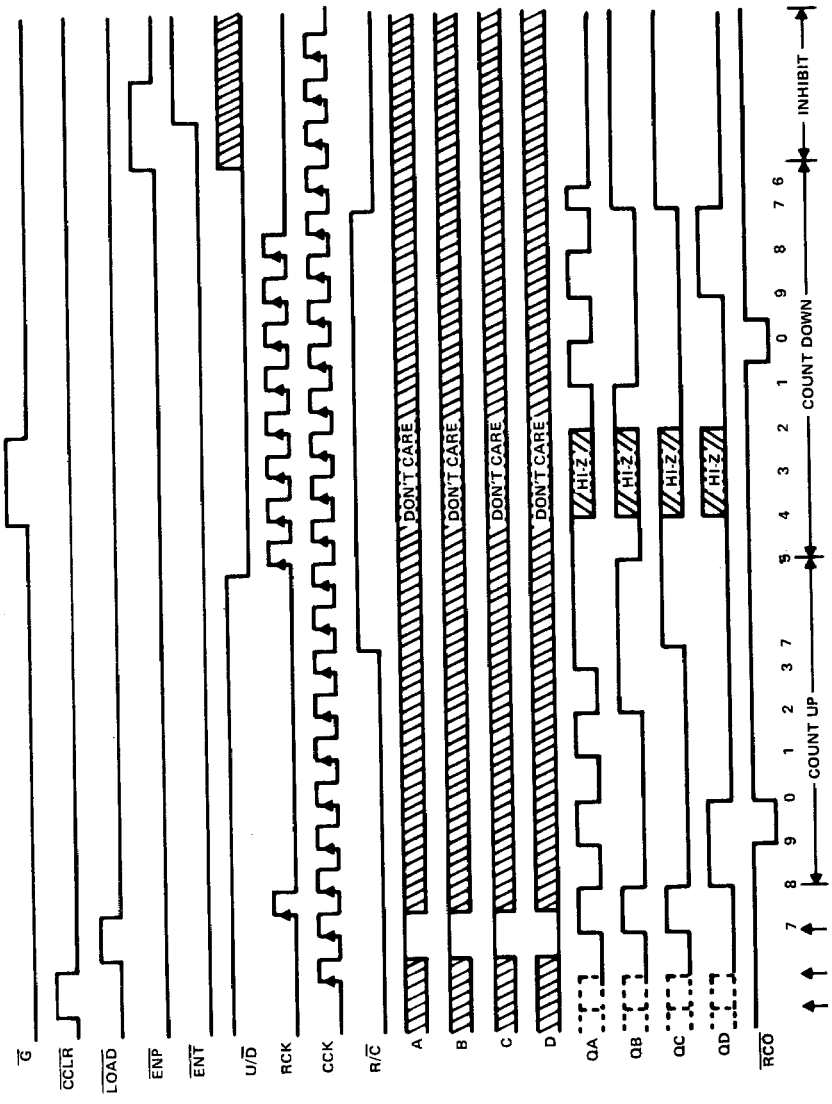
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS696, 'LS697 MIN	'LS696, 'LS697 TYP	'LS696, 'LS697 MAX	'LS698, 'LS699 MIN	'LS698, 'LS699 TYP	'LS698, 'LS699 MAX	UNIT
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	ns
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			13	20		13	20	ns
t_{PHL}					13	20		13	20	ns
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	ns
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	ns

NOTE 6: See General Information Section for load circuits and voltage waveforms.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

typical operating sequences

'LS696 DECADE COUNTER, Asynchronous Clear
'LS698 DECADE COUNTER, Synchronous Clear



typical operating sequences (continued)

'LS697 BINARY COUNTER, Asynchronous Clear
'LS699 BINARY COUNTER, Synchronous Clear