Signetics

74LS568A, 569A
3-State Bidirectional Counters

'568A BCD Decade Up/Down Synchronous Counter (3-State)
'569A 4-Bit Binary Up/Down Synchronous Counter (3-State)
Product Specification

Logic Products

FEATURES
- **Speed improved over LS568/ LS569**
- **Synchronous counting and loading**
- **UP/DOWN counting**
- **BCD decade counter – '568A**
- **Modulo 16 binary counter – '569A**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous Master Reset**
- **3-State Counter outputs**
- **Gated Carry output**

DESCRIPTION
The '568A and '569A are synchronous presettable UP/DOWN counters featuring an internal carry look-ahead for applications in high speed counting designs.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count-Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the Clock.

TYPE	TYPICAL f_{Max}	TYPICAL SUPPLY CURRENT (TOTAL)
74LS568A	35MHz	28mA
74LS569A	35MHz	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74LS568AN, N74LS569AN

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74LS
All	Inputs	1LSul
$Q_0 - Q_3$	Outputs	30LSul
$\overline{TC}$, GC	Outputs	10LSul

NOTE:
A 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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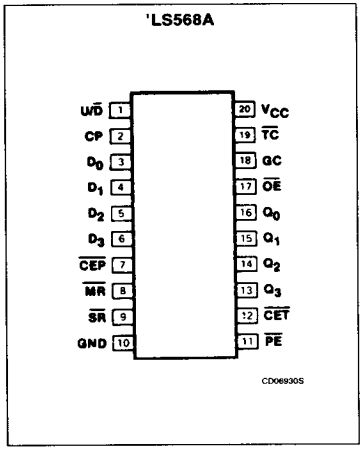
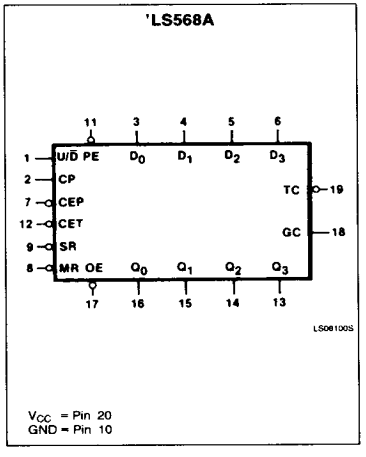
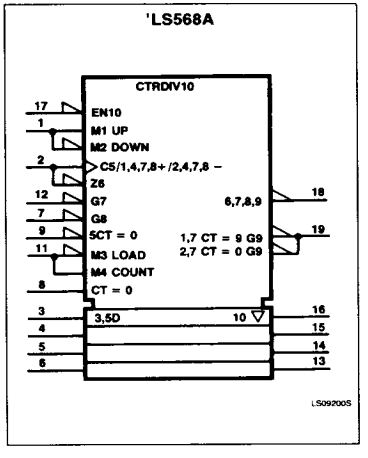
PIN CONFIGURATION



LOGIC SYMBOL



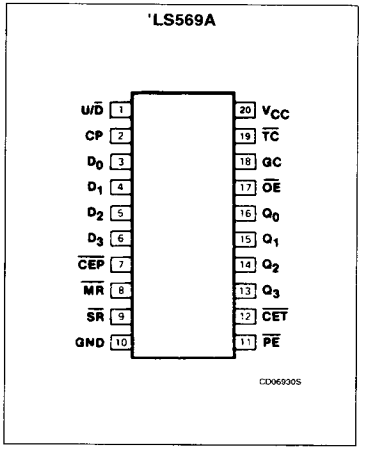
LOGIC SYMBOL (IEEE/IEC)



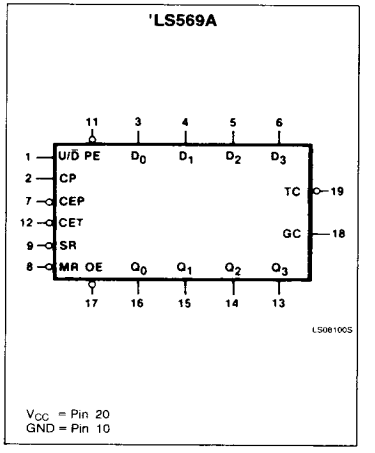
3-State Bidirectional Counters

74LS568A, 569A

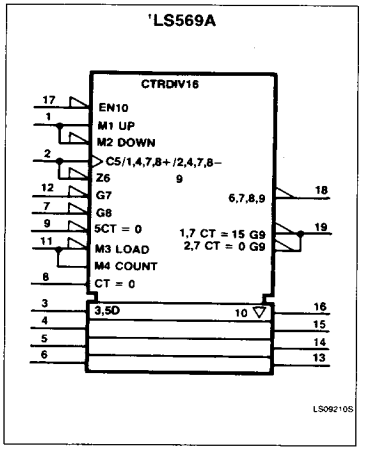
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the Clock, and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the Clock. The Synchronous Reset ($\overline{SR}$), when LOW one set-up time before the LOW-to-HIGH transition of the Clock, overrides the $\overline{CEP}$, $\overline{CET}$ and $\overline{PE}$ inputs, and causes the flip-flops to go LOW coincident with the positive Clock transition.

The Master Reset ($\overline{MR}$) is an asynchronous overriding clear function which forces all stages to a LOW state while the $\overline{MR}$ input is LOW without regard to the Clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$·$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure A in '168/'169 data sheet for the fast synchronous multistage counting connections.

The Gated Clock output (GC) is a Terminal Count output which provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the Clock pulse when $\overline{TC}$ is LOW. The GC output can be used as a Clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the UP/DOWN (U/$\overline{D}$) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The active LOW Output Enable ($\overline{OE}$) input controls the 3-State buffer outputs independent of the counter operation. When $\overline{OE}$ is LOW, the count appears at the buffer outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT — FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	$\overline{MR}$	CP	$\overline{SR}$	U/$\overline{D}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	D_n	Q_0	Q_1	Q_2	Q_3
Asynchronous reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous reset	H	↑	l	X	X	X	X	X	L	L	L	L
Parallel load	H	↑	h	X	l	X	X	l	L	L	L	L
	H	↑	h	X	l	X	X	h	H	H	H	H
Count up	H	↑	h	h	h	l	l	X	count up			
Count down	H	↑	h	l	h	l	l	X	count down			
Hold (do nothing)	H	↑	h	X	h	h	X	X	no change			
	H	↑	h	X	h	X	h	X	no change			

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	$\overline{OE}$	Q_n-Counter	Q_0, Q_1, Q_2, Q_3
Read counter	L	L	L
	L	H	H
Disable outputs	H	L	(Z)
	H	H	(Z)

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TERMINAL COUNT FUNCTION TABLE, '568A

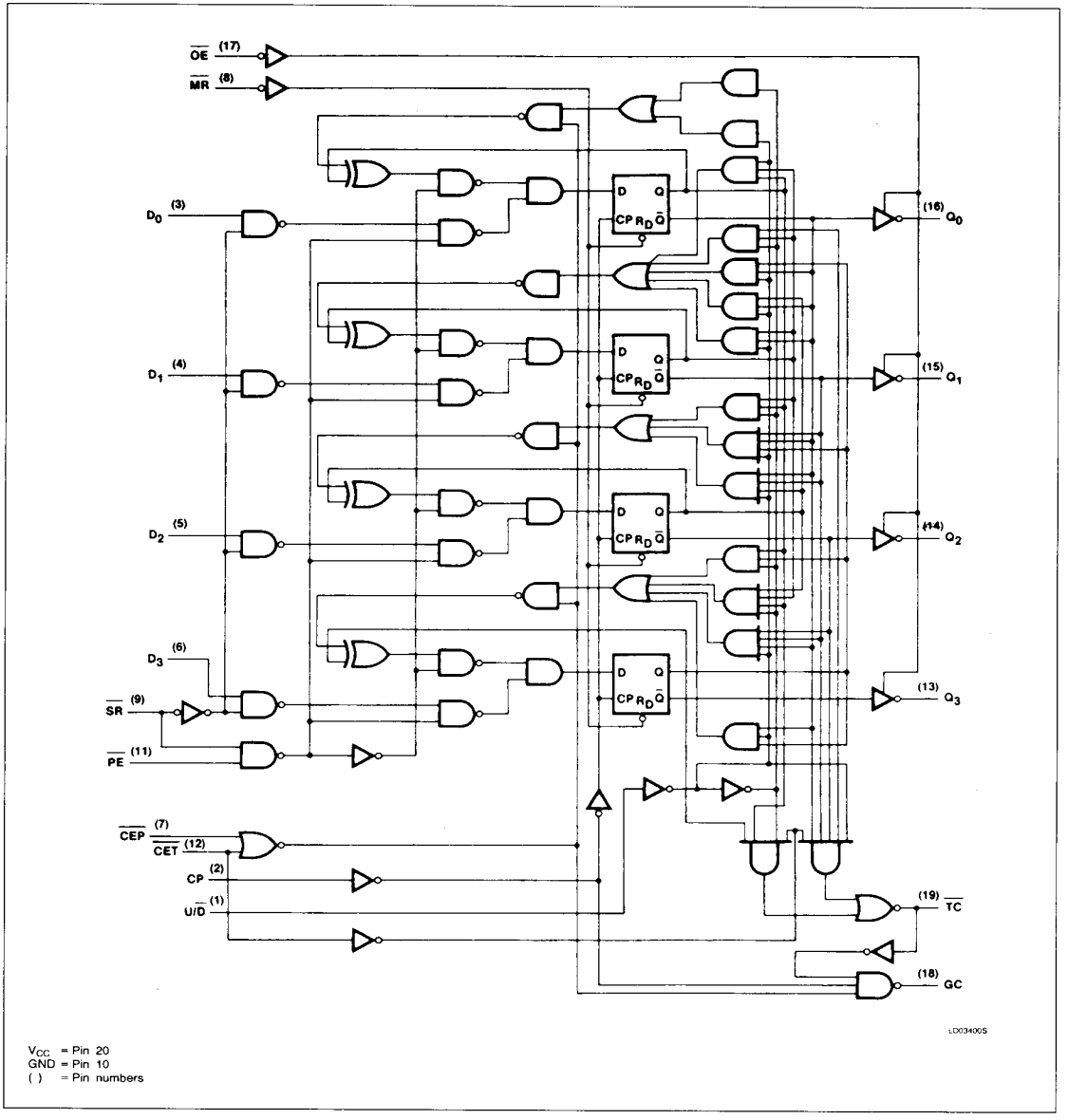
INPUTS				COUNTER STATES				OUTPUTS	
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	X	X	H	L	H
L	H	L	L	H	X	X	H	L	L
X	H	H	L	H	X	X	H	L	H
X	H	X	H	H	X	X	H	H	H

TERMINAL COUNT FUNCTION TABLE, '569A

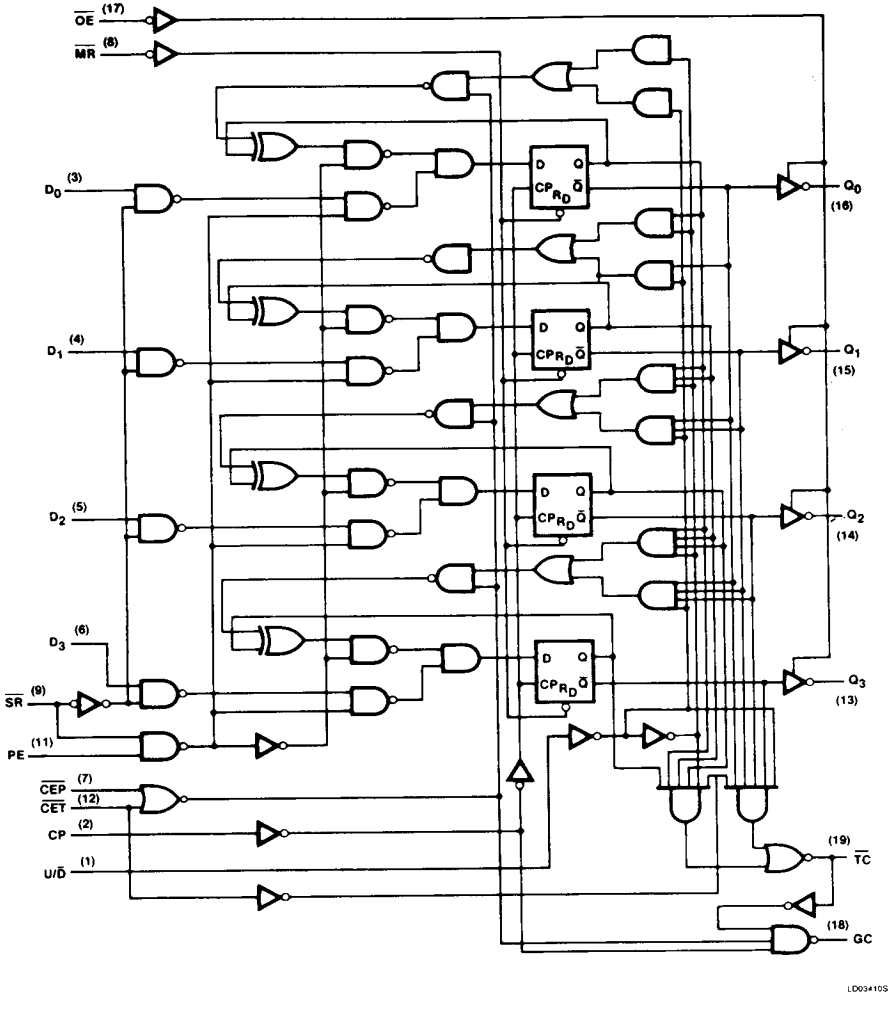
INPUTS				COUNTER STATES				OUTPUTS	
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	L	L
X	H	H	L	H	H	H	H	L	H
X	H	X	H	H	H	H	H	H	H

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
X = Don't care
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM, '568A



LOGIC DIAGRAM, '569A



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	74LS	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	$Q_0 - Q_3$			−2.6	mA
		$\overline{TC}$,GC			−400	μA
I_{OL}	LOW-level output current	$Q_0 - Q_3$			24	mA
		$\overline{TC}$, GC			8	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			74LS568, 569			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	$Q_0 - Q_3$	I_{OH} = MAX	2.4			V
			$\overline{TC}$, GC	I_{OH} = MAX	2.4			V
	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	$Q_0 - Q_3$	I_{OL} = MAX			0.5	V
				I_{OL} = 12mA (74LS)			0.5	V
			$\overline{TC}$, GC	I_{OL} = MAX			0.5	V
				I_{OL} = 4mA (74LS)			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.7V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V					−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	$Q_0 - Q_3$		−30		−100	mA
			$\overline{TC}$, GC		−15		−100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				28	43	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX +0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

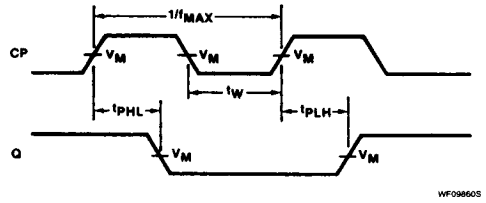
PARAMETER		TEST CONDITIONS	74LS $C_L = 45pF$, $R_L = 667\Omega$		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		15 20	ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{TC}$	Waveform 2		20 25	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3		14 15	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ control to $\overline{TC}$	Waveform 4		20 25	ns
t_{PLH} t_{PHL}	Propagation delay Clock to GC	Waveform 2		15 17	ns
t_{PLH} t_{PHL}	CET or CEP to GC	Waveform 2		16 26	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 5		20	ns
t_{PZH}	Output enable to HIGH level	Waveform 6		15	ns
t_{PZL}	Output enable to LOW level	Waveform 7		15	ns
t_{PHZ}	Output disable from HIGH level	Waveform 6, $C_L = 5pF$		20	ns
t_{PLZ}	Output disable from LOW level	Waveform 7, $C_L = 5pF$		22	ns

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

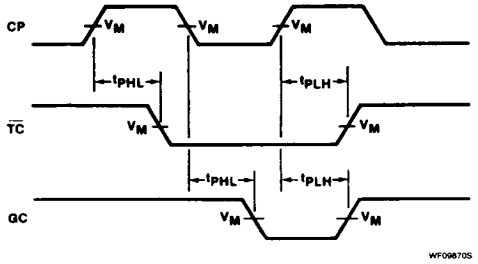
PARAMETER		TEST CONDITIONS	74LS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_S	Set-up time data to clock	Waveform 8	20		ns
t_h	Hold time data to clock	Waveform 8	0		ns
t_S	Set-up time $\overline{PE}$ to clock	Waveform 8	25		ns
t_h	Hold time $\overline{PE}$ to clock	Waveform 8	0		ns
t_S	Set-up time $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 9	20		ns
t_h	Hold time $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 9	0		ns
t_S	Set-up time U/$\overline{D}$ to clock	Waveform 10	30		ns
t_h	Hold time U/$\overline{D}$ to clock	Waveform 10	0		ns
t_S	Set-up time $\overline{SR}$ to clock	Waveform 11	30		ns
t_h	Hold time $\overline{SR}$ to clock	Waveform 11	0		ns
t_{rec}	Recovery time $\overline{MR}$ to clock	Waveform 5	20		ns

AC WAVEFORMS



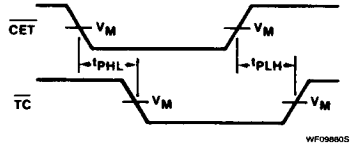
V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.

Waveform 1. Clock To Output Delays And Clock Pulse Width



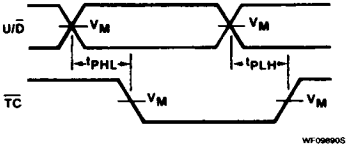
V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.

Waveform 2. Clock To Terminal Count Delays



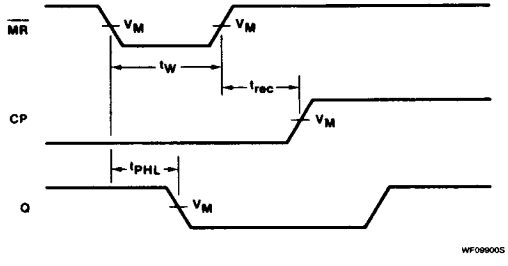
V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.

Waveform 3. Propagation Delay $\overline{CET}$ Input To Terminal Count Output



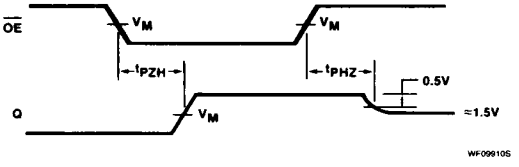
V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.

Waveform 4. Propagation Delay U/$\overline{D}$ Control To Terminal Count Output



V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.

Waveform 5. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time



V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.

Waveform 6. 3-State Enable Time To High Level And Disable Time From High Level

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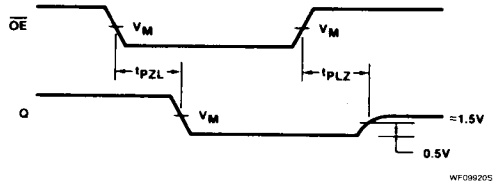
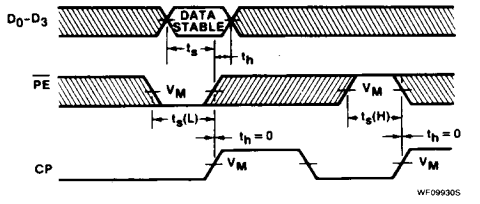
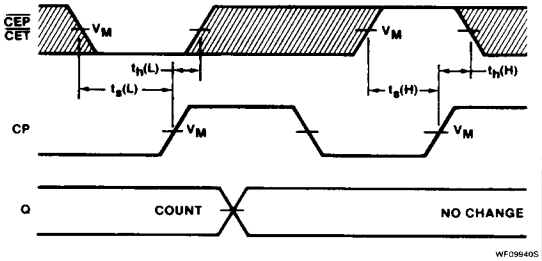
AC WAVEFORMS (Continued)



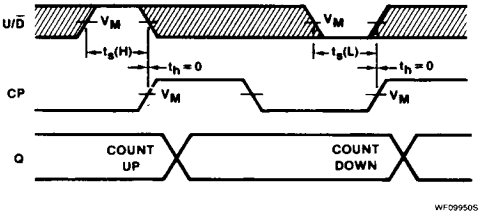
Waveform 7. 3-State Enable Time To Low Level And Disable Time From Low Level



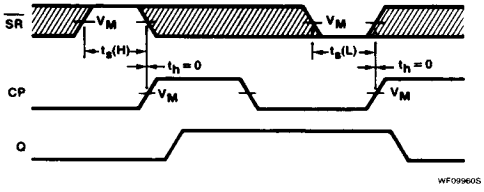
Waveform 8. Parallel Data And Parallel Enable Set-up And Hold Times



Waveform 9. Count Enable Set-up And Hold Times



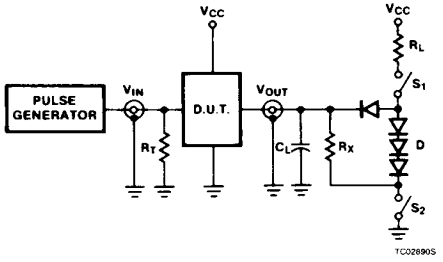
Waveform 10. Up/Down Control Set-up And Hold Times



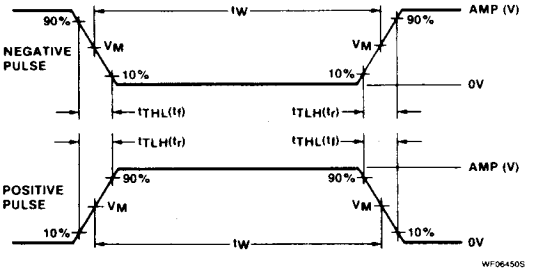
For all waveforms, V_M = 1.3V for 74 and 74S; V_M = 1.5V for 74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 11. Synchronous Reset Set-up And Hold Times

TEST CIRCUITS AND WAVEFORMS



Test Circuit For 3-State Outputs



V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH 1	SWITCH 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

R_X = 1kΩ for 74, 74S, R_X = 5kΩ for 74LS.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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