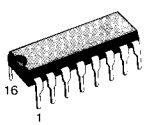
T54LS256 T74LS256

DUAL 4-BIT ADDRESSABLE LACTH

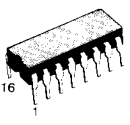
DESCRIPTION

The T54LS256/T74LS256 is a Dual 4-Bit Addressable Latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input ($\overline{E}$) and an active LOW Clear input ($\overline{C}$). Each latch has a Data input (D) and four outputs (Q_0-Q_3).

When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{C}$) is LOW, all outputs (Q_0-Q_3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{C}$ and $\overline{E}$ are both LOW. When $\overline{C}$ is HIGH and $\overline{E}$ is LOW, the selected outputs (Q_0-Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the lacth are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{C}$ = HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{C}$ = HIGH).



B1
Plastic Package



D1/D2
Ceramic Package

M1
Micro Package

C1
Plastic Chip Carrier

ORDERING NUMBERS:

T54LS256 D2	T74LS256 C1
T74LS256 D1	T74LS256 M1
T74LS256 B1	

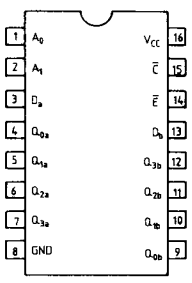
- SERIAL-TO-PARALLEL CAPABILITY
- OUTPUT FROM EACH STORAGE BIT AVAILABLE
- RANDOM (ADDRESSABLE) DATA ENTRY
- EASILY EXPANDABLE
- ACTIVE LOW COMMON CLEAR
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

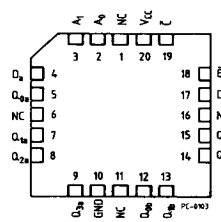
A_0,A_1	Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Enable (Active LOW) Input
$\overline{C}$	Clear (Active LOW) Input
Q_{0a}-Q_{3a}, Q_{0b}-Q_{3b}	Parallel Latch Outputs

PIN CONNECTION
(top view)

DUAL IN LINE

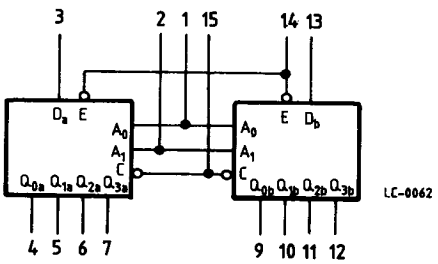


CHIP CARRIER



NC = No Internal Connection

LOGIC SYMBOL



MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Dual 4-Channel Demultiplexer
H	L	Clear

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 15	V
V_O	Output Voltage, Applied to Output	−0.5 to 10	V
I_I	Input Current, Into Inputs	−30 to 5	mA
I_O	Output Current, Into Outputs	30	mA

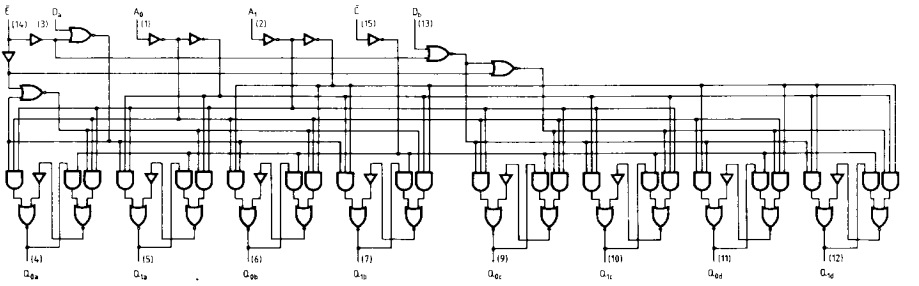
Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS256D2	4.5 V	5.0 V	5.5 V	−55°C to +125°C
T74LS256XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

XX = package type.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

TRUTH TABLE

$\overline{C}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3	MODE
L	H	X	X	X	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	Demultiplexer
L	L	H	L	L	H	L	L	L	
L	L	L	H	L	L	L	L	L	
L	L	H	H	L	L	H	L	L	
L	L	L	L	H	L	L	L	L	
L	L	H	L	H	L	L	H	L	
L	L	L	H	H	L	L	L	L	
L	L	H	H	H	L	L	L	H	
H	H	X	X	X	Q_{n-1}	Q_{n-1}	Q_{n-1}	Q_{n-1}	Memory
H	L	L	L	L	L	Q_{n-1}	Q_{n-1}	Q_{n-1}	Addressable Latch
H	L	H	L	L	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	
H	L	L	H	L	Q_{n-1}	L	Q_{n-1}	Q_{n-1}	
H	L	H	H	L	Q_{n-1}	H	Q_{n-1}	Q_{n-1}	
H	L	L	L	H	Q_{n-1}	Q_{n-1}	L	Q_{n-1}	
H	L	H	L	H	Q_{n-1}	Q_{n-1}	H	Q_{n-1}	
H	L	L	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	L	
H	L	H	H	H	Q_{n-1}	Q_{n-1}	Q_{n-1}	H	

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)		Units
			Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage		2.0			Guaranteed input Logical HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage	54			0.7	Guaranteed input Logical LOW Voltage for all Inputs		V
		74			0.8			
V_{CD}	Input Clamp Diode Voltage				−1.5	V_{CC} = MIN, I_{IN} = −18mA		V
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V_{CC} = MIN, I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
		74	2.4	3.1				
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
		74		0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current $\underline{A_0}$, A_1, $\overline{C}$, D_a, D_b				20	V_{CC} = MAX, V_{IN} = 2.7V		μA
	$\overline{E}$				40			
	Input HIGH Current $\underline{A_0}$, A_1, $\overline{C}$, D_a, D_b				0.1	V_{CC} = MAX, V_{IN} = 7.0V		mA
	$\overline{E}$				0.2			
I_{IL}	Input LOW Current $\underline{A_0}$, A_1, $\overline{C}$, D_a, D_b				−0.4	V_{CC} = MAX, V_{IN} = 0.4V		mA
	$\overline{E}$				−0.8			
I_{OS}	Output Short Circuit Current (Note 2)		−20		−100	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current			20	25	V_{CC} = MAX		mA

AC CHARACTERISTICS: T_A = 25°C

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_{PLH}	Turn-Off Delay, Enab. to Out.		20	27	Fig. 1	V_{CC} = 5.0V, C_L = 15pF	ns
t_{PHL}	Turn-On Delay, Enab. to Out.		16	24			
t_{PLH}	Turn-Off Delay, Data to Output		20	30	Fig. 2		ns
t_{PHL}	Turn-On Delay, Data to Output		13	20			
t_{PLH}	Turn-Off Delay, Addr. to Outp.		20	30	Fig. 3		ns
t_{PHL}	Turn-On Delay, Addr. to Outp.		14	24			
t_{PHL}	Turn-On Delay, Clear to Output		12	23	Fig. 5		ns

Notes:
1) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: $T_A = 25°C$

Symbol	Parameter	Limits			Test Conditions		Units
		Min.	Typ.	Max.			
t_sH	Set-up Time HIGH, Data to Enable	20	13		$V_{CC} = 5.0V$	Fig. 4	ns
t_hH	Hold Time HIGH, Data to Enable	0	−7.0				
t_sL	Set-up Time LOW, Data to Enable	15	7.0				ns
t_hL	Hold Time LOW, Data to Enable	0	10				
$t_sA\text{-}\overline{E}$	Set-up Time, Address to Enable (Note 4)	0	−7.0		$V_{CC} = 5.0V$	Fig. 6	ns
$t_W\overline{E}$	Enable Pulse Width	17	12		$V_{CC} = 5.0V$	Fig. 1	ns

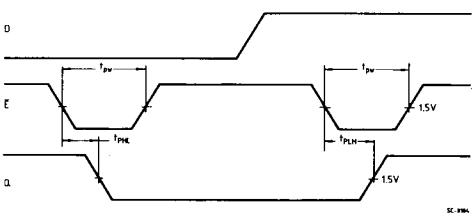
Notes:

4) The address to Enable Set-up Time is the time befor the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

5) The shaded areas indicate when the inputs are permitted to change for predictable output performance.

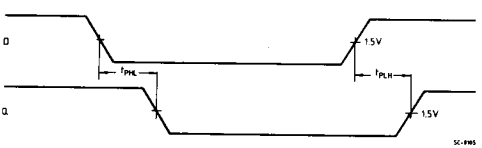
AC WAVEFORMS

Fig. 1 Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width



OTHER CONDITIONS: $\overline{C} = H$, A = STABLE

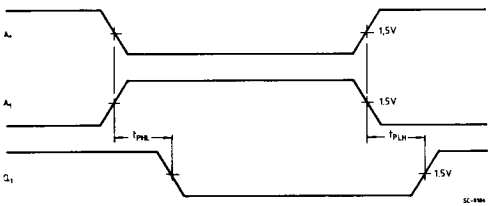
Fig. 2 Turn-On and Turn-Off Delays, Data to Output



OTHER CONDITIONS: $\overline{E} = L$, $\overline{C} = H$, A = STABLE

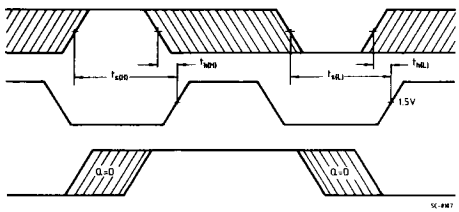
AC WAVEFORMS (Continued)

Fig. 3 Turn-On and Turn-Off Delays, Address to Output



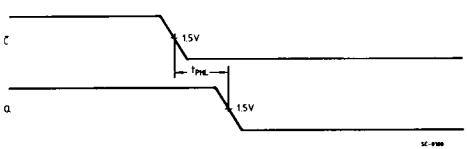
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 Set-up and Hold Time, Data to Enable



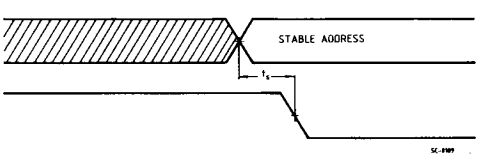
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 Turn-On Delay, Clear to Output



OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 Set-up Time, Address to Enable (see notes 4 and 5)



OTHER CONDITIONS: $\overline{C}$ = H