National Semiconductor

May 1997

74LCX373
Low-Voltage Octal Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

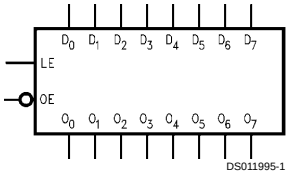
The LCX373 consists of eight latches with TRI-STATE® outputs for bus organized system applications. The device is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 8.0 ns t_{PD} max, 10 µA I_{CCQ} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 373
- Latch-up performance exceeds 500 mA
- ESD performance:
  — Human Body Model > 2000V
  — Machine Model > 200V

Logic Symbols



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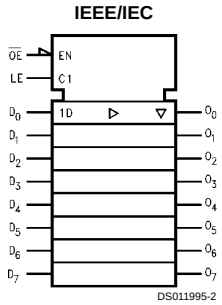

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	SOIC JEDEC	SOIC EIAJ	SSOP Type II	TSSOP JEDEC
Order Number	74LCX373WM	74LCX373SJ	74LCX373MSA	74LCX373MTC
	74LCX373WMX	74LCX373SJX	74LCX373MSAX	74LCX373MTCX
See NS Package Number	M20B	M20D	MSA20	MTC20

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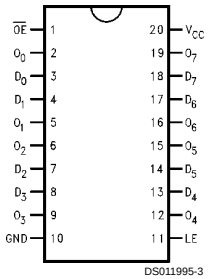
Quiet Series™ is a trademark of National Semiconductor Corporation.

Connection Diagram

Pin Assignment for SOIC, SSOP and TSSOP



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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Functional Description

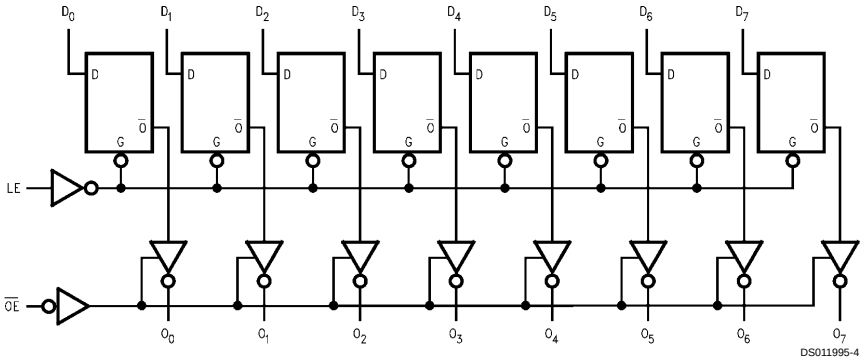
The LCX373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in TRI-STATE	V
		−0.5 to V_{CC} + 0.5	Output in High or Low State (Note 2)	V
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		˚C

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		TRI-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V–3.6V		±24	mA
		V_{CC} = 2.7V		±12	
T_A	Free-Air Operating Temperature		−40	85	˚C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	$I_{OH} = -100$ µA	2.7–3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12$ mA	2.7	2.2		V
		$I_{OH} = -18$ mA	3.0	2.4		V
		$I_{OH} = -24$ mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	$I_{OL} = 100$ µA	2.7–3.6		0.2	V
		$I_{OL} = 12$ mA	2.7		0.4	V
		$I_{OL} = 16$ mA	3.0		0.4	V
		$I_{OL} = 24$ mA	3.0		0.55	V
I_I	Input Leakage Current	$0 \le V_I \le 5.5V$	2.7–3.6		±5.0	µA
I_{OZ}	TRI-STATE Output Leakage	$0 \le V_O \le 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or $V_O = 5.5V$	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		10	µA
		$3.6V \le V_I, V_O \le 5.5V$	2.7–3.6		±10	µA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		500	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ C$ to $+85^\circ C$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	8.0	1.5	9.0	ns
t_{PLH}	D_n to O_n	1.5	8.0	1.5	9.0	
t_{PHL}	Propagation Delay	1.5	8.5	1.5	9.5	ns
t_{PLH}	LE to O_n	1.5	8.5	1.5	9.5	
t_{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	ns
t_{PZH}		1.5	8.5	1.5	9.5	
t_{PLZ}	Output Disable Time	1.5	7.5	1.5	8.5	ns
t_{PHZ}		1.5	7.5	1.5	8.5	
t_s	Setup Time, D_n to LE	2.5		2.5		ns
t_H	Hold Time, D_n to LE	1.5		1.5		ns
t_W	LE Pulse Width	3.3		3.3		ns
t_{OSHL}	Output to Output Skew		1.0			ns
t_{OSLH}	(Note 3)		1.0			

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}).

Dynamic Switching Characteristics

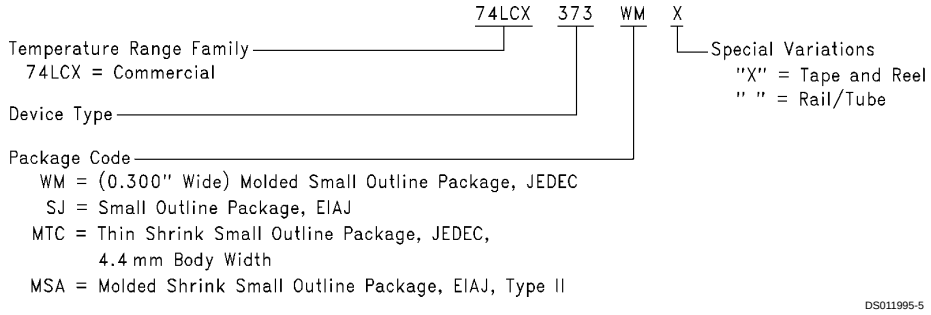
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3V, V_{IL} = 0V	3.3	−0.8	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	25	pF

74LCX373 Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows



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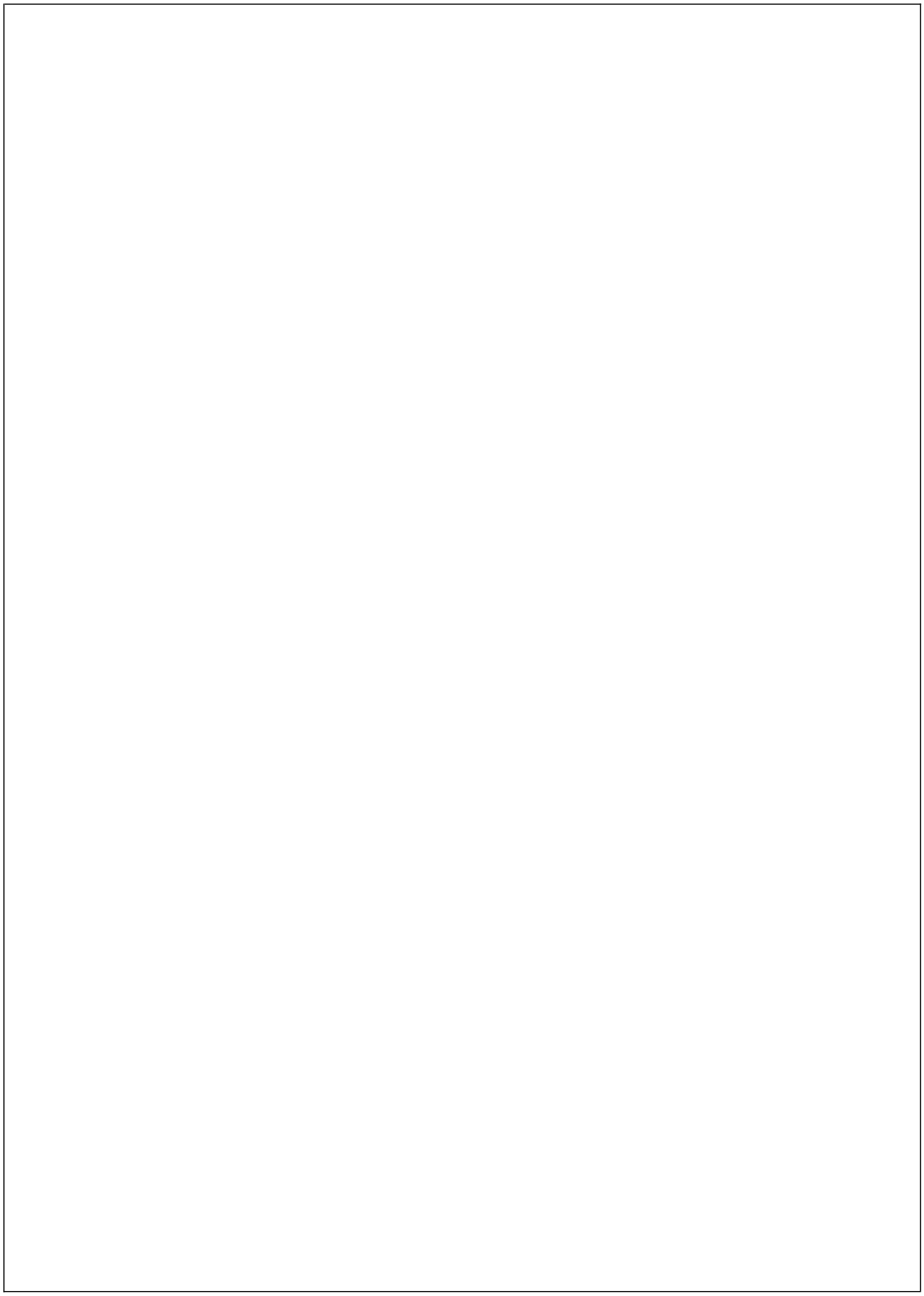
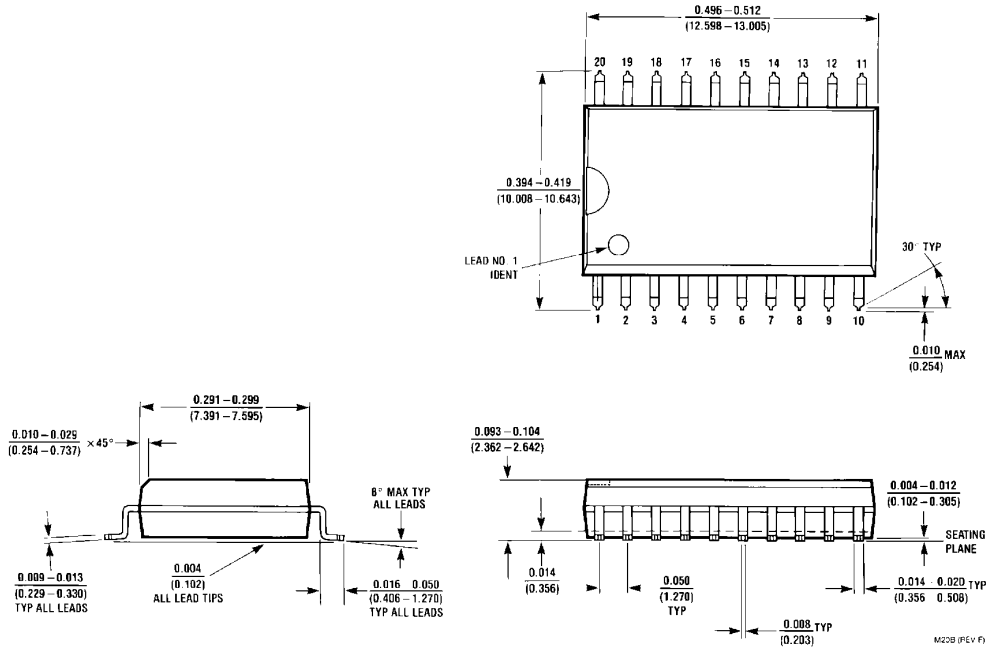
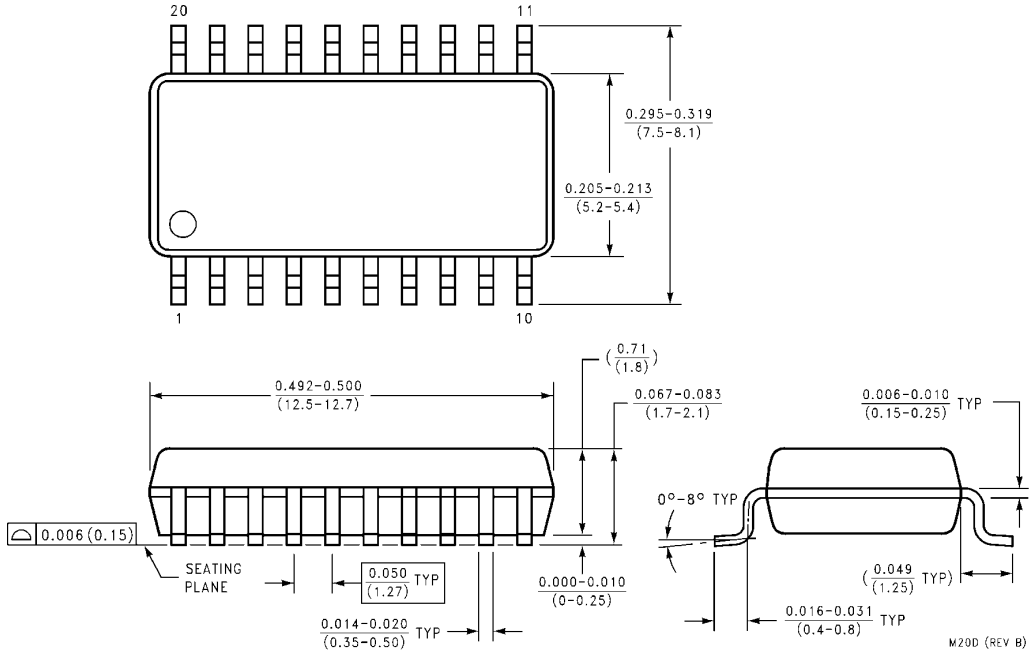


Physical Dimensions inches (millimeters)



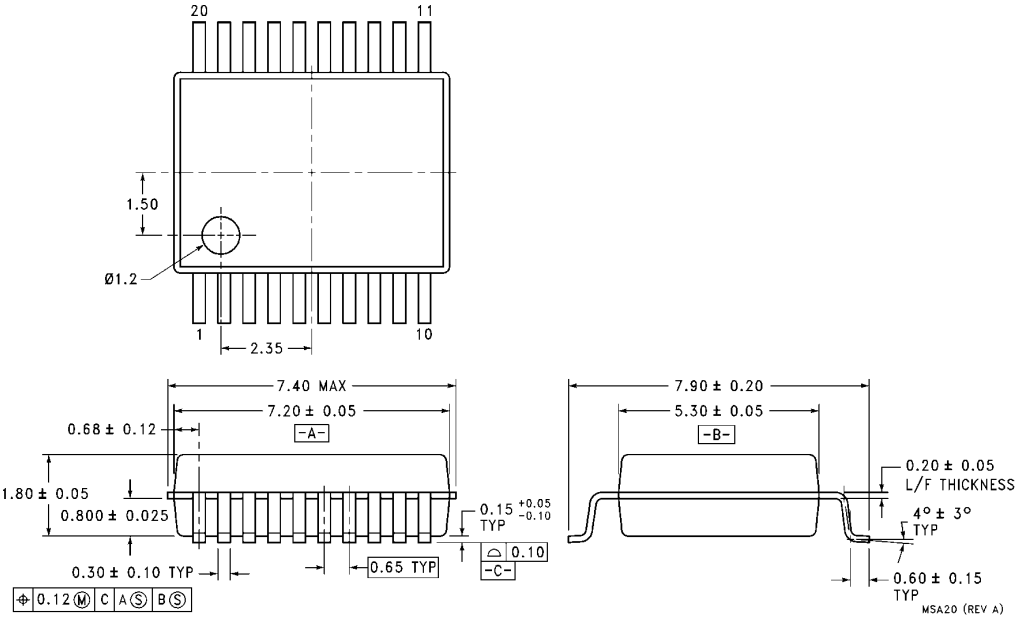
20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
Order Number 74LCX373WM or 74LCX373WMX
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



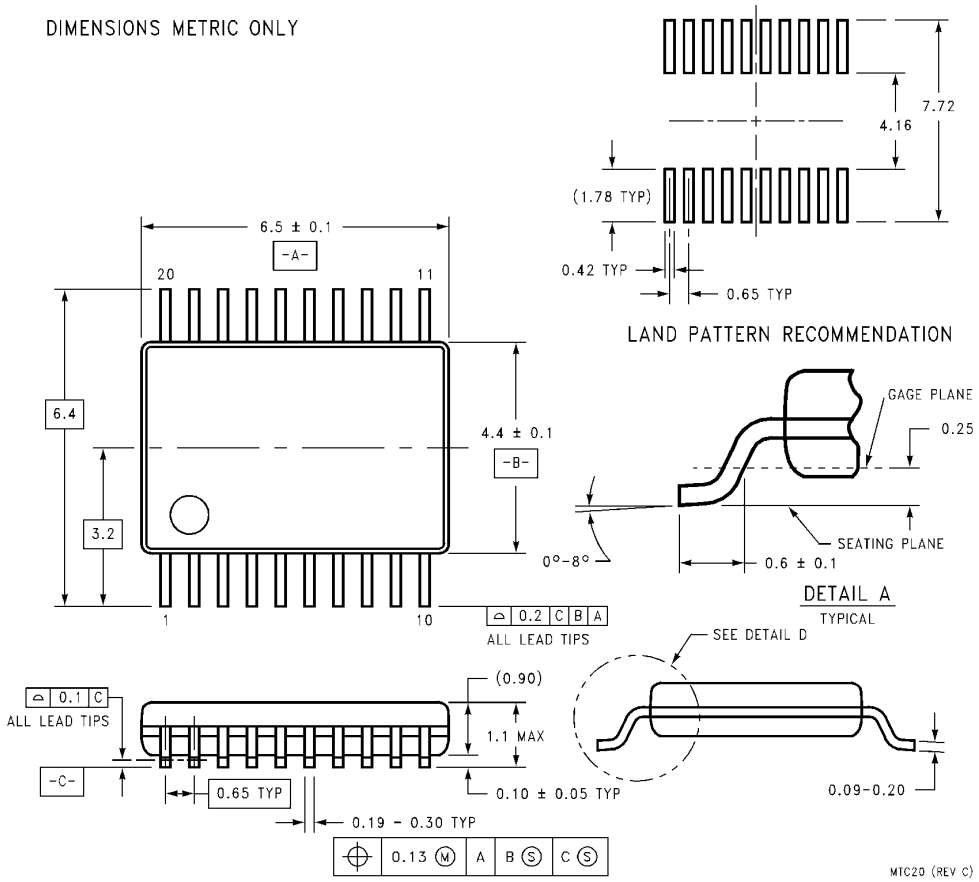
20-Lead Small Outline Package, EIAJ (SJ)
Order Number 74LCX373SJ or 74LCX373SJX
NS Package Number M20D

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded Shrink Small Outline Package, EIAJ, Type II
Order Number 74LCX373MSA or 74LCX373MSAX
NS Package Number MSA20

Physical Dimensions inches (millimeters) (Continued)



20-Lead Thin Shrink Small Outline Package, JEDEC
Order Number 74LCX373MTC or 74LCX373MTCX
NS Package Number MTC20

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