

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT85** 4-bit magnitude comparator

Product specification  
File under Integrated Circuits, IC06

December 1990

## 4-bit magnitude comparator

## 74HC/HCT85

### FEATURES

- Serial or parallel expansion without extra gating
- Magnitude comparison of any binary words
- Output capability: standard
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT85 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT85 are 4-bit magnitude comparators that can be expanded to almost any length. They perform comparison of two 4-bit binary, BCD or other monotonic codes and present the three possible magnitude results at the outputs ( $Q_{A>B}$ ,  $Q_{A=B}$  and  $Q_{A<B}$ ). The 4-bit inputs are

weighted ( $A_0$  to  $A_3$  and  $B_0$  to  $B_3$ ), where  $A_3$  and  $B_3$  are the most significant bits.

The operation of the "85" is described in the function table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed forward conditions that exist in the parallel expansion scheme.

For proper compare operation the expander inputs ( $I_{A>B}$ ,  $I_{A=B}$  and  $I_{A<B}$ ) to the least significant position must be connected as follows:  $I_{A<B} = I_{A>B} = \text{LOW}$  and  $I_{A=B} = \text{HIGH}$ .

For words greater than 4-bits, units can be cascaded by connecting outputs  $Q_{A<B}$ ,  $Q_{A>B}$  and  $Q_{A=B}$  to the corresponding inputs of the significant comparator.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$			
	$A_n, B_n$ to $Q_{A>B}$ , $Q_{A<B}$		20	22	ns
	$A_n, B_n$ to $Q_{A=B}$		18	20	ns
	$I_{A<B}$ , $I_{A=B}$ , $I_{A>B}$ to $Q_{A<B}$ , $Q_{A>B}$		15	15	ns
	$I_{A=B}$ to $Q_{A=B}$		11	15	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1 and 2	18	20	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND}$  to  $V_{CC}$   
For HCT the condition is  $V_I = \text{GND}$  to  $V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

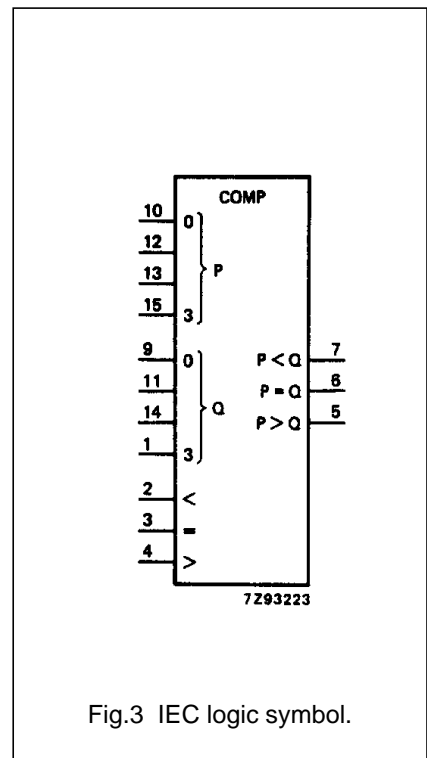
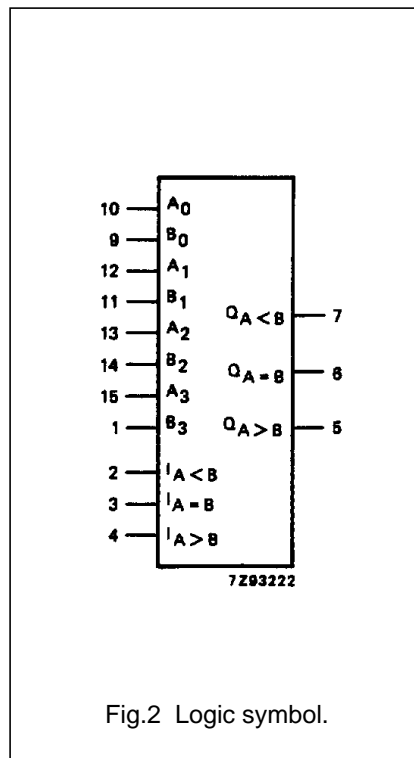
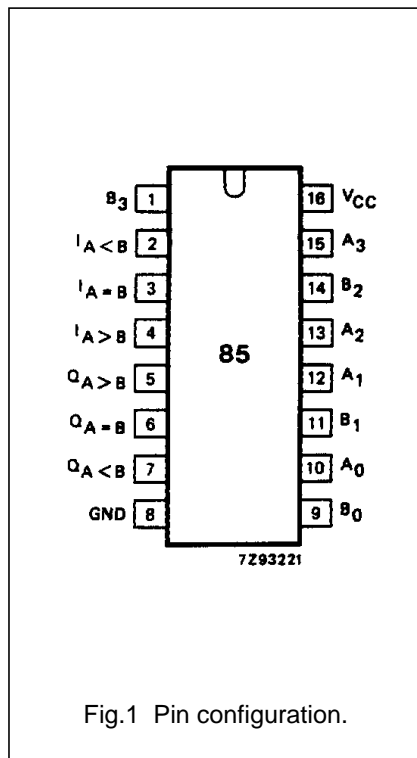
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2	$I_{A<B}$	A < B expansion input
3	$I_{A=B}$	A = B expansion input
4	$I_{A>B}$	A > B expansion input
5	$Q_{A>B}$	A > B output
6	$Q_{A=B}$	A = B output
7	$Q_{A<B}$	A < B output
8	GND	ground (0 V)
9, 11, 14, 1,	$B_0$ to $B_3$	word B inputs
10, 12, 13, 15	$A_0$ to $A_3$	word A inputs
16	$V_{CC}$	positive supply voltage



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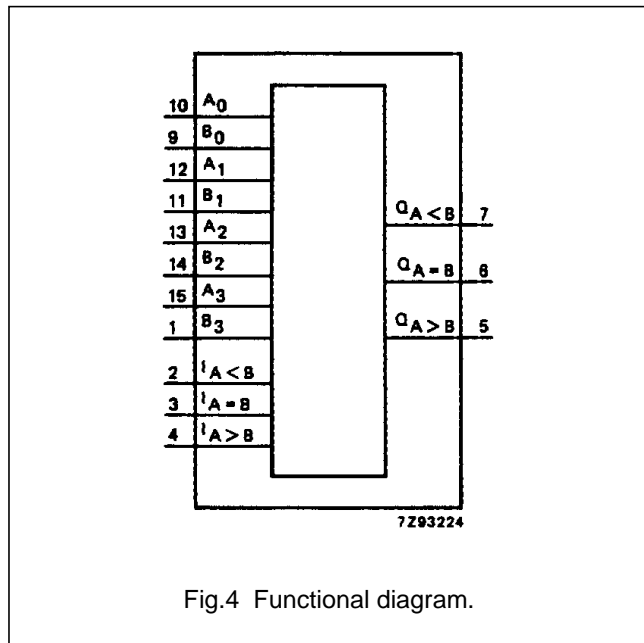


Fig.4 Functional diagram.

APPLICATIONS

- Process controllers
- Servo-motor control

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A <sub>3</sub> , B <sub>3</sub>	A <sub>2</sub> , B <sub>2</sub>	A <sub>1</sub> , B <sub>1</sub>	A <sub>0</sub> , B <sub>0</sub>	I <sub>A&gt;B</sub>	I <sub>A&lt;B</sub>	I <sub>A=B</sub>	Q <sub>A&gt;B</sub>	Q <sub>A&lt;B</sub>	Q <sub>A=B</sub>
A <sub>3</sub> >B <sub>3</sub>	X	X	X	X	X	X	H	L	L
A <sub>3</sub> <B <sub>3</sub>	X	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> >B <sub>2</sub>	X	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> <B <sub>2</sub>	X	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> >B <sub>1</sub>	X	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> <B <sub>1</sub>	X	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> >B <sub>0</sub>	X	X	X	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> <B <sub>0</sub>	X	X	X	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	L	L	H	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	H	L	L	H	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	L	H	L	L	H
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	X	X	H	L	L	H
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	H	H	L	L	L	L
A <sub>3</sub> =B <sub>3</sub>	A <sub>2</sub> =B <sub>2</sub>	A <sub>1</sub> =B <sub>1</sub>	A <sub>0</sub> =B <sub>0</sub>	L	L	L	H	H	L

Notes

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care

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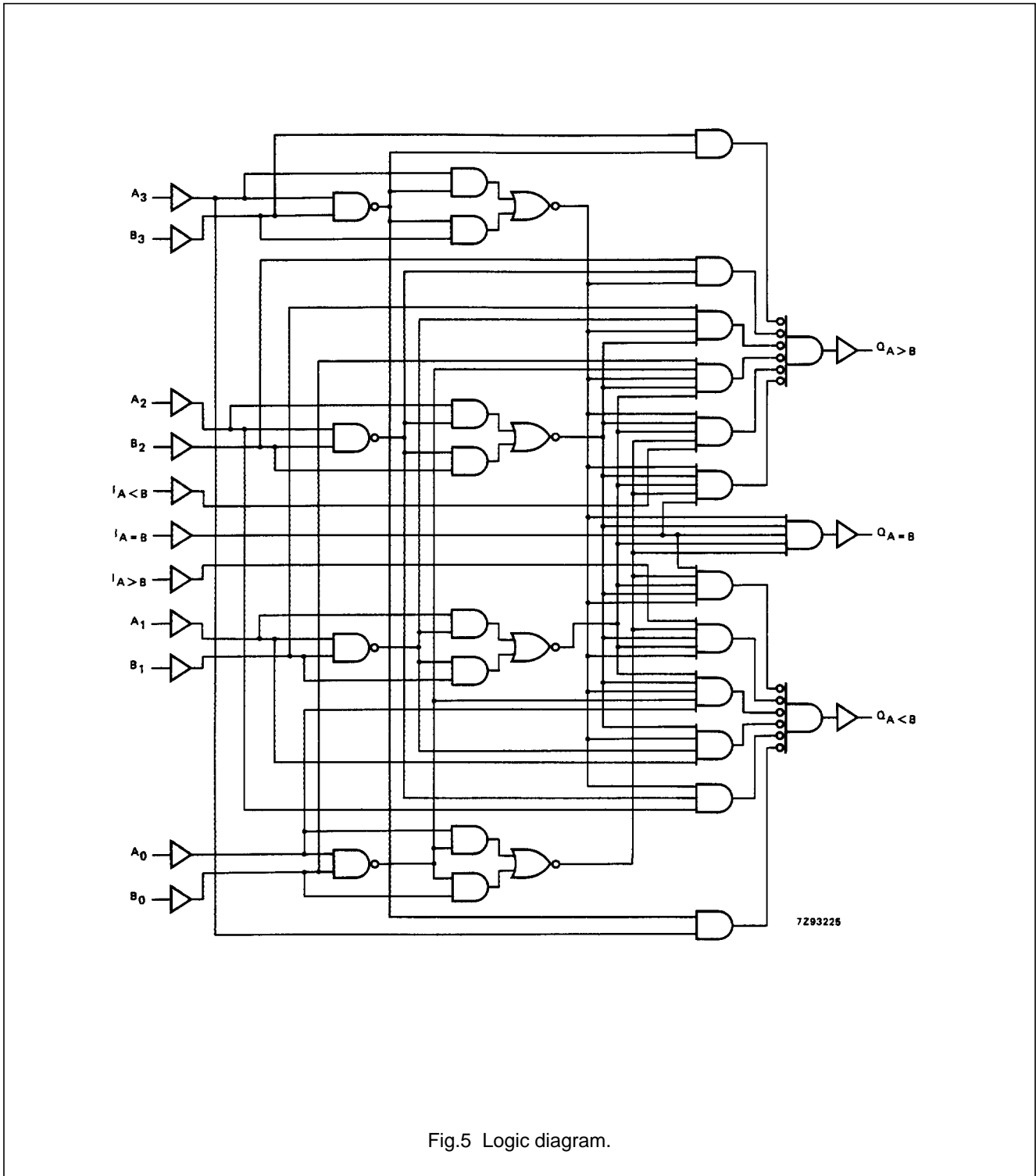


Fig.5 Logic diagram.

## 4-bit magnitude comparator

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	V <sub>CC</sub> (V)	TEST CONDITIONS WAVEFORMS
		74HC										
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A&gt;B</sub> or Q <sub>A&lt;B</sub>		63	195		245		295	ns	2.0	Fig.6	
			23	39		49		59				
			18	33		42		50				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A=B</sub>		58	175		220		265	ns	2.0	Fig.6	
			21	35		44		53				
			17	30		37		45				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>A&lt;B</sub> , I <sub>A=B</sub> , I <sub>A&gt;B</sub> to Q <sub>A&lt;B</sub> , Q <sub>A&gt;B</sub>		50	140		175		210	ns	2.0	Fig.6	
			18	28		35		42				
			14	24		30		36				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>A=B</sub> to Q <sub>A=B</sub>		39	120		150		180	ns	2.0	Fig.6	
			14	24		30		36				
			11	20		26		31				
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19	75		95		110	ns	2.0	Fig.6	
			7	15		19		22				
			6	13		16		19				

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I <sub>A&lt;B</sub>	1.00
I <sub>A&gt;B</sub>	1.00
I <sub>A=B</sub>	1.50
A <sub>n</sub> , B <sub>n</sub>	1.50

**AC CHARACTERISTICS FOR 74HCT**

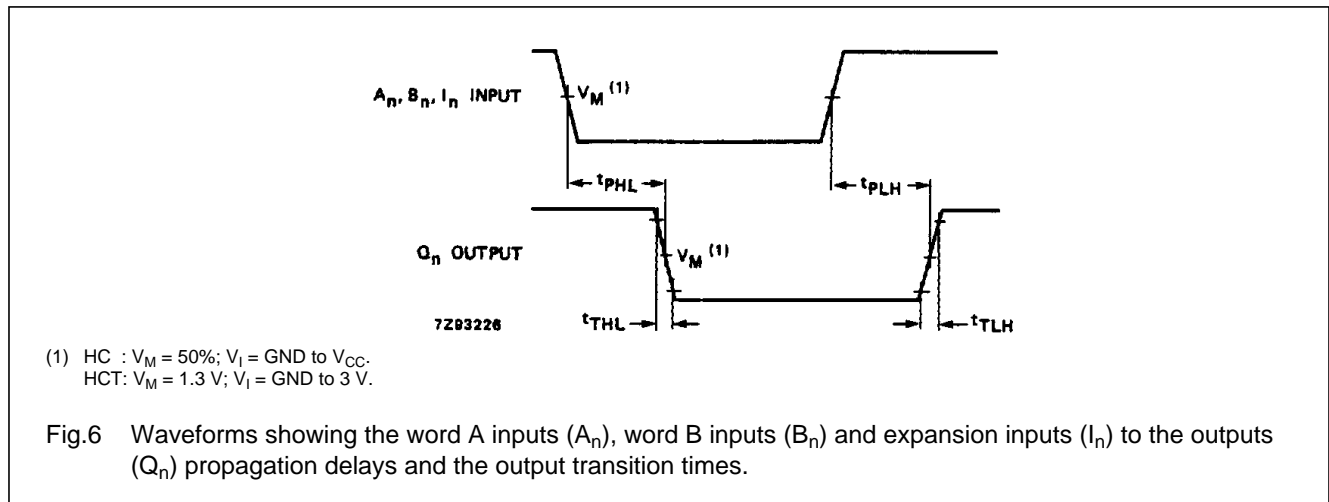
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A&gt;B</sub> or Q <sub>A&lt;B</sub>		26	44		55		66	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to Q <sub>A=B</sub>		24	40		50		60	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>A&lt;B</sub> , I <sub>A=B</sub> , I <sub>A&gt;B</sub> to Q <sub>A&lt;B</sub> , Q <sub>A&gt;B</sub>		18	31		39		47	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay I <sub>A=B</sub> to Q <sub>A=B</sub>		18	31		39		47	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6

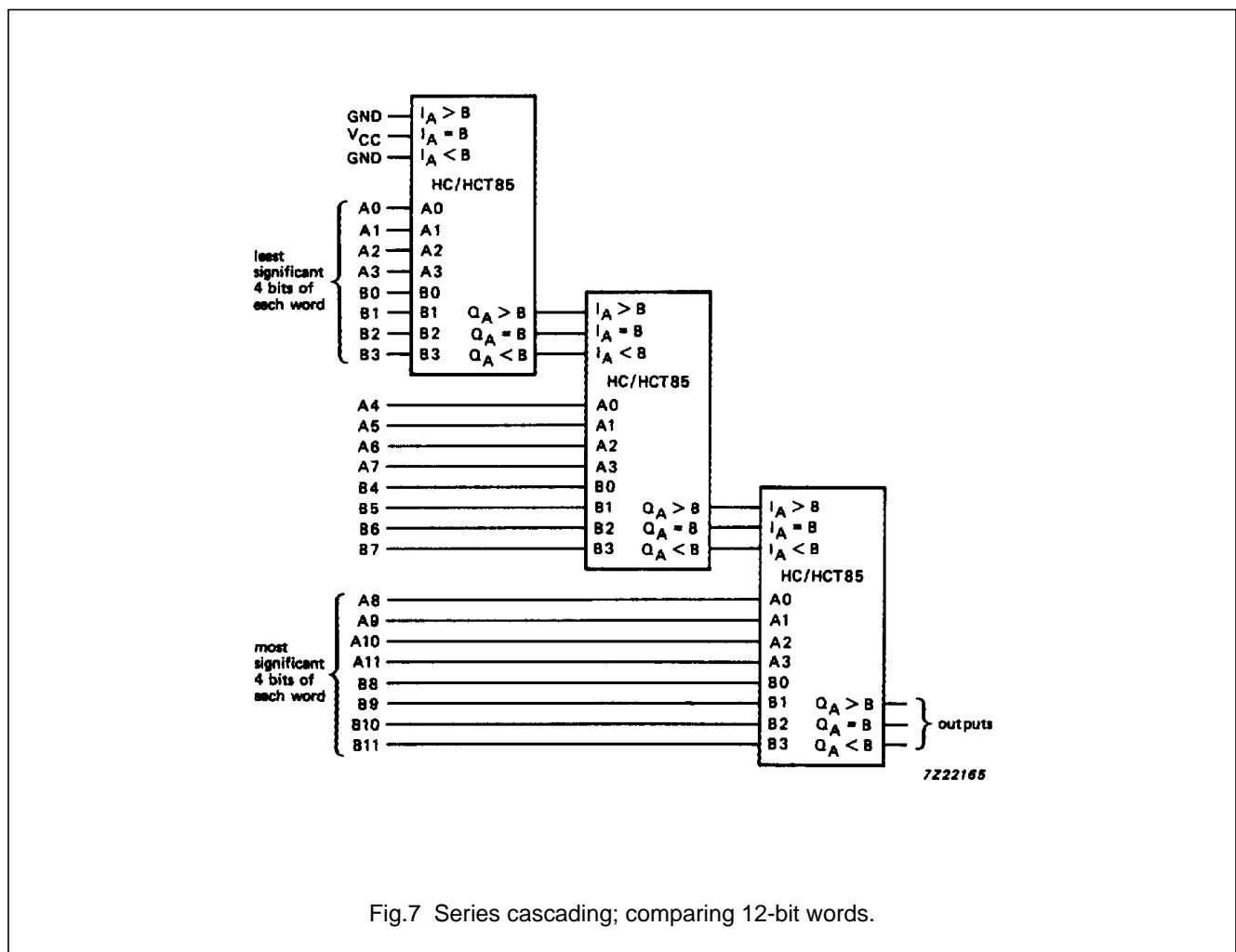
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## AC WAVEFORMS



## APPLICATION INFORMATION





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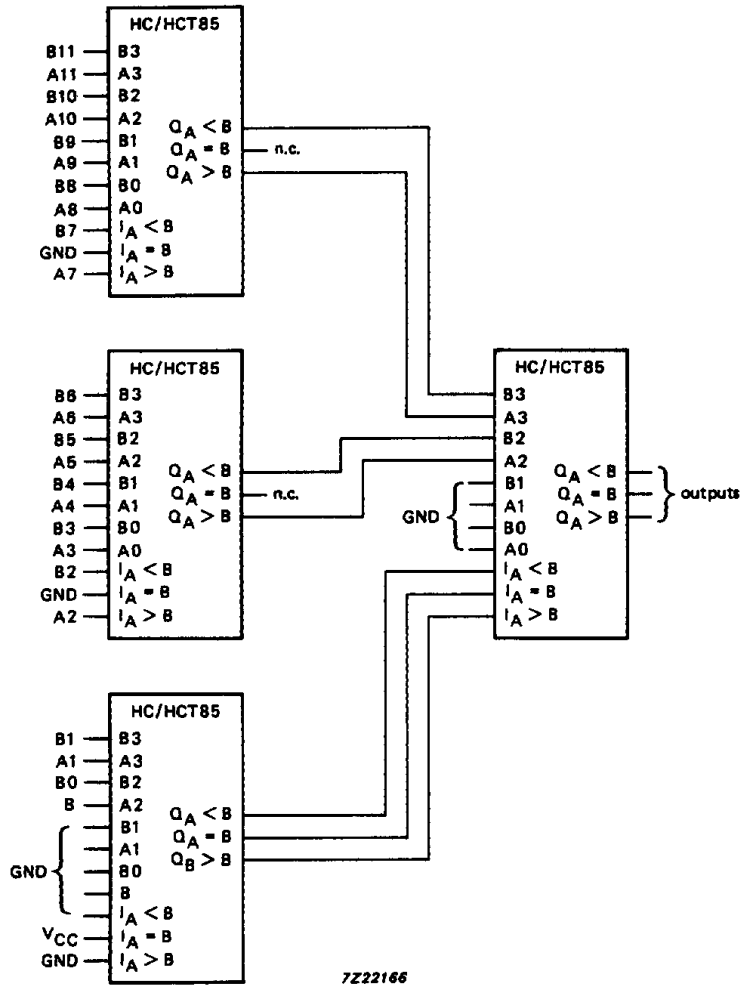


Fig.8 Parallel cascading; comparing 12-bit words.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".