PHASE-LOCKED-LOOP WITH VCO

FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

(continued on next page)

APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

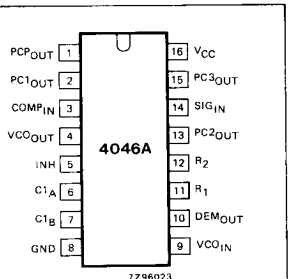


Fig. 1 Pin configuration.

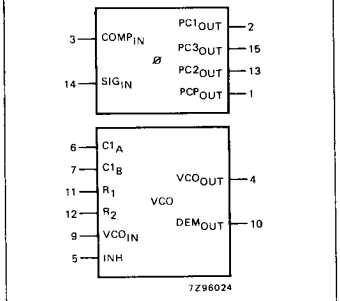


Fig. 2 Logic symbol.

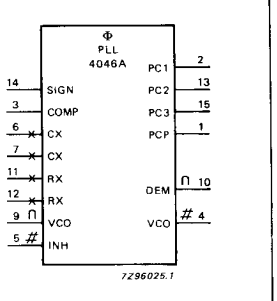


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP_{OUT}	phase comparator pulse output
2	$PC1_{OUT}$	phase comparator 1 output
3	$COMP_{IN}$	comparator input
4	VCO_{OUT}	VCO output
5	INH	inhibit input
6	$C1_A$	capacitor C1 connection A
7	$C1_B$	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO_{IN}	VCO input
10	DEM_{OUT}	demodulator output
11	R_1	resistor R1 connection
12	R_2	resistor R2 connection
13	$PC2_{OUT}$	phase comparator 2 output
14	SIG_{IN}	signal input
15	$PC3_{OUT}$	phase comparator 3 output
16	V_{CC}	positive supply voltage

GENERAL DESCRIPTION (Cont'd)

VCO

The VCO requires one external capacitor C1 (between $C1_A$ and $C1_B$) and one external resistor R1 (between R_1 and GND) or two external resistors R1 and R2 (between R_1 and GND, and R_2 and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input ($COMP_{IN}$), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG_{IN} (pin 14) or $COMP_{IN}$ (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC1OUT}$ (via low-pass filter).

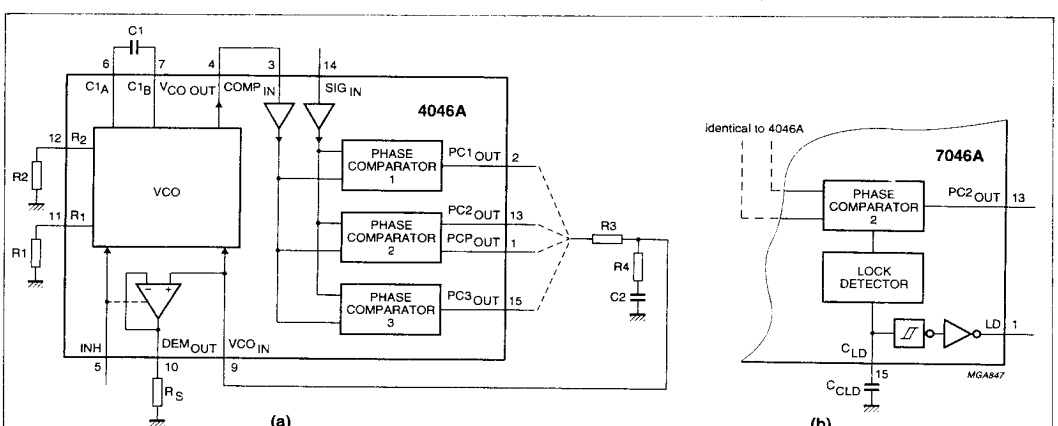


Fig. 4 Functional diagram.

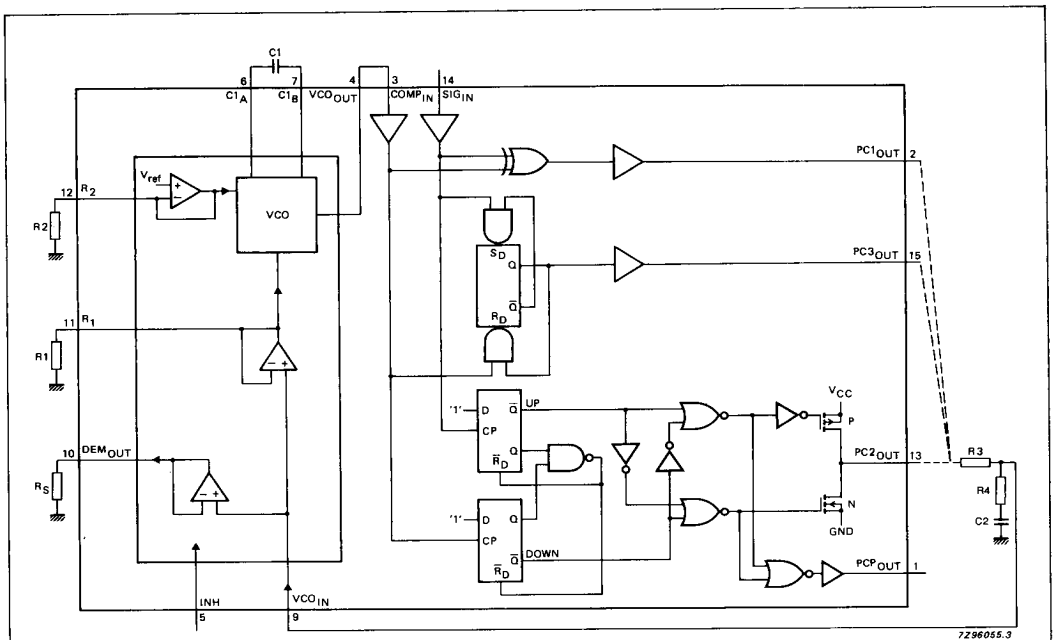


Fig. 5 Logic diagram.

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{\pi} \text{ (V/r)}.$$

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input ($COMP_{IN}$) as shown in Fig. 6. The average of V_{DEMOUT} is equal to 1/2 V_{CC} when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_o). Typical waveforms for the PC1 loop locked at f_o are shown in Fig. 7.

The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

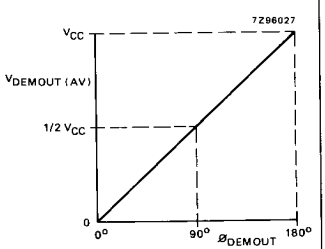


Fig. 6 Phase comparator 1: average output voltage versus input phase difference:

$V_{DEMOUT} = V_{PC1OUT} =$

$\frac{V_{CC}}{\pi}(\phi_{SIGIN} - \phi_{COMPIN})$

$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

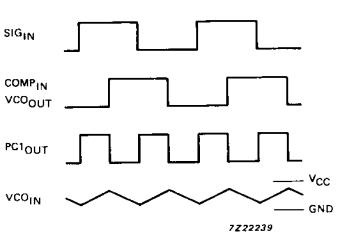


Fig. 7 Typical waveforms for PLL using phase comparator 1, loop locked at f_o.

GENERAL DESCRIPTION (Cont'd)

Phase comparators (Cont'd)

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range. This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig. 5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{4\pi} \text{ (V/r)}.$$

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig. 9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p- type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

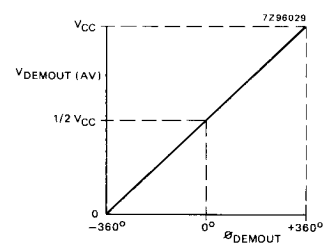


Fig. 8 Phase comparator 2: average output voltage versus input phase difference:
$V_{DEMOUT} = V_{PC2OUT} =$
$\frac{V_{CC}}{4\pi}(\phi_{SIGIN} - \phi_{COMPIN})$
$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

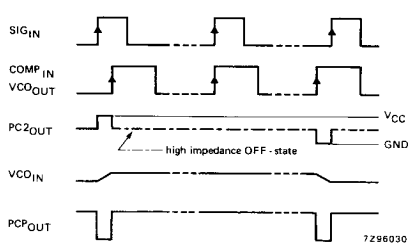


Fig. 9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed, is:

$$V_{DEMOUT} = \frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
$V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The phase comparator gain is:

$$K_p = \frac{V_{CC}}{2\pi} \text{ (V/r)}.$$

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig. 10. Typical waveforms for the PC3 loop locked at f_o are shown in Fig. 11.

The phase-to-output response characteristic of PC3 (Fig. 10) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC3, to its lowest frequency.

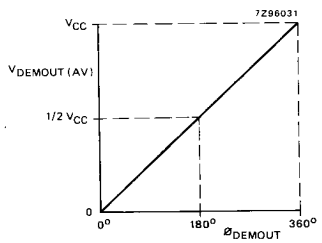


Fig. 10 Phase comparator 3: average output voltage versus input phase difference:
$V_{DEMOUT} = V_{PC3OUT} =$
$\frac{V_{CC}}{2\pi}(\phi_{SIGIN} - \phi_{COMPIN})$
$\phi_{DEMOUT} = (\phi_{SIGIN} - \phi_{COMPIN})$.

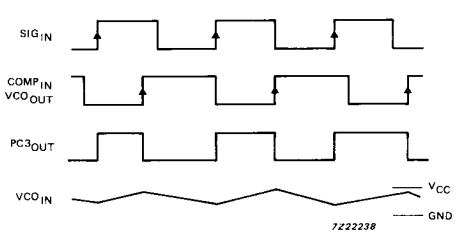


Fig. 11 Typical waveforms for PLL using phase comparator 3, loop locked at f_o.

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V_{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHARACTERISTICS
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times (pin 5)		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
$\pm I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current		25	mA	for -0.5 V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC}$; $\pm I_{GND}$	DC V_{CC} or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range: −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5, and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			3.0 7.0 18.0 30.0		4.0 9.0 23.0 38.0		5.0 11.0 27.0 45.0	μA	2.0 3.0 4.5 6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		800 250 150						kΩ	3.0 4.5 6.0	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HC (Cont'd)

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2		V	3.0 4.5 6.0		
V_{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8		0.9 1.35 1.8	V	3.0 4.5 6.0		
V_{OH}	HIGH level output voltage VCO_{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9		V	3.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$ $-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O = 4.0$ mA $-I_O = 5.2$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	3.0 4.5 6.0	V_{IH} or V_{IL}	$I_O = 20\ \mu A$ $I_O = 20\ \mu A$ $I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$			0.40 0.40		0.47 0.47		0.54 0.54	V	4.5 6.0	V_{IH} or V_{IL}	$I_O = 4.0$ mA $I_O = 5.2$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
R1	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
R2	resistor range	3.0 3.0 3.0		300 300 300					kΩ	3.0 4.5 6.0		note 1
C1	capacitor range	40 40 40		no limit					pF	3.0 4.5 6.0		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1 1.1 1.1		1.9 3.4 5.9					V	3.0 4.5 6.0		over the range specified for R1; for linearity see Figs 20 and 21.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50 50 50		300 300 300					kΩ	3.0 4.5 6.0	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 15
R_D	dynamic output resistance at DEM_{OUT}		25 25 25						Ω	3.0 4.5 6.0	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		63 23 18	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		96 35 28	340 68 58		425 85 72		510 102 87	ns	2.0 4.5 6.0	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		77 28 22	270 54 46		340 68 58		405 81 69	ns	2.0 4.5 6.0	Fig. 16
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		83 30 24	280 56 48		350 70 60		420 84 71	ns	2.0 4.5 6.0	Fig. 17
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		99 36 29	325 65 55		405 81 69		490 98 83	ns	2.0 4.5 6.0	Fig. 17
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 16
$V_{I(p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		9 11 15 33						mV	2.0 3.0 4.5 6.0	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN}$ = 1/2 V_{CC}; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18
f_o	VCO centre frequency (duty factor = 50%)	3.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μA	6.0	pins 3, 5 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	μA	4.5 to 5.5	pins 3 and 14 at V_{CC}; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above.
   To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	DC coupled HIGH level input voltage SIG_{IN}, $COMP_{IN}$	3.15	2.4						V	4.5		
V_{IL}	DC coupled LOW level input voltage SIG_{IN}, $COMP_{IN}$		2.1	1.35					V	4.5		
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage PCP_{OUT}, PC_{nOUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage PCP_{OUT}, PC_{nOUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current SIG_{IN}, $COMP_{IN}$			30		38		45	μA	5.5	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current $PC2_{OUT}$			0.5		5.0		10.0	μA	5.5	V_{IH} or V_{IL}	$V_O = V_{CC}$ or GND
R_I	input resistance SIG_{IN}, $COMP_{IN}$		250						kΩ	4.5	V_I at self-bias operating point; $\Delta V_I = 0.5$ V; see Figs 12, 13 and 14	

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} V	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V_{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V_{OH}	HIGH level output voltage VCO_{OUT}	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O = 20\ \mu A$
V_{OH}	HIGH level output voltage VCO_{OUT}	3.98	4.32		3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O = 4.0$ mA
V_{OL}	LOW level output voltage VCO_{OUT}		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	$I_O = 20\ \mu A$
V_{OL}	LOW level output voltage VCO_{OUT}		0.15	0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
V_{OL}	LOW level output voltage $C1_A$, $C1_B$ (test purposes only)			0.40		0.47		0.54	V	4.5	V_{IH} or V_{IL}	$I_O = 4.0$ mA
$\pm I_I$	input leakage current INH, VCO_{IN}			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R2	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V_{VCOIN}	operating voltage range at VCO_{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 20 and 21.

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	OTHER
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R_S	resistor range	50		300					kΩ	4.5	at $R_S > 300$ kΩ the leakage current can influence V_{DEMOUT}
V_{OFF}	offset voltage VCO_{IN} to V_{DEMOUT}		±20						mV	4.5	$V_I = V_{VCOIN} = 1/2\ V_{CC}$; values taken over R_S range; see Fig. 15
R_D	dynamic output resistance at DEM_{OUT}		25						Ω	4.5	$V_{DEMOUT} = 1/2\ V_{CC}$

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	OTHER
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC1_{OUT}$		23	40		50		60	ns	4.5	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to PCP_{OUT}		35	68		85		102	ns	4.5	Fig. 16
t_{PHL}/t_{PLH}	propagation delay SIG_{IN}, $COMP_{IN}$ to $PC3_{OUT}$		28	54		68		81	ns	4.5	Fig. 16
t_{PZH}/t_{PZL}	3-state output enable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		30	56		70		84	ns	4.5	Fig. 17
t_{PHZ}/t_{PLZ}	3-state output disable time SIG_{IN}, $COMP_{IN}$ to $PC2_{OUT}$		36	65		81		98	ns	4.5	Fig. 17
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 16
$V_{I\ (p-p)}$	AC coupled input sensitivity (peak-to-peak value) at SIG_{IN} or $COMP_{IN}$		15						mV	4.5	f_i = 1 MHz

VCO section

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT									
		+25			−40 to +85		−40 to +125			V_{CC} V	OTHER
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.15				%/K	4.5	$V_I = V_{VCOIN}$ within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig. 18b
f_o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V_{VCOIN} = 1/2 V_{CC}; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig. 19
Δf_{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ_{VCO}	duty factor at VCO_{OUT}		50						%	4.5	

FIGURE REFERENCES FOR DC CHARACTERISTICS

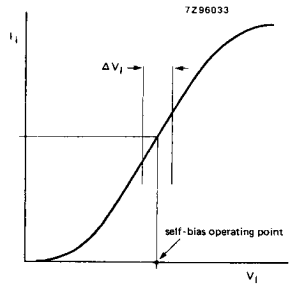


Fig. 12 Typical input resistance curve at SIG_{IN}, $COMP_{IN}$.

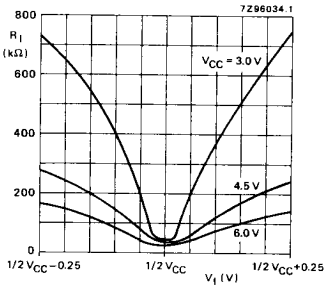


Fig. 13 Input resistance at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.

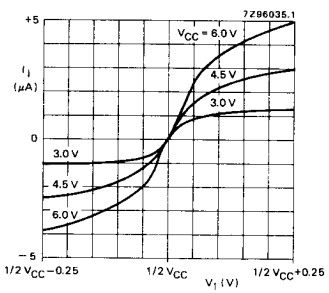
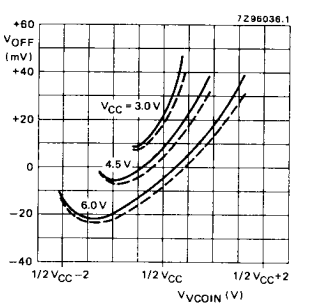


Fig. 14 Input current at SIG_{IN}, $COMP_{IN}$ with ΔV_I = 0.5 V at self-bias point.



—— R_S = 50 kΩ
- - - R_S = 300 kΩ

Fig. 15 Offset voltage at demodulator output as a function of VCO_{IN} and R_S.

AC WAVEFORMS

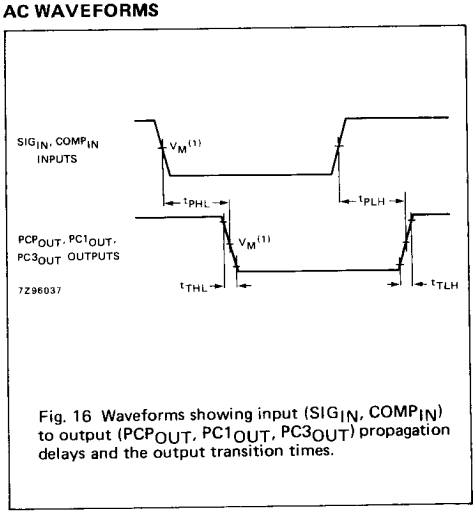


Fig. 16 Waveforms showing input (SIG_{IN}, $COMP_{IN}$) to output (PCP_{OUT}, $PC1_{OUT}$, $PC3_{OUT}$) propagation delays and the output transition times.

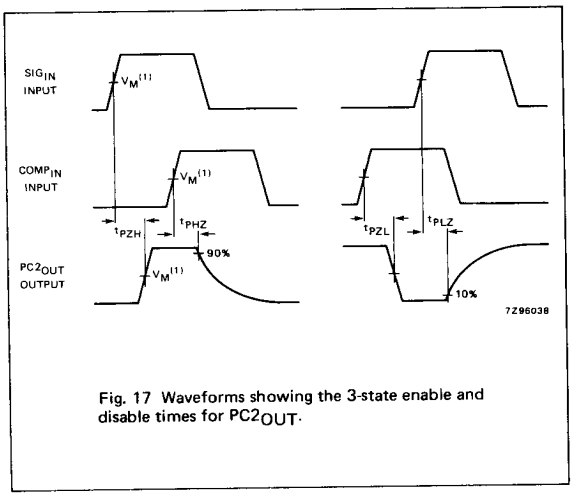


Fig. 17 Waveforms showing the 3-state enable and disable times for $PC2_{OUT}$.

Note to AC waveforms

(1) HC : $V_M = 50\%$; V_I = GND to V_{CC}.

AC WAVE FORMS (Continued)

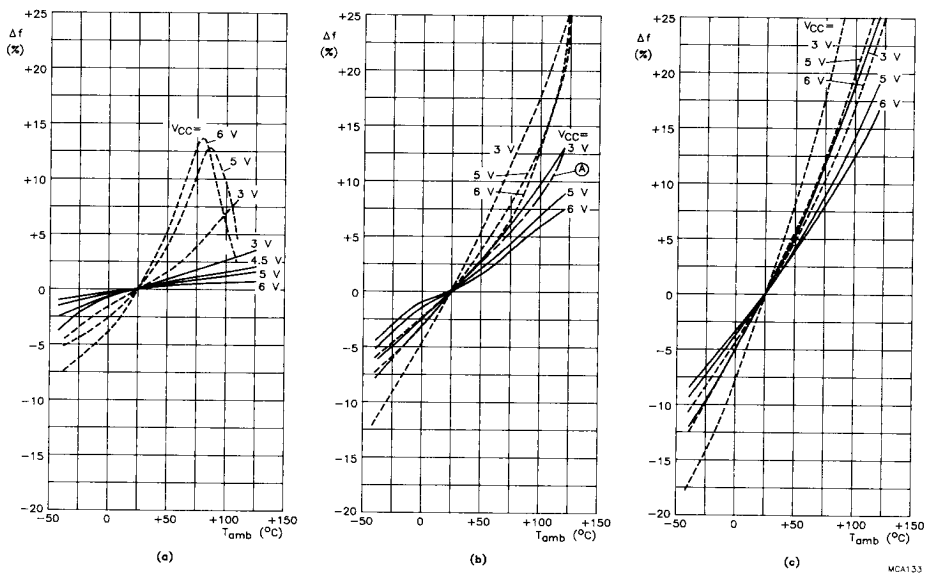
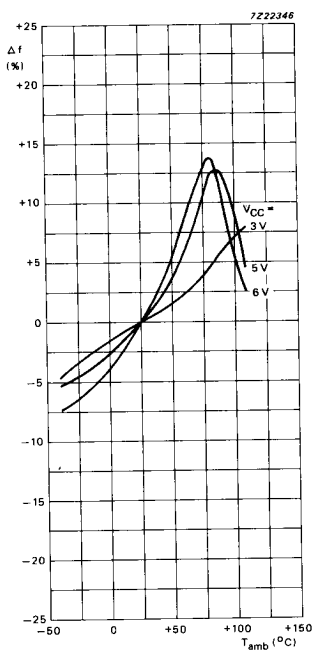
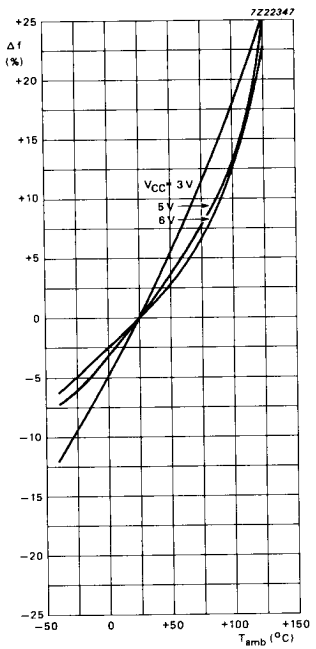


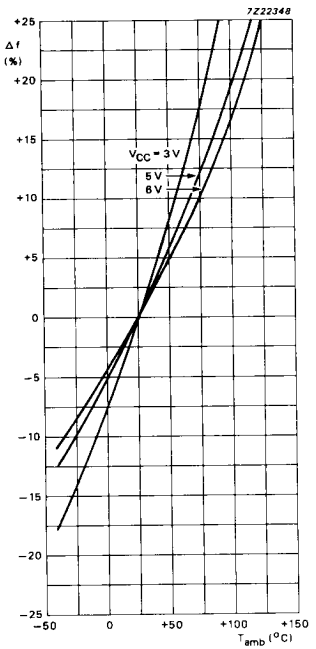
Fig.18 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.
——— without offset (R2 = ∞): (a) R1 = 3 kΩ; (b) R1 = 10 kΩ; (c) R1 = 300 kΩ.
– – – with offset (R1 = ∞): (a) R2 = 3 kΩ; (b) R2 = 10 kΩ; (c) R2 = 300 kΩ.
In (b), the frequency stability for R1 = R2 = 10 kΩ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 kΩ stability cuves. C1 = 100 pF; $V_{VCO\ IN} = 0.5\ V_{CC}$.



(d) $R_2 = 3\ k\Omega$
$R_1 = \infty$



(e) $R_2 = 10\ k\Omega$
$R_1 = \infty$

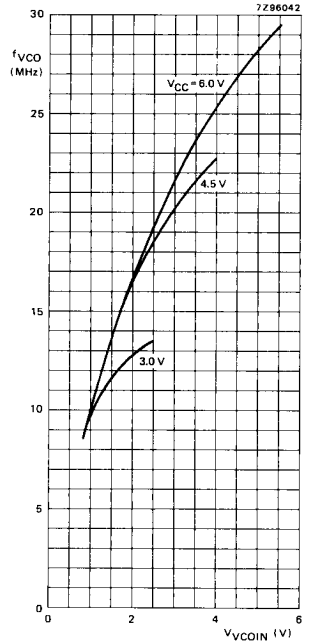


(f) $R_2 = 300\ k\Omega$
$R_1 = \infty$

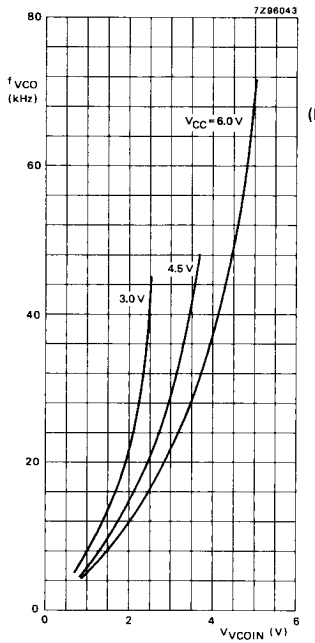
Fig. 18 Continued.

Note to Fig. 18
To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

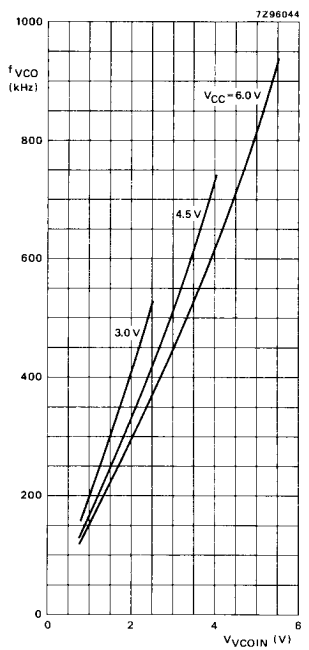
AC WAVEFORMS (Continued)



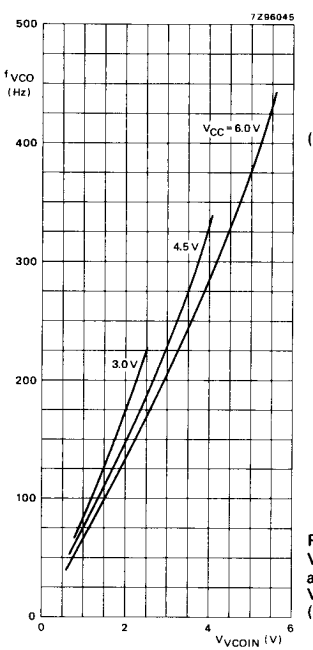
(a) R1 = 3 kΩ; C1 = 40 pF



(b) R1 = 3 kΩ; C1 = 100 nF



(c) R1 = 300 kΩ; C1 = 40 pF



(d) R1 = 300 kΩ; C1 = 100 nF

Fig. 19 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

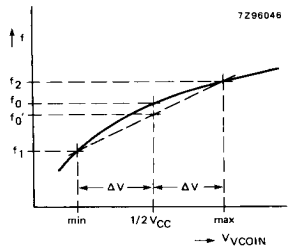


Fig. 20 Definition of VCO frequency linearity: $\Delta V = 0.5$ V over the V_{CC} range: for VCO linearity

$$f'_0 = \frac{f_1 + f_2}{2},$$

$$\text{linearity} = \frac{f'_0 - f_0}{f'_0} \times 100\%$$

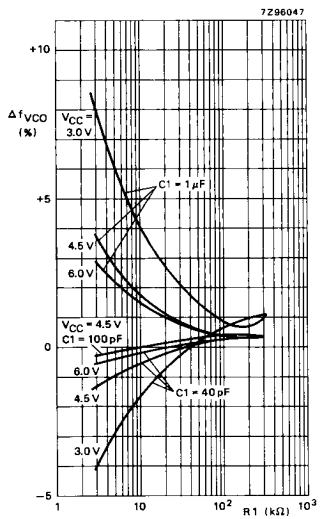
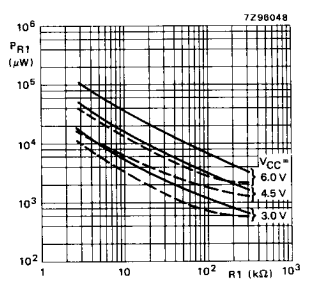
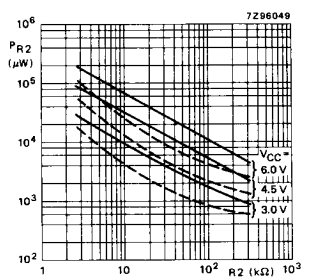


Fig. 21 Frequency linearity as a function of R1, C1 and V_{CC}: $R2 = \infty$ and $\Delta V = 0.5$ V.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 22 Power dissipation versus the value of R1: $C_L = 50$ pF; R2 = ∞; $V_{VCOIN} = 1/2\ V_{CC}$; $T_{amb} = 25$ °C.



— C1 = 40 pF
- - - C1 = 1 μF

Fig. 23 Power dissipation versus the value of R2: $C_L = 50$ pF; R1 = ∞; $V_{VCOIN} = GND = 0$ V; $T_{amb} = 25$ °C.

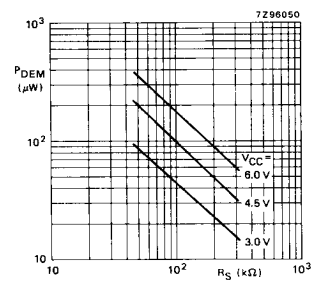


Fig. 24 Typical dc power dissipation of demodulator sections as a function of R_S: R1 = R2 = ∞; $T_{amb} = 25$ °C; $V_{VCOIN} = 1/2\ V_{CC}$.

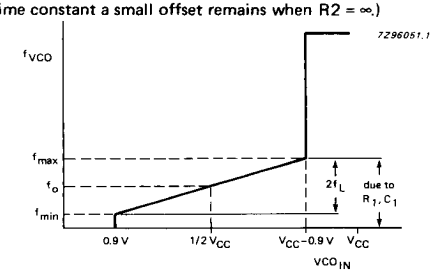
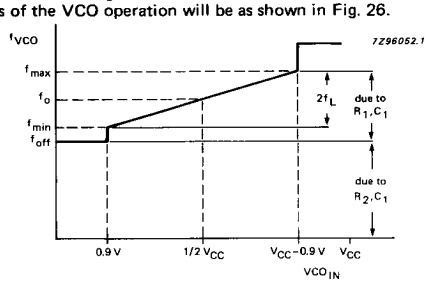
APPLICATION INFORMATION

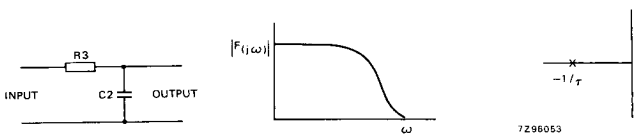
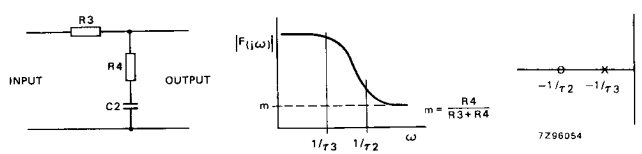
This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

References should be made to Figs 29, 30 and 31 as indicated in the table.

Values of the selected components should be within the following ranges:

R1	between 3 kΩ and 300 kΩ;
R2	between 3 kΩ and 300 kΩ;
R1 + R2	parallel value > 2.7 kΩ;
C1	greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency **without extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R2 = ∞ and R1 within the range 3 kΩ < R1 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 25. (Due to R1, C1 time constant a small offset remains when R2 = ∞.)  Fig. 25 Frequency characteristic of VCO operating without offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1	**Selection of R1 and C1** Given f_o, determine the values of R1 and C1 using Fig. 29.
	PC2 or PC3	Given f_{max} and f_o, determine the values of R1 and C1 using Fig. 29, use Fig. 31 to obtain $2f_L$ and then use this to calculate f_{min}.
VCO frequency **with extra offset**	PC1, PC2 or PC3	**VCO frequency characteristic** With R1 and R2 within the ranges 3 kΩ < R1 < 300 kΩ, 3 kΩ < R2 < 300 kΩ, the characteristics of the VCO operation will be as shown in Fig. 26.  Fig. 26 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.
	PC1, PC2 or PC3	**Selection of R1, R2 and C1** Given f_o and f_L, determine the value of product R1C1 by using Fig. 31. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C1 and R2 by using Fig. 30. Calculate the value of R1 from the value of C1 and the product R1C1.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with ϕ_{DEMOUT} = 90° and V_{VCOIN} = 1/2 V_{CC} (see Fig. 6).
	PC2	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 8).
	PC3	VCO adjusts to f_o with ϕ_{DEMOUT} = −360° and V_{VCOIN} = min. (see Fig. 10).
PLL frequency capture range	PC1, PC2 or PC3	**Loop filter component selection**  (a) τ = R3 x C2 (b) amplitude characteristic (c) pole-zero diagram A small capture range ($2f_c$) is obtained if $2f_c \approx 1/\pi\ (\sqrt{2\pi f_L/\tau})$ Fig. 27 Simple loop filter for PLL **without** offset; R3 ⩾ 500 Ω.  (a) τ_1 = R3 x C2; τ_2 = R4 x C2; τ_3 = (R3 + R4) x C2 (b) amplitude characteristic (c) pole-zero diagram Fig. 28 Simple loop filter for PLL **with** offset; R3 + R4 ⩾ 500 Ω.
PLL locks on harmonics at centre frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at ϕ_{DEMOUT} = 90°
	PC2	$f_r = f_i$, small ripple content at ϕ_{DEMOUT} = 0°
	PC3	$f_r = f_i$, large ripple content at ϕ_{DEMOUT} = 180°

APPLICATION INFORMATION (Continued)

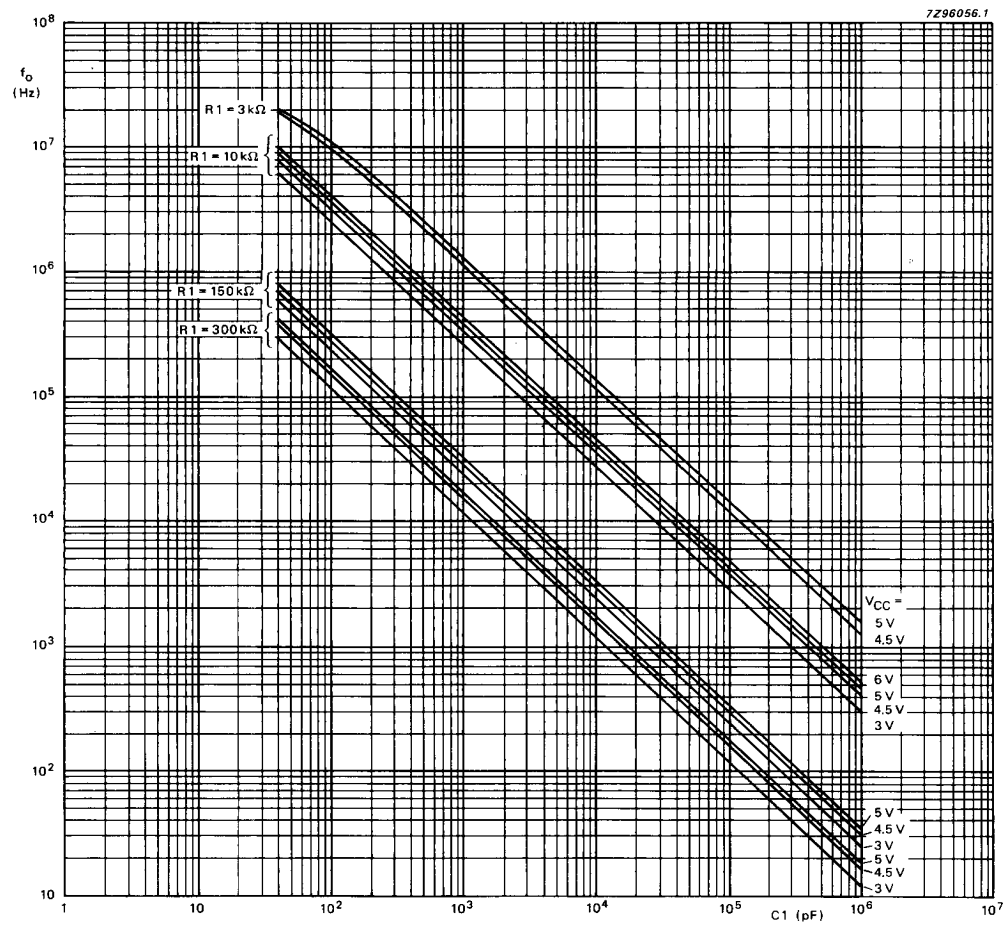


Fig. 29 Typical value of VCO centre frequency (f_o) as a function of C1: R2 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 29

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R1 can be easily calculated because, a constant R1C1 product will produce almost the same VCO output frequency.

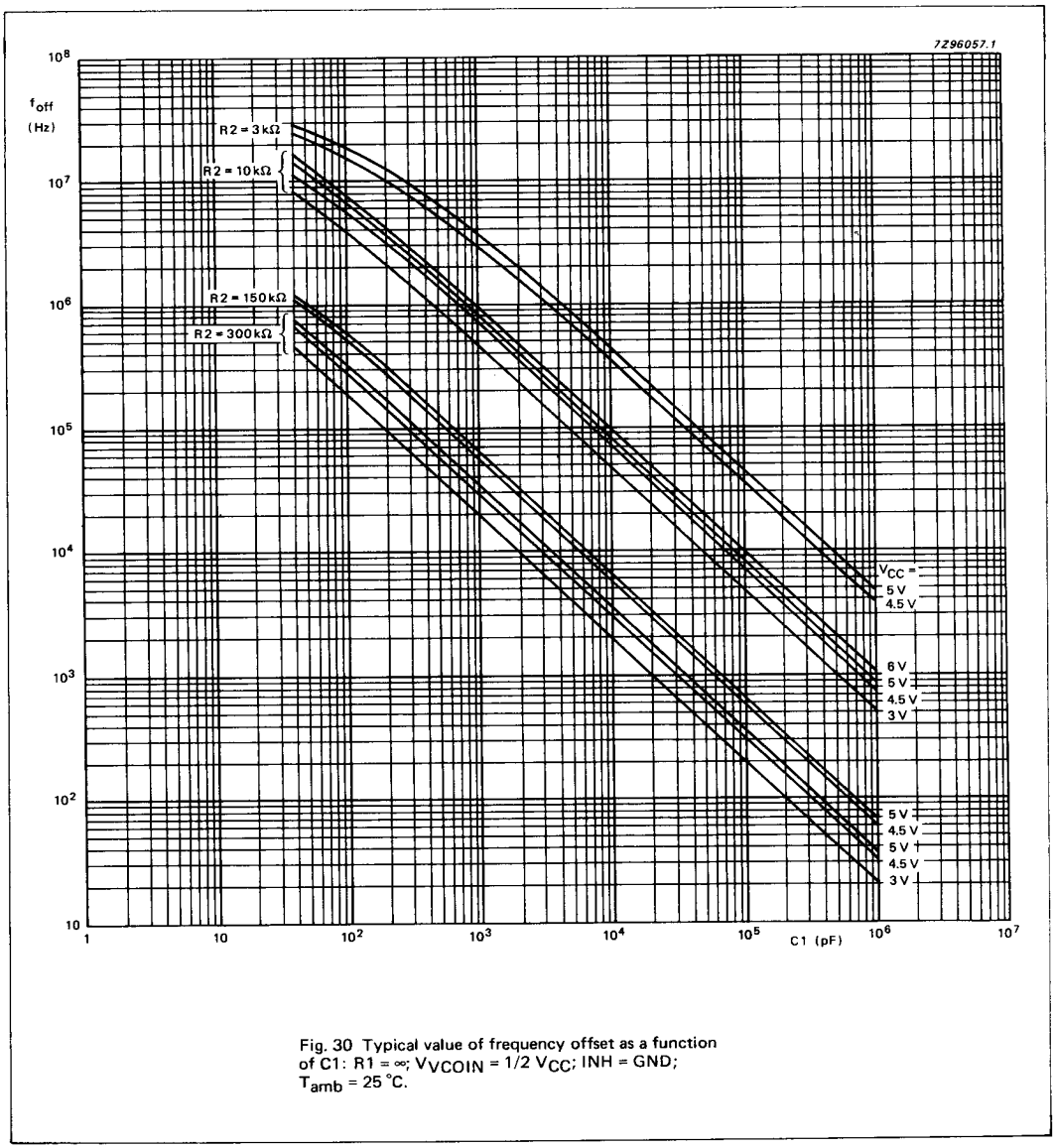


Fig. 30 Typical value of frequency offset as a function of C1: R1 = ∞; V_{VCOIN} = 1/2 V_{CC}; INH = GND; T_{amb} = 25 °C.

Notes to Fig. 30

1. To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
2. Interpolation for various values of R2 can be easily calculated because, a constant R2C1 product will produce almost the same VCO output frequency.

APPLICATION INFORMATION (Continued)

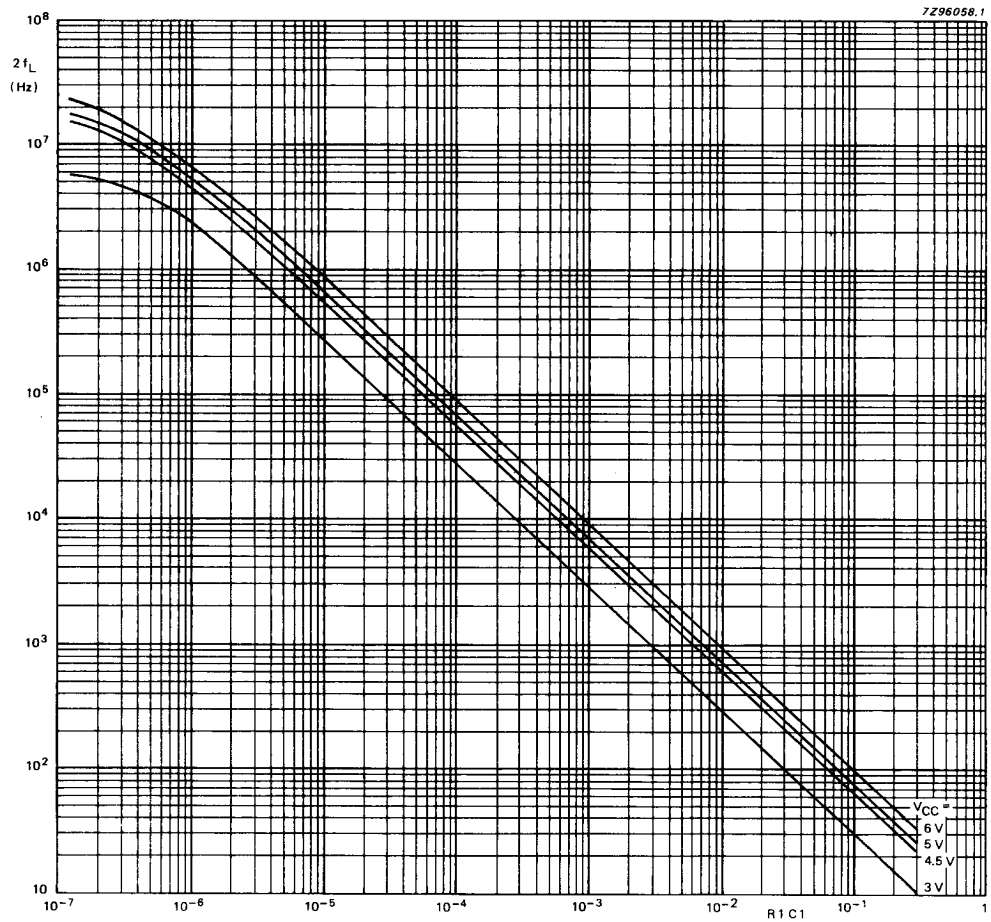


Fig. 31 Typical frequency lock range ($2f_L$) versus the product R1C1: V_{VCOIN} range = 0.9 to (V_{CC} − 0.9) V; R2 = ∞; VCO gain:

$$K_v = \frac{2f_L}{V_{VCOIN\ range}} 2\pi \text{ (r/s/V)}.$$

PLL design example

The frequency synthesizer, used in the design example shown in Fig. 32, has the following parameters:

Output frequency: 2 MHz to 3 MHz
frequency steps : 100 kHz
settling time : 1 ms
overshoot : < 20%

The open-loop gain is H (s) x G (s) = $K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
K_f = low-pass filter transfer gain
K_o = K_v/s VCO gain
K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2\ MHz}{100\ kHz} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3\ MHz}{100\ kHz} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable).
The values can be determined using the information in the section "DESIGN CONSIDERATIONS".
With f_o = 2.5 MHz and f_L = 500 kHz this gives the following values (V_{CC} = 5.0 V):
R1 = 10 kΩ
R2 = 10 kΩ
C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)} = \frac{1\ MHz}{3.2} \times 2\pi \approx 2 \times 10^6\ r/s/V$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4\ V/r.$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}.$$

Where:

τ_1 = R3C2 and τ_2 = R4C2.

The characteristics equation is:

$1 + H(s) \times G(s) = 0.$

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0.$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}.$$

and the damping value ξ is defined as follows:

$$\xi = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}.$$

In Fig. 33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n. From Fig. 33 it can be seen that the damping ratio ξ = 0.45 will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t$ = 5. The required settling time is 1 ms. This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3\ r/s.$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}.$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011\ s.$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \xi - 1}{K_p \times K_v \times K_n \times C2} = 315\ \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2\ k\Omega.$$

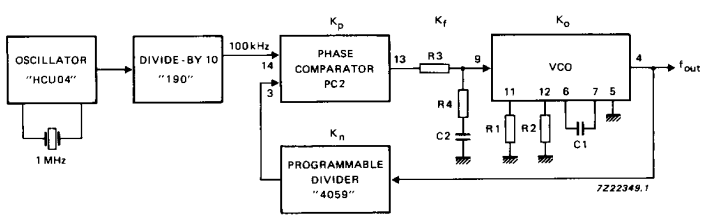


Fig. 32 Frequency synthesizer.

Note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.
Also available a computer design program for PLL's ordering number 9398 961 10061.

APPLICATION INFORMATION (Continued)

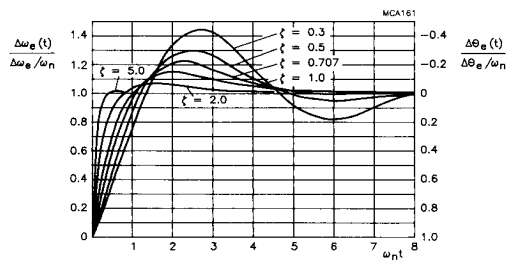


Fig. 33 Type 2, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

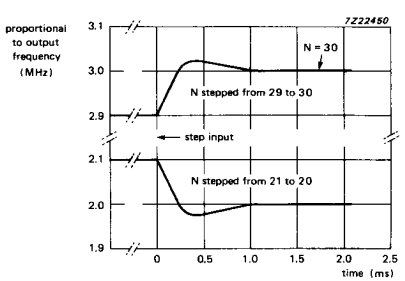


Fig. 34 Frequency compared to the time response.