TC74HC690P DECADE COUNTER REGISTER
TC74HC691P 4-BIT BINARY COUNTER REGISTER

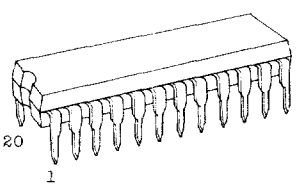
The TC74HC690/691 are high speed CMOS COUNTER/REGISTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

TC74HC690 is BCD DECADE COUNTER, TC74HC691 is 4-BIT BINARY COUNTER, these devices have Registers respectively.
If LOAD input ($\overline{LOAD}$) is held "L", DATA input (A ~ D) are loaded in internal counter at positive edge of counter clock input ($\overline{CCK}$). And at counter mode, internal counter counts up at positive edge of counter clock. If counter clear input ($\overline{CCLR}$) is held "L", internal counter cleared asynchronously to counter clock.

Internal counter's outputs are stored in output register at positive edge of register clock (RCK). If register clear input ($\overline{RCLR}$) is held "L", the register cleared asynchronously to register clock. At this point, internal counter outputs no change. The outputs (Q_A ~ Q_D) are selected internal counter outputs or register outputs respectively by output select input (R/$\overline{C}$). Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gate.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

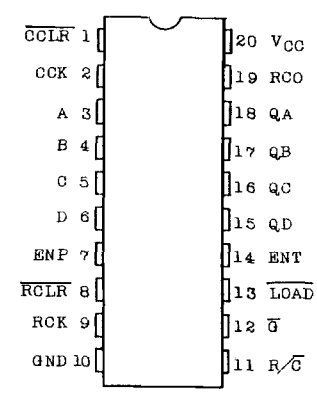


DIP20(3D20A-P)

FEATURES:

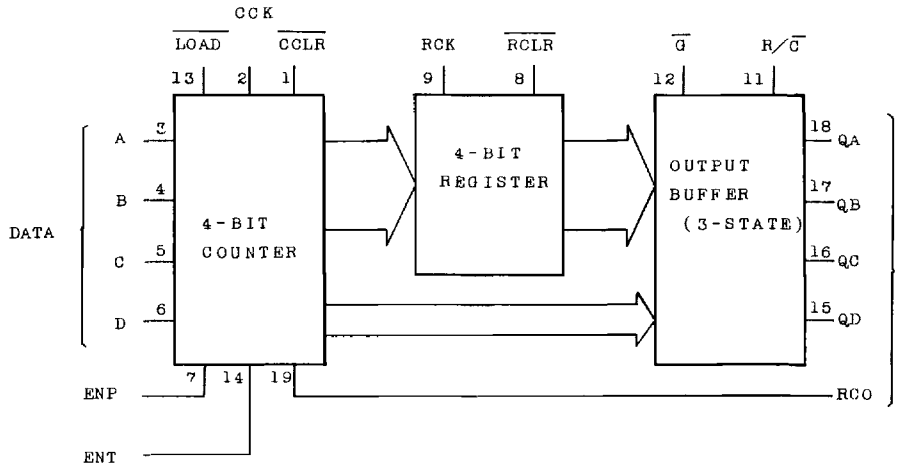
- High Speed ..... f_{MAX}=33MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads (For Q_A ~ Q_D)
  10 LSTTL Loads (For RCO)
- Symmetrical Output Impedance
  $|I_{OH}|=I_{OL}$=6mA(Min.) for Q_A ~ Q_D Output
  $|I_{OH}|=I_{OL}$=4mA(Min.) for RCO Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ~ 6V
- Pin and Function Compatible with LSTTL(74LS690/691)

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM



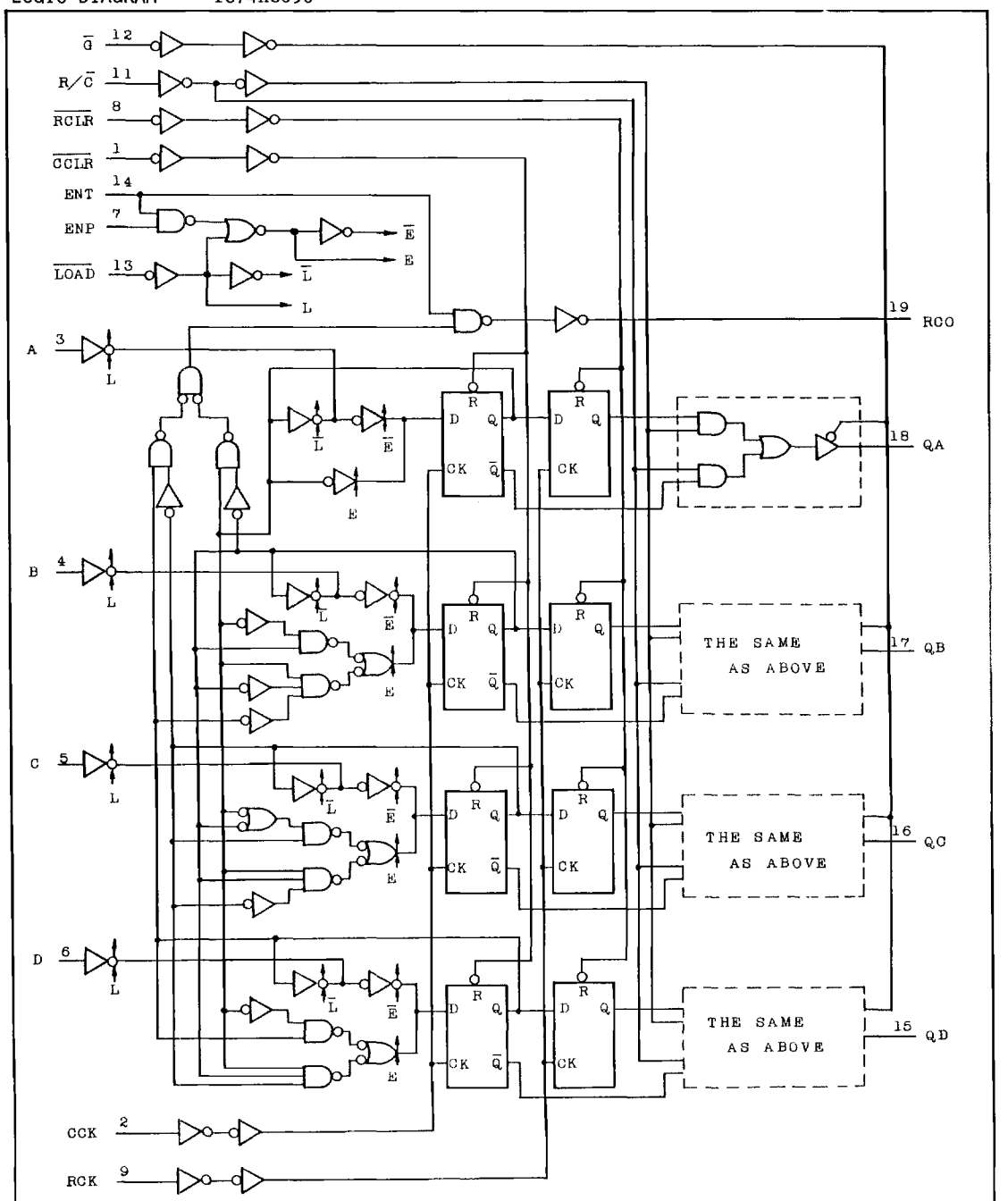
TRUTH TABLE

INPUTS									OUTPUTS				FUUCTION
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	CCK	$\overline{RCLR}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	COUNTER CLEAR
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	↑	X	X	L	L	NO CHANGE				COUNT DISABLE NO CHANGE
H	H	X	L	↑	X	X	L	L					
H	H	H	H	↑	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	X	H	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO CHANGE

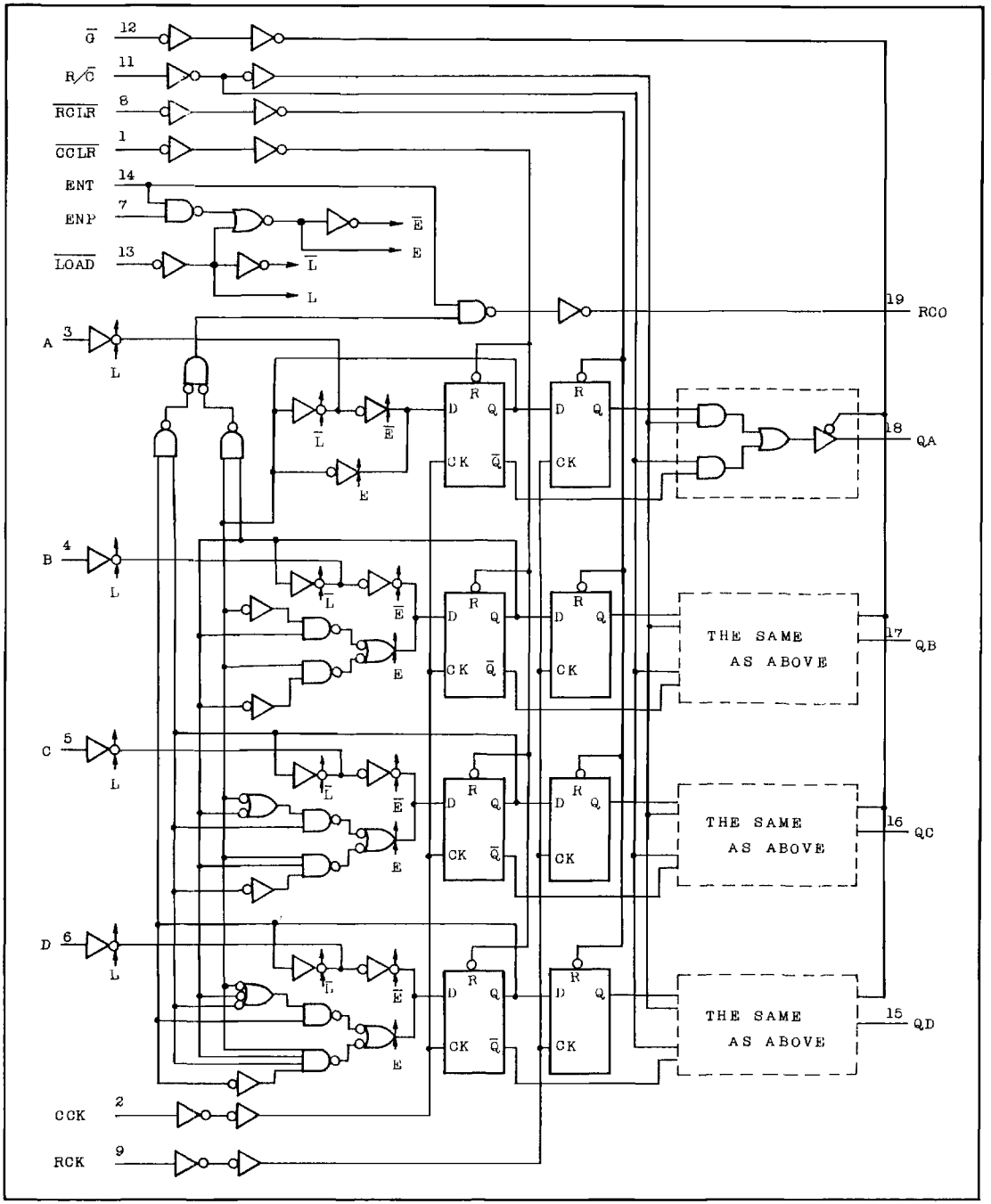
X: Don't Care
Z: High Impedance
a∿d: The level of steady state input voltage at inputs A∿D respectively.
a'∿d': The level of internal counter outputs respectively, before the most recent positive edge of the register clock.

TC74HC690 RCO=QA • QD • ENT
TC74HC691 RCO=QA • QB • QC • QD • ENT

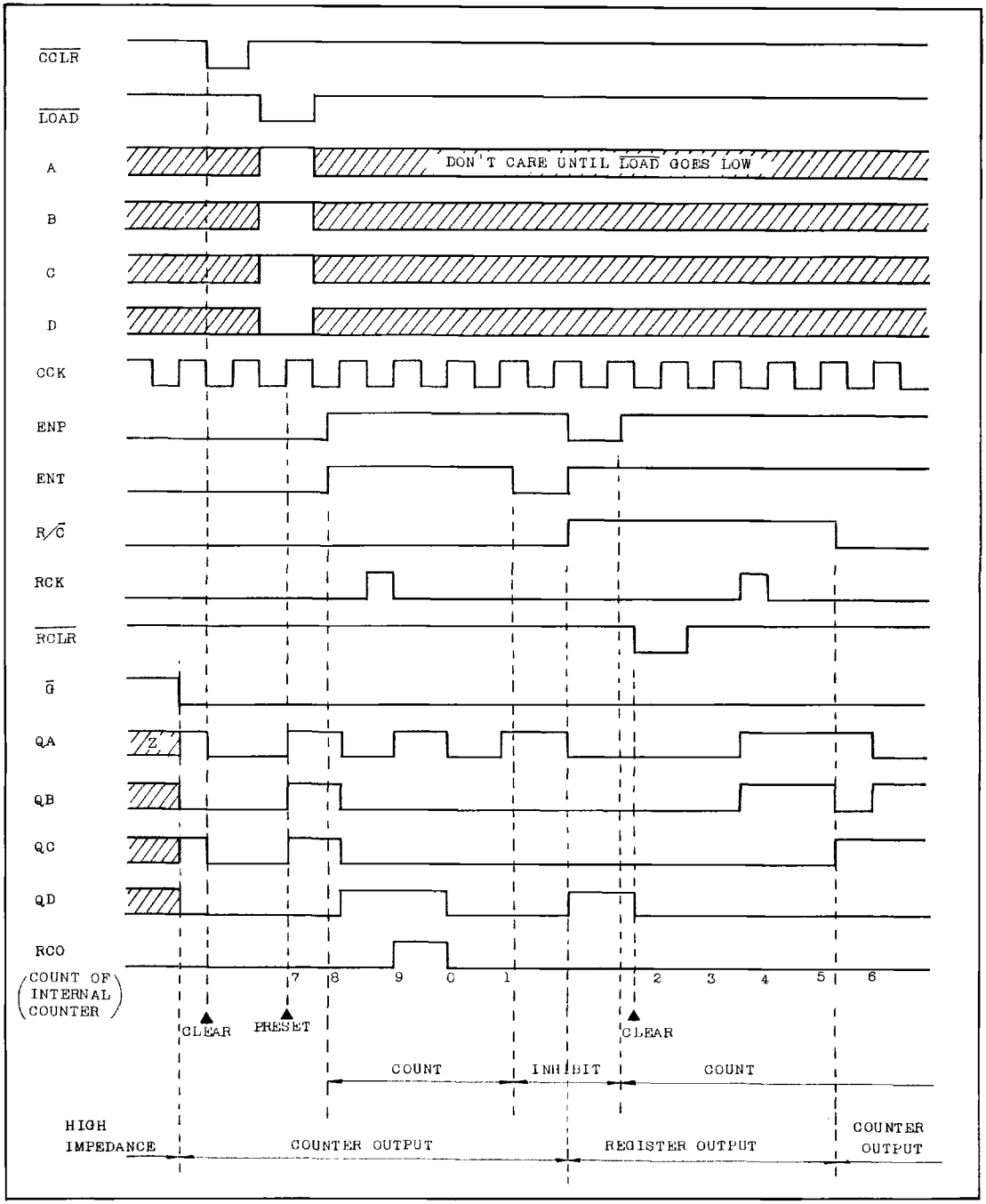
LOGIC DIAGRAM TC74HC690



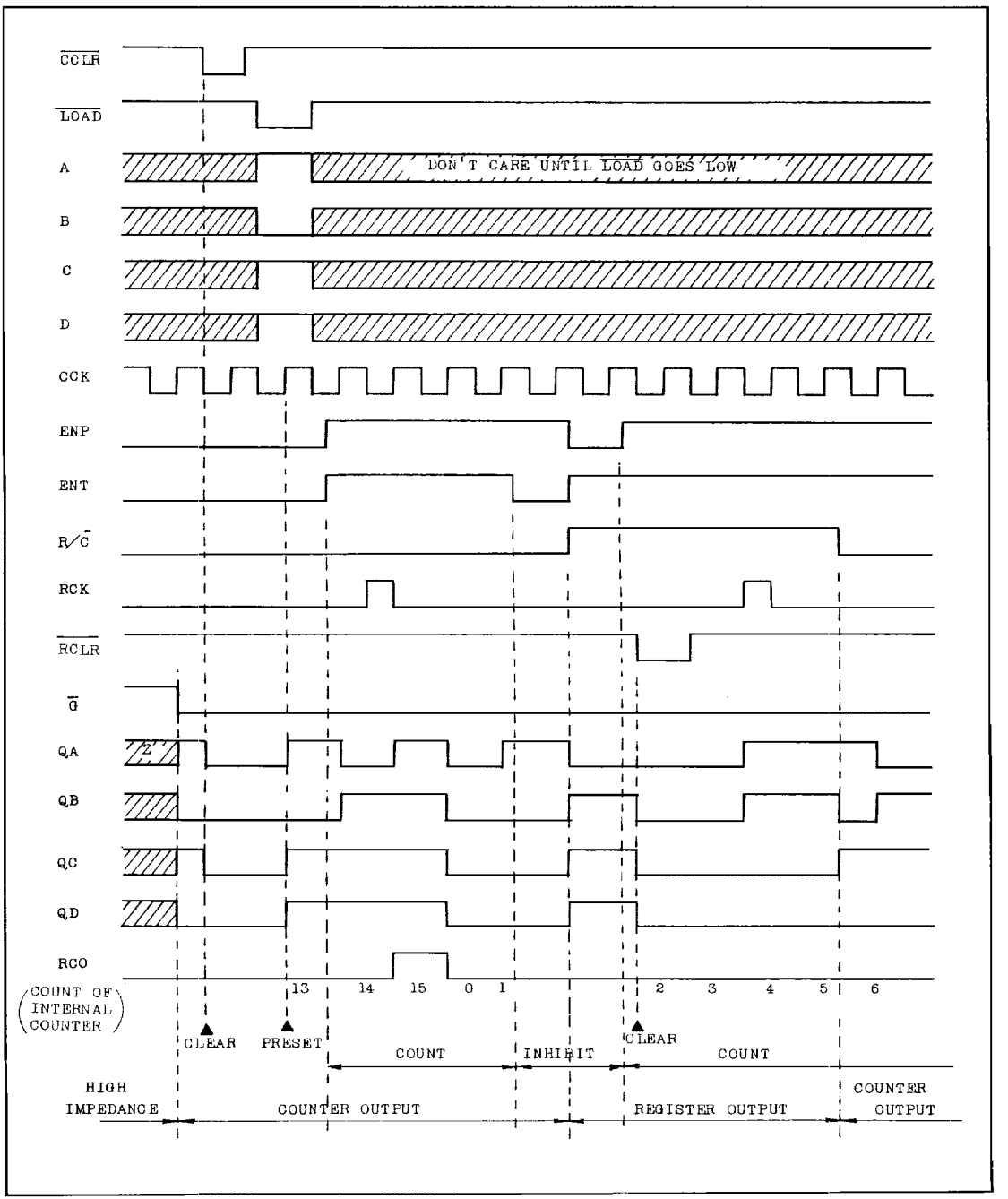
LOGIC DIAGRAM TC74HC691



TIMING CHART TC74HC690

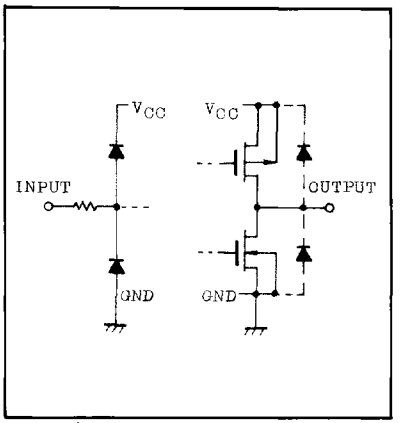


TIMING CHART TC74HC691



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATING	UNIT
Supply Voltage Range		V_{CC}	-0.5 ∿ 7	V
DC Input Voltage		V_{IN}	-0.5 ∿ V_{CC}+0.5	
DC Output Voltage		V_{OUT}	-0.5 ∿ V_{CC}+0.5	
Input Diode Current		I_{IK}	±20	mA
Output Diode Current		I_{OK}	±20	
DC Output Current	(RCO)	I_{OUT}	±25	
	(QA ∿ QD)		±35	
DC V_{CC}/Ground Current		I_{CC}	±70	
Power Dissipation		P_D	500*	mW
Storage Temperature		T_{STG}	-65 ∿ 150	°C
Lead Temperature(10sec)		T_L	300	



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		RCO	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA∿QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		RCO	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Off Leak Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0		40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (RCO)	t_{TLH}		2.0	-	30	75	-	95	
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH}		2.0	-	136	265	-	330	
	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (RCK - Q)	t_{pLH}		2.0	-	148	285	-	355	
	t_{pHL}		4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time (CCK - RCO)	t_{pLH}		2.0	-	128	250	-	315	
	t_{pHL}		4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($R/\overline{C}$ - Q)	t_{pLH}		2.0	-	104	200	-	250	
	t_{pHL}		4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (ENT - RCO)	t_{pLH}		2.0	-	56	110	-	140	
	t_{pHL}		4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	

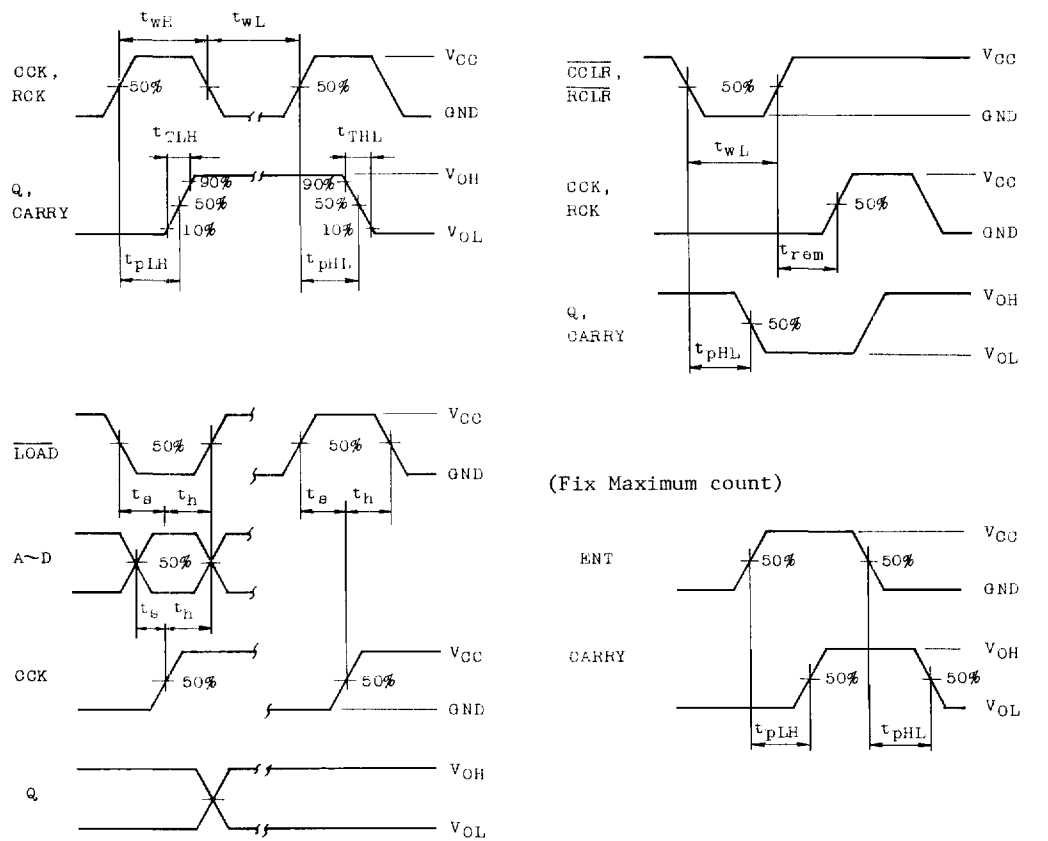
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Propagation Delay Time ($\overline{CCLR}$ - Q)	t_{pHL}		2.0	-	160	305	-	380	ns
			4.5	-	40	61	-	76	
			6.0	-	12	52	-	65	
Propagation Delay Time ($\overline{CCLR}$ - RCO)	t_{pLH}		2.0	-	132	255	-	320	
			4.5	-	33	51	-	64	
			6.0	-	28	44	-	54	
Propagation Delay Time ($\overline{RCLR}$ - Q)	t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{CCLR}$, $\overline{RCLR}$)	$t_{w(L)}$		2.0	-	44	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Removal Time	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Set up Time ($\overline{LOAD}$, ENT, ENP)	t_s		2.0	-	80	175	-	220	
			4.5	-	20	35	-	44	
			6.0	-	17	30	-	37	
Minimum Set up Time (A, B, C, D)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Set up Time (CCK - RCK)	t_s		2.0	-	76	175	-	220	
			4.5	-	19	35	-	44	
			6.0	-	16	30	-	37	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	92	170	-	215	
			4.5	-	23	34	-	43	
			6.0	-	20	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	80	-	-	-	

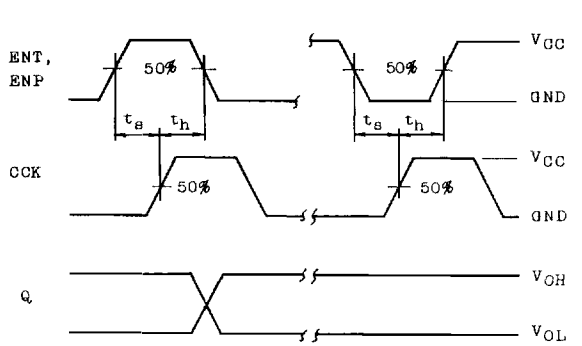
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

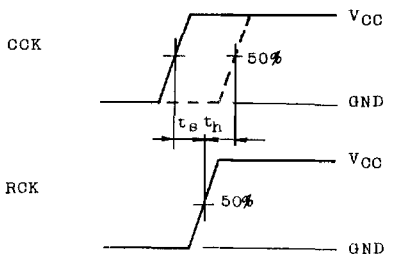
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

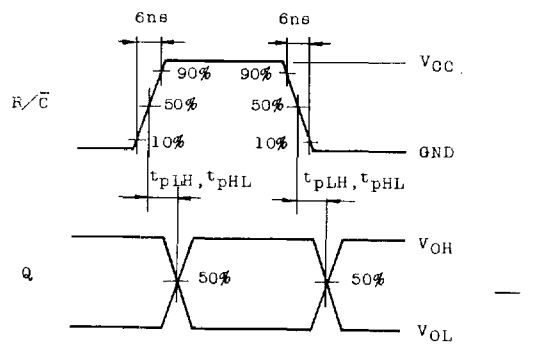
SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 1)



SWITCHING CHARACTERISTICS TEST WAVEFORM (Part 2)

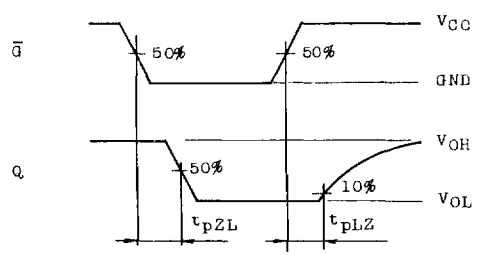






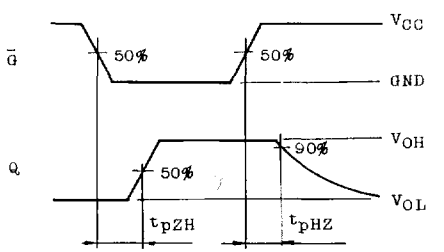
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{G}$ input is held low.



t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{G}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{G}$ input is held low.



I_{CC}(Opr.) TEST WAVEFORM