QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- **Gated input enable for hold (do nothing) mode**
- **Gated output enable control**
- **Edge-triggered D-type register**
- **Asynchronous master reset**
- **Output capability: bus driver**
- **I_{CC} category: MSI**

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two data enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the data on the D_n inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}_n$ inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ($\overline{OE}_1$ and $\overline{OE}_2$) are LOW, the data in the register is presented to the Q_n outputs. When one or both $\overline{OE}_n$ inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}_n$ transition does not affect the clock and reset operations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n	$C_L = 15$ pF; $V_{CC} = 5$ V	17	17	ns
	MR to Q_n		13	17	ns
f_{max}	maximum clock frequency		88	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\,(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma\,(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to $V_{CC} - 1.5$ V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q_0 to Q_3	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1$, $\overline{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	D_0 to D_3	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V_{CC}	positive supply voltage

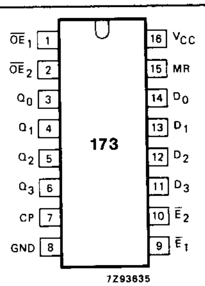

Fig. 1 Pin configuration.

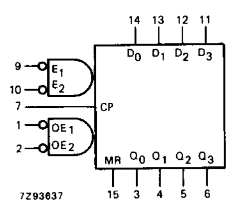

Fig. 2 Logic symbol.

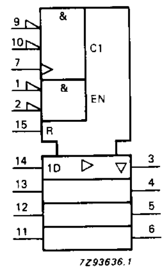

Fig. 3 IEC logic symbol.

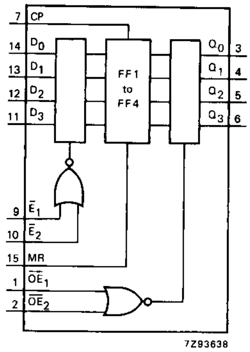

Fig. 4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (register)
reset (clear)	H	X	X	X	X	L
parallel load	L L	↑ ↑	l l	l l	l h	L H
hold (no change)	L L	X X	h X	X h	X X	q_n q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q_n (register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0	Q_1	Q_2	Q_3
read	L H	L L	L L	L H	L H	L H	L H
disabled	X X	H X	X H	Z Z	Z Z	Z Z	Z Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

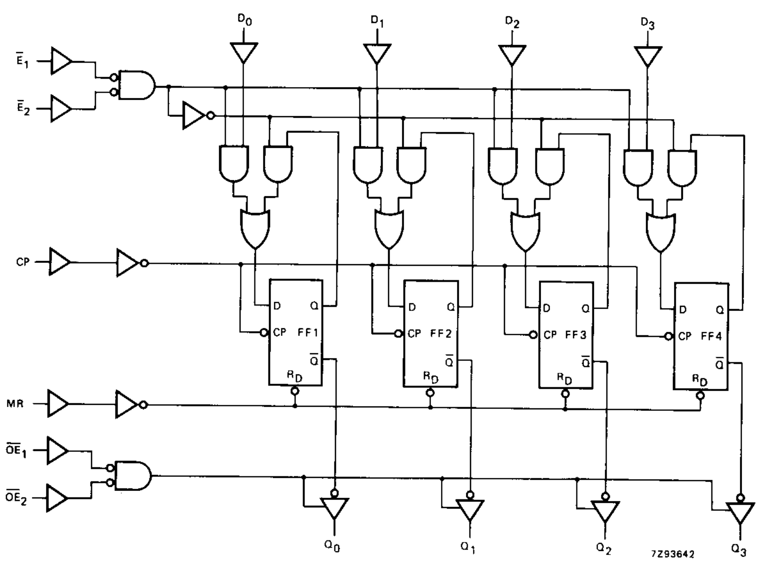

Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	V_{CC} V	WAVEFORMS
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}	propagation delay MR to Q_n		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 8
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	master reset pulse width; HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time MR to CP	60 12 10	−8 −3 −2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time $\overline{E}_n$ to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 9
t_{su}	set-up time D_n to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time $\overline{E}_n$ to CP	0 0 0	−17 −6 −5		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 9
t_h	hold time D_n to CP	1 1 1	−11 −4 −3		1 1 1		1 1 1		ns	2.0 4.5 6.0	Fig. 9
f_{max}	maximum clock pulse frequency	6.0 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1$, $\overline{OE}_2$	0.50
MR	0.60
$\overline{E}_1$, $\overline{E}_2$	0.40
D_n	0.25
CP	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	TEST CONDITIONS V_{CC} V	WAVEFORMS
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		20	40		50		60	ns	4.5	Fig. 6
t_{PHL}	propagation delay MR to Q_n		20	37		46		56	ns	4.5	Fig. 7
t_{PZH}/ t_{PZL}	3-state output enable time $\overline{OE}_n$ to Q_n		20	35		44		53	ns	4.5	Fig. 8
t_{PHZ}/ t_{PLZ}	3-state output disable time $\overline{OE}_n$ to Q_n		19	30		38		45	ns	4.5	Fig. 8
t_{THL}/ t_{TLH}	output transition time		5	12		15		19	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 6
t_W	master reset pulse width; HIGH	15	6		19		22		ns	4.5	Fig. 7
t_{rem}	removal time MR to CP	12	−2		15		18		ns	4.5	Fig. 7
t_{su}	set-up time $\overline{E}_n$ to CP	22	13		28		33		ns	4.5	Fig. 9
t_{su}	set-up time D_n to CP	12	7		15		18		ns	4.5	Fig. 9
t_h	hold time $\overline{E}_n$ to CP	0	−6		0		0		ns	4.5	Fig. 9
t_h	hold time D_n to CP	0	−3		0		0		ns	4.5	Fig. 9
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig. 6

AC WAVEFORMS

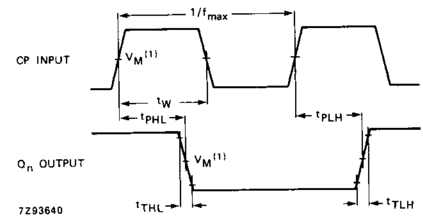

Fig. 6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency.

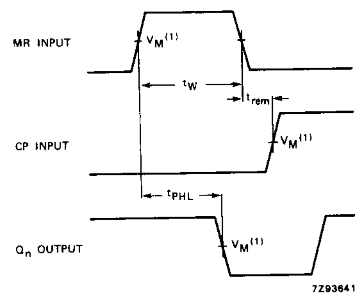

Fig. 7 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

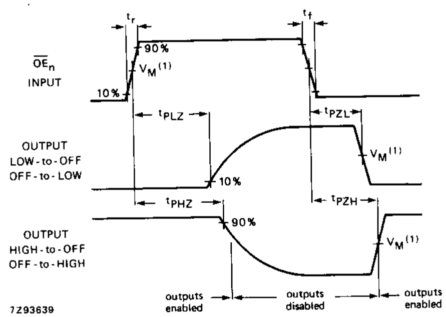

Fig. 8 Waveforms showing the 3-state enable and disable times.

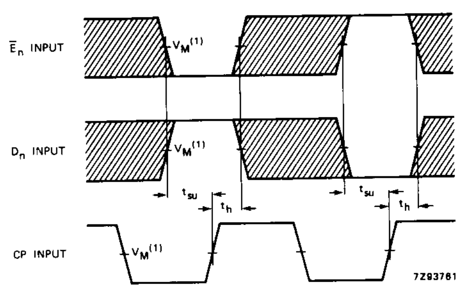

Fig. 9 Waveforms showing the data set-up and hold times from input ($\overline{E}_n$, D_n) to clock (CP).

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC}.
HCT: $V_M = 1.3\ V$; $V_I = GND$ to $3\ V$.

Note to Fig. 9

The shaded areas indicate when the input is permitted to change for predictable output performance.