National Semiconductor

August 1995

74F675A
16-Bit Serial-In, Serial/Parallel-Out Shift Register

General Description

The 'F675A contains a 16-bit serial in/serial out shift register and a 16-bit parallel out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

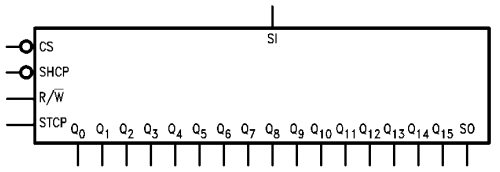
Features

- Serial-to-parallel converter
- 16-Bit serial I/O shift register
- 16-Bit parallel out storage register
- Recirculating parallel transfer
- Expandable for longer words
- Slim 24 lead package
- 'F675A version prevents false clocking through $\overline{CS}$ or R/$\overline{W}$ inputs

Commercial	Package Number	Package Description
74F675ASPC	N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
74F675APC	N24A	24-Lead (0.600″ Wide) Molded Dual-In-Line
74F675ASC (Note 1)	M24B	24-Lead (0.300″ Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Logic Symbols



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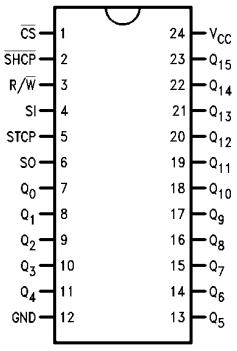
Connection Diagram

Pin Assignment for DIP and SOIC



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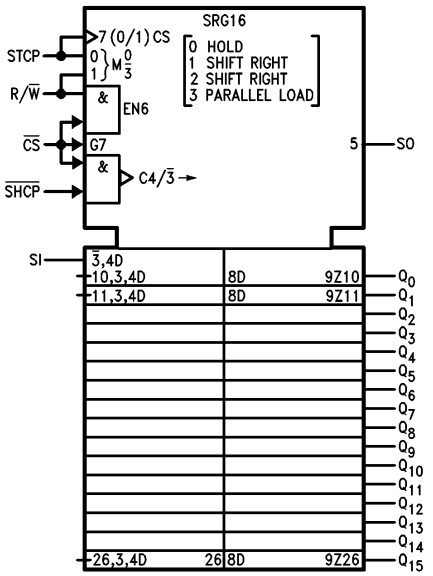
Logic Symbols (Continued)

IEEE/IEC



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Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
SI	Serial Data Input	1.0/1.0	20 μA/−0.6 mA
$\overline{CS}$	Chip Select Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	1.0/1.0	20 μA/−0.6 mA
STCP	Store Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
R/$\overline{W}$	Read/Write Input	1.0/1.0	20 μA/−0.6 mA
SO	Serial Data Output	50/33.3	−1 mA/20 mA
Q_0–Q_{15}	Parallel Data Outputs	50/33.3	−1 mA/20 mA

Functional Description

The 16-Bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift Right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

Shift Register Operations Table

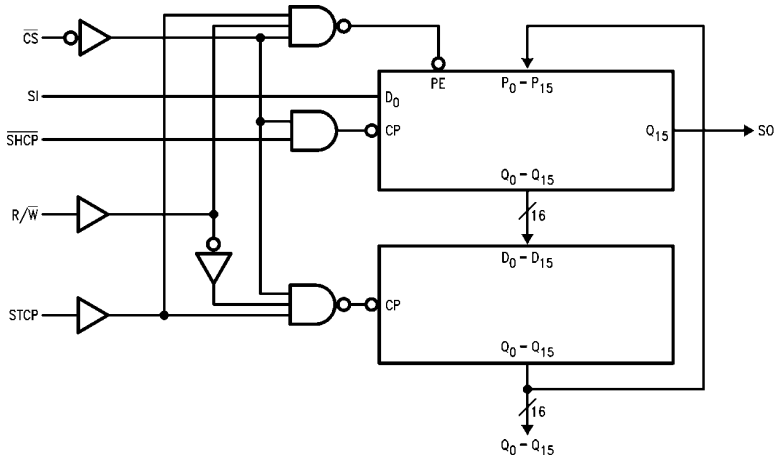
Control Inputs				Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↘	X	Shift Right
L	H	↘	L	Shift Right
L	H	↘	H	Parallel Load, No Shifting

Storage Register Operations Table

Inputs			Operating Mode
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↗	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition
↘ = HIGH-to-LOW Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCH}	Power Supply Current			106	160	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			106	160	mA	Max	V_O = LOW

AC Electrical Characteristics

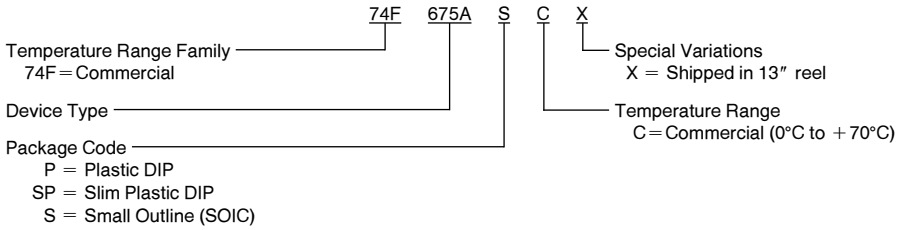
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	130		85		MHz
t_{PLH} t_{PHL}	Propagation Delay STCP to Q_n	3.0 3.0	8.0 10.5	10.5 13.5	2.5 2.5	12.0 15.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{SHCP}$ to SO	4.0 4.5	7.0 8.0	9.5 10.5	3.5 4.0	10.5 12.0	ns

AC Operating Requirements

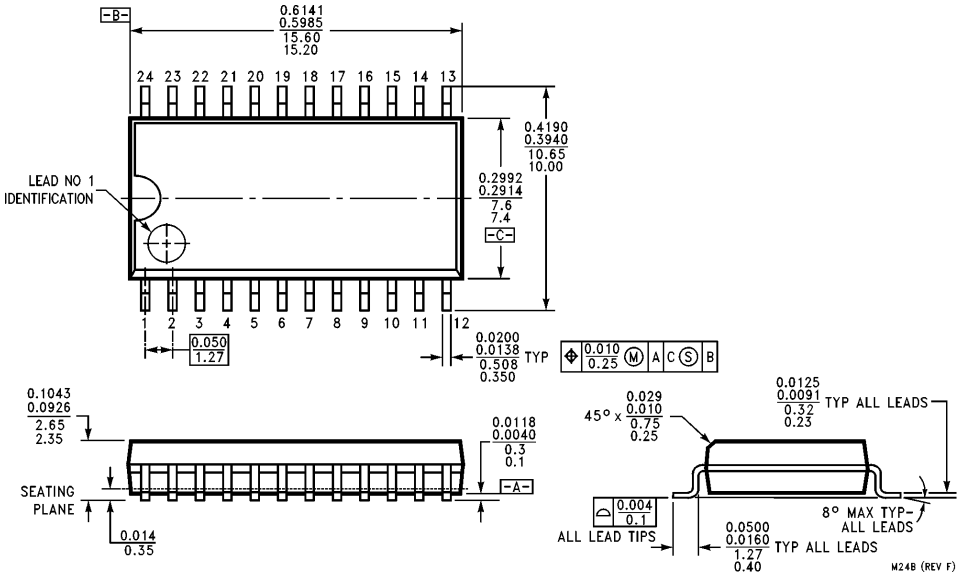
Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	3.5 5.5		4.0 6.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.5 3.5		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	6.5 9.0		7.5 10.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STCP to $\overline{SHCP}$	7.0 7.0		8.0 8.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STCP to $\overline{SHCP}$	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CS}$ to $\overline{SHCP}$	3.0 3.0		3.5 3.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CS}$ to $\overline{SHCP}$	3.0 3.0		3.5 3.5		
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ Pulse Width HIGH or LOW	5.0 5.0		6.0 6.0		ns
$t_w(H)$ $t_w(L)$	STCP Pulse Width HIGH or LOW	6.0 5.0		7.0 6.0		
$t_s(L)$	$\overline{SHCP}$ to STCP	8.0		9.0		ns
$t_h(H)$	$\overline{SHCP}$ to STCP	0.0		0.0		ns

Ordering Information

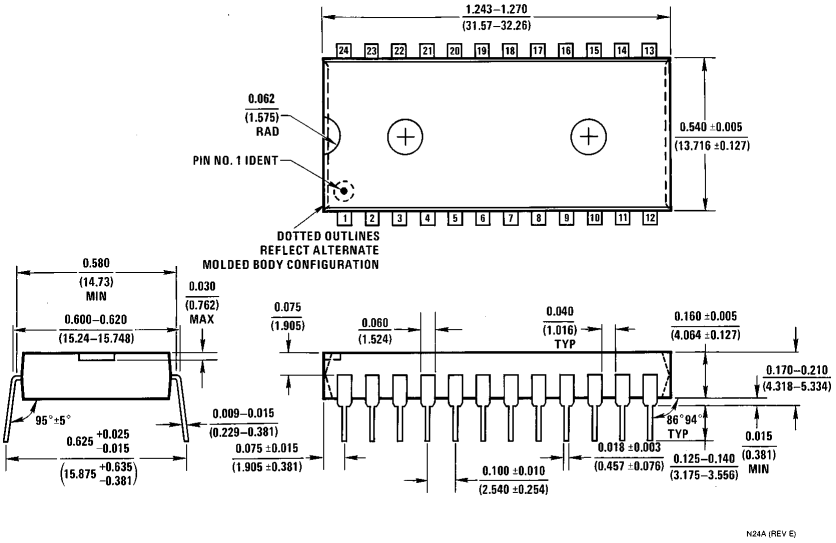
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

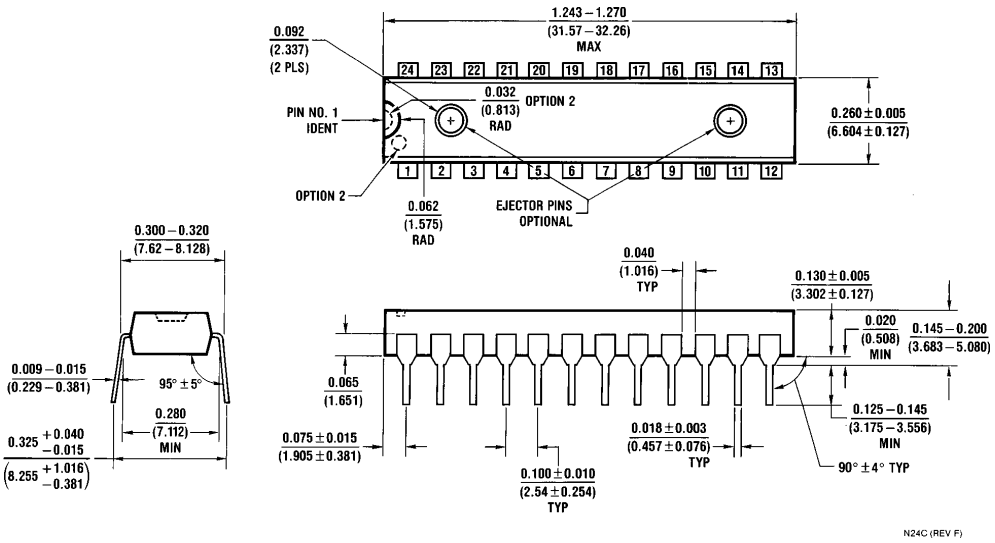


24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B



24-Lead (0.600″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N24A

Physical Dimensions inches (millimeters) (Continued)



24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

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