National Semiconductor

August 1995

74F640 • 74F645
Octal Bus Transceiver with TRI-STATE® Outputs

General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA, have TRI-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive ($T/\overline{R}$) input. The ’F645 is a high speed/low power version of the ’F245. The ’F640 is an inverting option of the ’F645.

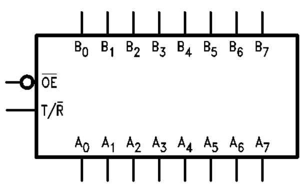
Features

- Designed for asynchronous two-way data flow between busses
- Outputs sink 64 mA
- Transmit/receive ($T/\overline{R}$) input controls the direction of data flow
- Guaranteed 4000V minimum ESD protection
- ’F645 is a lower power, faster version of the ’F245
- ’F640 is an inverting option of the ’F645

Commercial	Package Number	Package Description
74F640PC	N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
74F640SC (Note 1)	M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F645PC	N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

Logic Symbol



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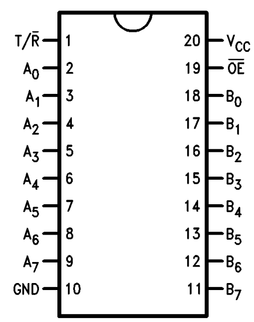
Connection Diagram

Pin Assignment for DIP and SOIC



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Unit Loading/Fan Out

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/1.0	20 μA/−0.6 mA
A_0–A_7	Side A Inputs or	3.5/0.667	70 μA/−0.4 mA
	TRI-STATE Outputs	600/106.6	−12 mA/64 mA
B_0–B_7	Side B Inputs or	3.5/0.667	70 μA/−0.4 mA
	TRI-STATE Outputs	600/106.6	−12 mA/64 mA

RRD-B30M115/Printed in U. S. A.

Functional Description

The output enable ($\overline{OE}$) is active LOW. If the device is disabled ($\overline{OE}$ HIGH), the outputs are in the high impedance state. The transmit/receive input (T/$\overline{R}$) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When T/$\overline{R}$ is LOW, B data is sent to the A bus. If T/$\overline{R}$ is HIGH, A data is sent to the B bus.

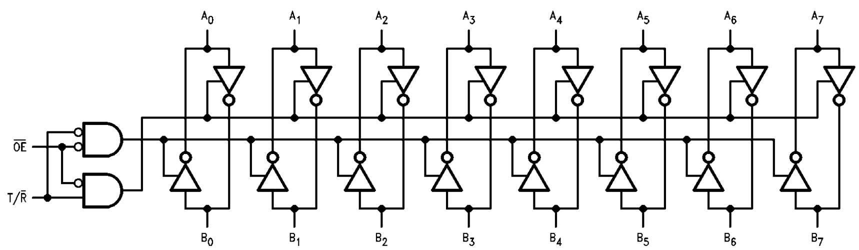
Function Table

Inputs		Outputs	
$\overline{OE}$	T/$\overline{R}$	'F640	'F645
L	L	Bus $\overline{B}$ data to Bus A	Bus B data to Bus A
L	H	Bus $\overline{A}$ data to Bus B	Bus A data to Bus B
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

Logic Diagrams

'F640



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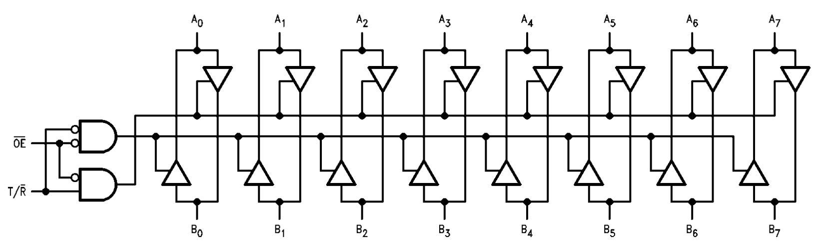
'F645



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F Min	74F Typ	74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.0			V	Min	I_{OH} = −15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown (I/O)	74F			0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Pins)
$I_{IH} + I_{OZH}$	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
$I_{IL} + I_{OZL}$	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25
I_{CCH}	Power Supply Current ('F640)				80	mA	Max	V_O = HIGH, V_{IN} = 0.2V
I_{CCL}	Power Supply Current ('F640)				80	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F640)				96	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current ('F645)				65	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F645)				80	mA	Max	V_O = LOW, V_{IN} = 0.2V
I_{CCZ}	Power Supply Current ('F645)				90	mA	Max	V_O = HIGH Z

’F640 AC Electrical Characteristics:

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output	2.5 2.0		7.5 7.0	2.0 2.0	8.0 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output	2.5 2.0		7.5 7.0	2.0 2.0	8.0 7.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		7.5 8.0	2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to A Output	1.5 1.5		7.0 6.0	1.0 1.5	7.5 6.0	
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.0	2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to B Output	1.5 1.5		7.0 6.0	1.0 1.5	7.5 6.0	

’F645 AC Electrical Characteristics:

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output	1.5 2.0		6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output	1.5 2.0		6.0 7.0	1.5 2.0	7.0 7.5	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		8.0 8.5	2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to A Output	1.5 1.0		7.0 5.5	1.0 1.0	8.0 5.5	
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.5	2.0 2.5	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to B Output	1.5 1.0		6.5 5.5	1.0 1.0	7.5 5.5	

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

74F 640 S C X

Temperature Range Family
74F = Commercial

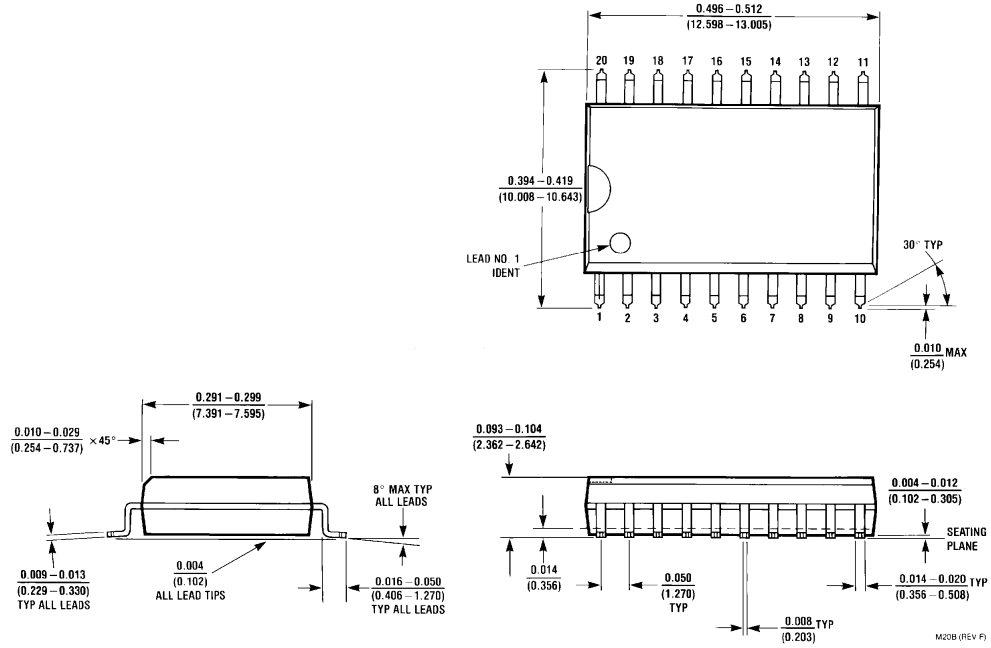
Device Type

Package Code
P = Plastic DIP
S = Small Outline (SOIC)

Special Variations
X = Devices shipped in 13″ reels

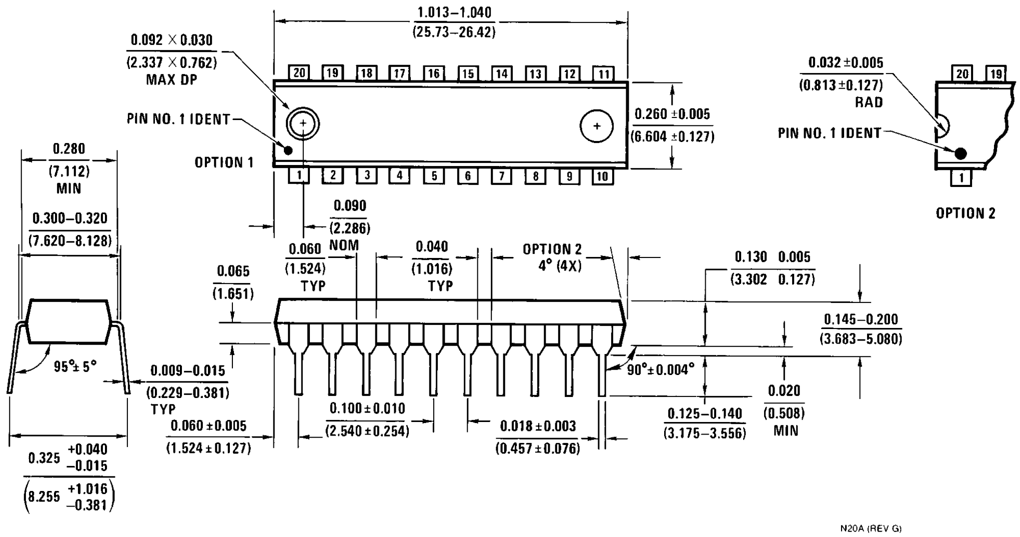
Temperature Range
C = Commercial (0°C to +70°C)

Physical Dimensions inches (millimeters)



20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

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