FAST 74F548
Decoder/Demultiplexer

Octal Decoder/Demultiplexer with Acknowledge
Product Specification

FAST Products

FEATURES

- **3- to 8-line address decoder**
- **Multiple enables for address extension**
- **Open-Collector Acknowledge output**
- **Active-Low Decoder outputs**

DESCRIPTION

The 'F548 is a 3- to 8-line address decoder with four Enable inputs. Two of the Enables are active-Low and two are active-High for maximum addressing versatility. Also provided is an active-Low Acknowledge output that responds to either a Read or Write input signal when the Enables are active.

When enabled, the 'F548 accepts the $A_0 - A_2$ address inputs and decodes them to select one of eight active-Low mutually exclusive outputs, as shown in the Decoder Function Table. When one or more Enables is active, all decoder outputs are High. Thus, the 'F548 can be used as a demultiplexer by applying data to one of the Enables.

The Open-Collector Acknowledge ($\overline{ACK}$) output is normally High (i.e. OFF) and goes Low when the Enables are all active and either the READ ($\overline{RD}$) or Write ($\overline{WR}$) input is Low, as indicated in the Acknowledge Function Table.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F548	6.5ns	14mA

ORDERING INFORMATION

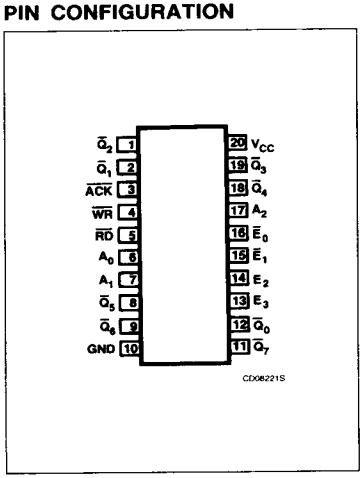
PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ± 10%; T_A = 0°C to +70°C
20-Pin Plastic DIP	N74F548N
20-Pin Plastic SOL	N74F548D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

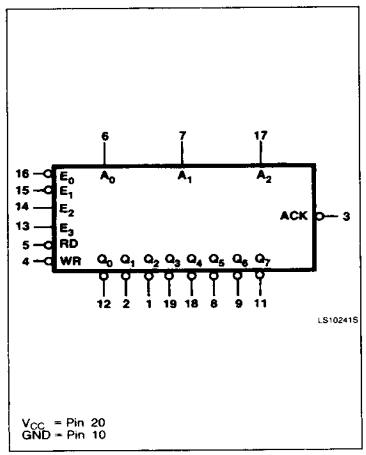
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_2$	Output select address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Chip enable inputs (active-Low)	1.0/1.0	20μA/0.6mA
E_2, E_3	Chip enable inputs	1.0/1.0	20μA/0.6mA
$\overline{RD}$	Read acknowledge input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{WR}$	Write acknowledge input (active-Low)	1.0/1.0	20μA/0.6mA
$\overline{Q}_0 - \overline{Q}_7$	Decoder outputs (active-Low)	50/33	1mA/20mA
ACK	Open-collector acknowledge output (active-Low)	OC*/33	OC*/20mA

NOTES:
1. One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
2. *OC = Open-Collector.

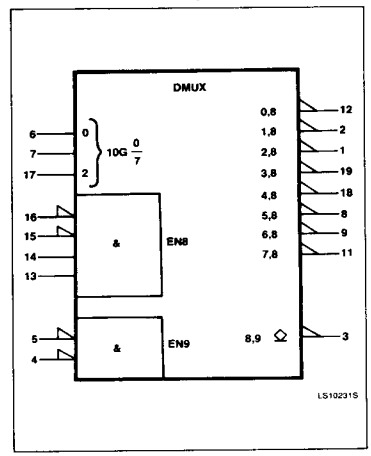
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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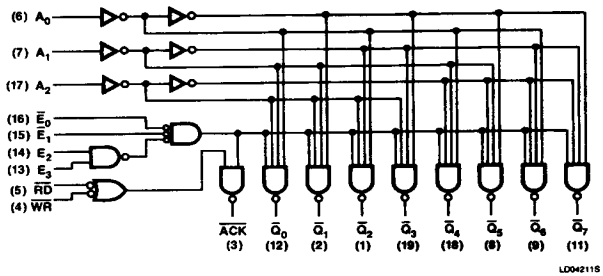
Decoder/Demultiplexer

FAST 74F548

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

FUNCTION TABLE (Decoder)

INPUTS							OUTPUTS							
$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$
H	X	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	X	H	H	H	H	H	H	H	H
X	X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE (Acknowledge)

INPUTS						OUTPUT
$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	H	H	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	High-level output voltage	$\overline{ACK}$ only			4.5	V
I_{OH}	High-level output current	Except $\overline{ACK}$			−1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	$\overline{ACK}$ only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = MAX				250	μA
V_{OH}	High-level output voltage	Except $\overline{ACK}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX	±10%V_{CC}	2.5			V
				±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
				±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	Except $\overline{ACK}$	V_{CC} = MAX		−60		−150	mA
I_{CC}	Supply current (total)		V_{CC} = MAX			14	21	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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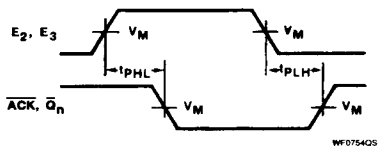
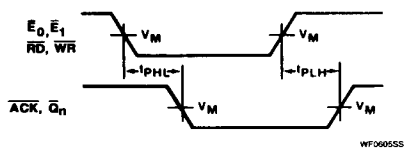
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	74F548					UNIT
			$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Q}_n$	Waveform 3	2.0 4.0	4.5 6.5	8.0 9.5	1.5 4.0	9.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{Q}_n$	Waveform 2	2.5 3.5	4.5 5.5	8.5 8.5	2.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to $\overline{Q}_n$	Waveform 1	4.0 4.0	6.0 6.0	9.5 9.5	3.0 3.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to $\overline{ACK}$	Waveform 1	6.5 3.0	9.5 6.0	12.5 9.5	6.5 3.0	13.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay E_2 or E_3 to $\overline{ACK}$	Waveform 1	8.0 4.0	11.0 7.0	14.0 10.0	8.0 4.0	15.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{RD}$ or $\overline{WR}$ to $\overline{ACK}$	Waveform 2	5.5 2.5	9.0 5.0	12.0 8.0	5.5 2.5	12.5 8.5	ns

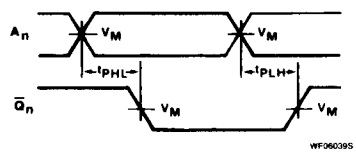
AC WAVEFORMS



Waveform 1. Propagation Delay for Chip Enable Inputs (E_3, E_4) to Write Acknowledge ($\overline{ACK}$) and Decoder (Q_n) Outputs



Waveform 2. Propagation Delay for Chip Enable Inputs ($\overline{E}_1$, $\overline{E}_2$) to Decoder Outputs ($\overline{Q}_n$) and Write Acknowledge Output ($\overline{ACK}$)



Waveform 3. Propagation Delays for Output Select Address Input (A_n) to Decoder Outputs ($\overline{Q}_n$)

NOTE: For all waveforms, $V_M = 1.5V$.

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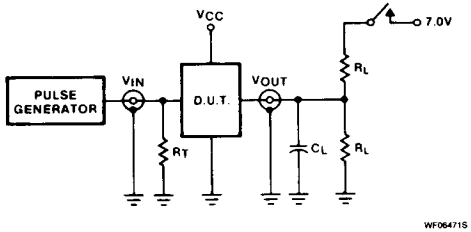
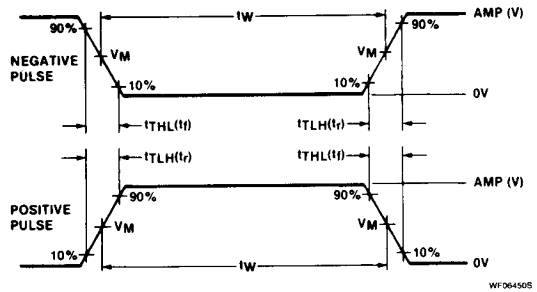
TEST CIRCUIT AND WAVEFORMS



Test Circuit for Open-Collector and Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
Open-Collector Totem-pole	closed open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

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