National Semiconductor

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# 74F350
# 4-Bit Shifter with TRI-STATE® Outputs

## General Description

The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select ($S_0$, $S_1$) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the TRI-STATE outputs of different packages and using the Output Enable ($\overline{OE}$) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions.

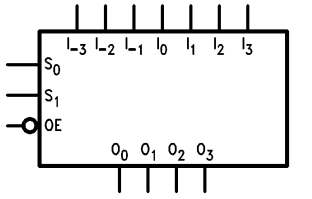
## Features

- Linking inputs for word expansion
- TRI-STATE outputs for extending shift range

| Commercial | Package Number | Package Description |
|---|---|---|
| 74F350PC | N16E | 16-Lead (0.300″ Wide) Molded Dual-In-Line |
| 74F350SC (Note 1) | M16A | 16-Lead (0.150″ Wide) Molded Small Outline, JEDEC |
| 74F350SJ (Note 1) | M16D | 16-Lead (0.300″ Wide) Molded Small Outline, EIAJ |

**Note 1:** Devices also available in 13″ reel. Use suffix = SCX and SJX.

## Logic Symbols

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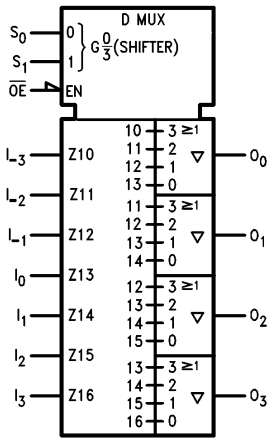
IEEE/IEC

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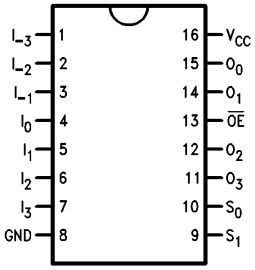
## Connection Diagram

Pin Assignment for DIP and SOIC

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RRD-B30M105/Printed in U. S. A.

## Unit Loading/Fan Out

| Pin Names | Description | 74F | |
|---|---|---|---|
| | | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
| $S_0$, $S_1$ | Select Inputs | 1.0/2.0 | 20 $\mu$A/ $-$1.2 mA |
| $I_{-3}$–$I_3$ | Data Inputs | 1.0/2.0 | 20 $\mu$A/ $-$1.2 mA |
| $\overline{OE}$ | Output Enable Input (Active LOW) | 1.0/2.0 | 20 $\mu$A/ $-$1.2 mA |
| $O_0$–$O_3$ | TRI-STATE Outputs | 150/40 (33.3) | $-$3 mA/24 mA (20 mA) |

## Functional Description

The 'F350 is operationally equivalent to a 4-input multiplexer with the inputs connected so that the select code causes successive one-bit shifts of the data word. This internal connection makes it possible to perform shifts of 0, 1, 2 or 3 places on words of any length.

A 4-bit data word is introduced at the $I_n$ inputs and is shifted according to the code applied to the select inputs $S_0$, $S_1$. Outputs $O_0$–$O_3$ are TRI-STATE, controlled by an active LOW output enable ($\overline{OE}$). When $\overline{OE}$ is LOW, data outputs will follow selected data inputs; when HIGH, the data outputs will be forced to the high impedance state. This feature allows shifters to be cascaded on the same output lines or to a common bus. The shift function can be logical, with zeros pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

## Logic Equations

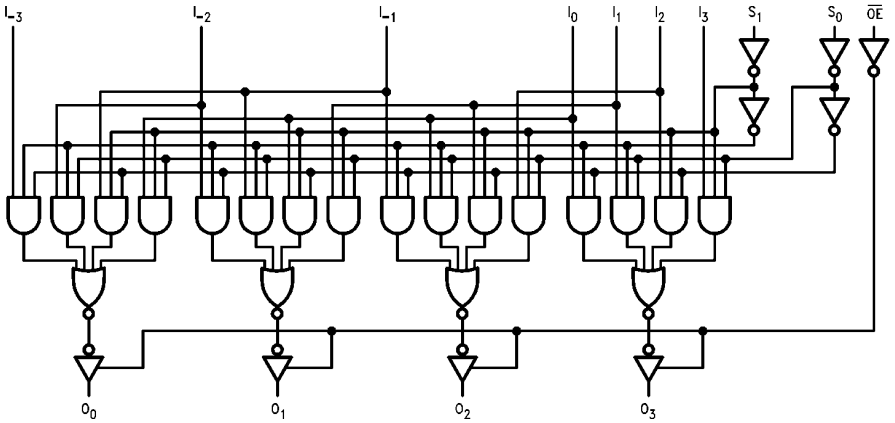
$$O_0 = \overline{S}_0\overline{S}_1I_0 + S_0\overline{S}_1I_{-1} + \overline{S}_0S_1I_{-2} + S_0S_1I_{-3}$$
$$O_1 = \overline{S}_0\overline{S}_1I_1 + S_0\overline{S}_1I_0 + \overline{S}_0S_1I_{-1} + S_0S_1I_{-2}$$
$$O_2 = \overline{S}_0\overline{S}_1I_2 + S_0\overline{S}_1I_1 + \overline{S}_0S_1I_0 + S_0S_1I_{-1}$$
$$O_3 = \overline{S}_0\overline{S}_1I_3 + S_0\overline{S}_1I_2 + \overline{S}_0S_1I_1 + S_0S_1I_0$$

## Truth Table

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | $S_1$ | $S_0$ | $O_0$ | $O_1$ | $O_2$ | $O_3$ |
| H | X | X | Z | Z | Z | Z |
| L | L | L | $I_0$ | $I_1$ | $I_2$ | $I_3$ |
| L | L | H | $I_{-1}$ | $I_0$ | $I_1$ | $I_2$ |
| L | H | L | $I_{-2}$ | $I_{-1}$ | $I_0$ | $I_1$ |
| L | H | H | $I_{-3}$ | $I_{-2}$ | $I_{-1}$ | $I_0$ |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

## Logic Diagram

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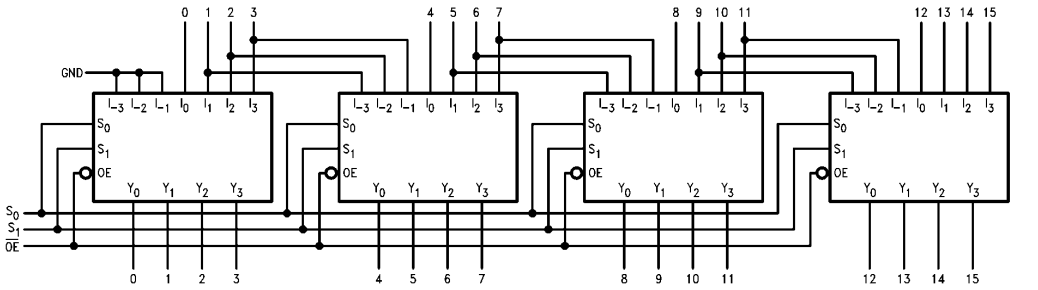
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Applications

**16-Bit Shift-Up 0 to 3 Places, Zero Backfill**

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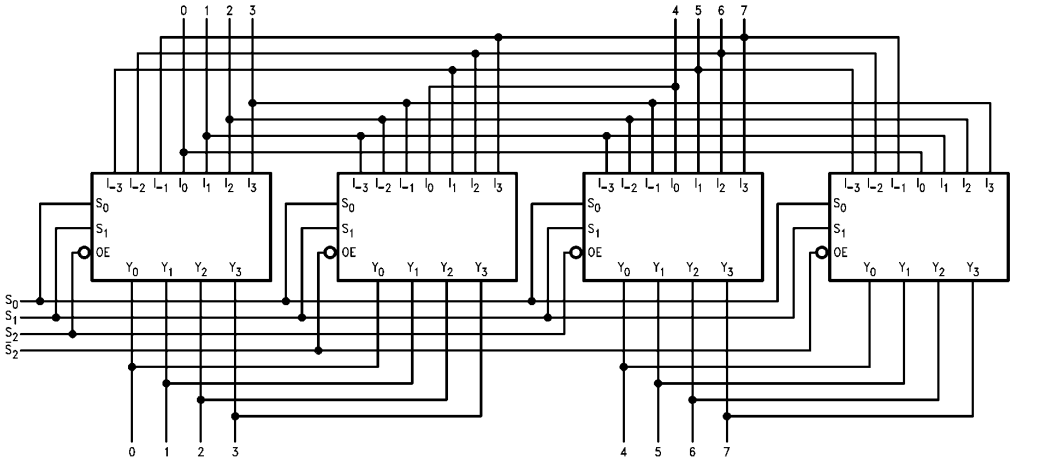
**Function Table**

| $S_1$ | $S_0$ | Shift Function |
|---|---|---|
| L | L | No Shift |
| L | H | Shift 1 Place |
| H | L | Shift 2 Places |
| H | H | Shift 3 Places |

**8-Bit End Around Shift 0 to 7 Places**

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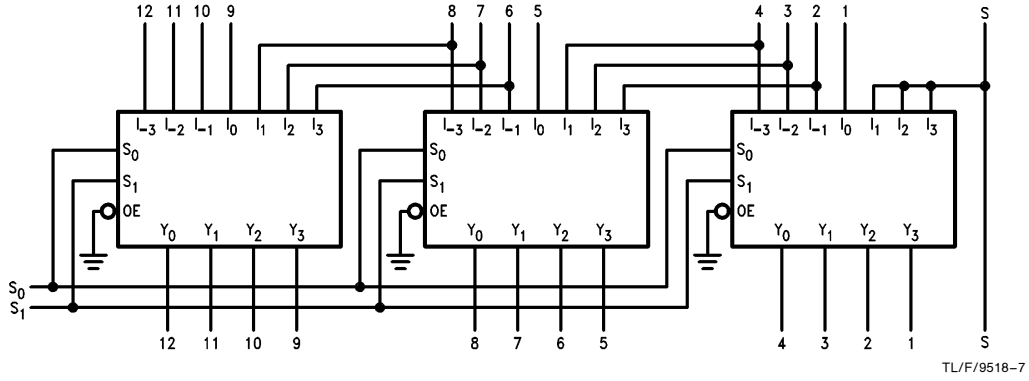
## Applications (Continued)

**Function Table**

| $S_2$ | $S_1$ | $S_0$ | Shift Function |
|---|---|---|---|
| L | L | L | No Shift |
| L | L | H | Shift End Around 1 |
| L | H | L | Shift End Around 2 |
| L | H | H | Shift End Around 3 |
| H | L | L | Shift End Around 4 |
| H | L | H | Shift End Around 5 |
| H | H | L | Shift End Around 6 |
| H | H | H | Shift End Around 7 |

**13-Bit Twos Complement Scaler**

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**Function Table**

| $S_1$ | $S_0$ | Scale |
|---|---|---|
| L | L ÷ 8 | ⅛ |
| L | H ÷ 4 | ¼ |
| H | L ÷ 2 | ½ |
| H | H No Change | 1 |

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +175°C |
| Plastic | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| TRI-STATE Output | −0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Commercial | +4.5V to +5.5V |

## DC Electrical Characteristics

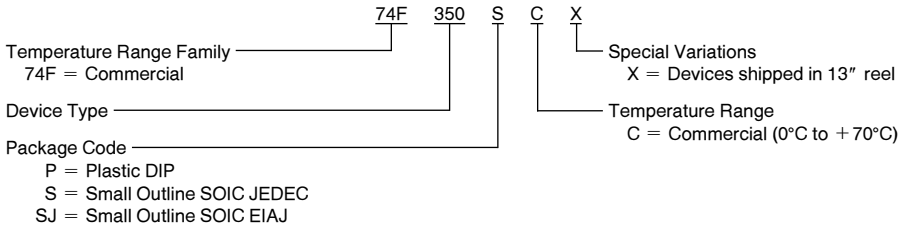
| Symbol | Parameter | | 74F | | | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | | |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 74F 10% $V_{CC}$ | 2.5 | | | V | Min | $I_{OH}$ = −1 mA |
| | | 74F 10% $V_{CC}$ | 2.4 | | | | | $I_{OH}$ = −3 mA |
| | | 74F 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −1 mA |
| | | 74F 10% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −3 mA |
| $V_{OL}$ | Output LOW Voltage | 74F 10% $V_{CC}$ | | | 0.5 | V | Min | $I_{OL}$ = 24 mA |
| $I_{IH}$ | Input HIGH Current | 74F | | | 5.0 | μA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | 74F | | | 7.0 | μA | Max | $V_{IN}$ = 7.0V |
| $I_{CEX}$ | Output HIGH Leakage Current | 74F | | | 50 | μA | Max | $V_{OUT}$ = $V_{CC}$ |
| $V_{ID}$ | Input Leakage Test | 74F | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 μA All Other Pins Grounded |
| $I_{OD}$ | Output Leakage Circuit Current | 74F | | | 3.75 | μA | 0.0 | $V_{IOD}$ = 150 mV All Other Pins Grounded |
| $I_{IL}$ | Input LOW Current | | | | −1.2 | mA | Max | $V_{IN}$ = 0.5V |
| $I_{OZH}$ | Output Leakage Current | | | | 50 | μA | Max | $V_{OUT}$ = 2.7V |
| $I_{OZL}$ | Output Leakage Current | | | | −50 | μA | Max | $V_{OUT}$ = 0.5V |
| $I_{OS}$ | Output Short-Circuit Current | | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V |
| $I_{ZZ}$ | Bus Drainage Test | | | | 500 | μA | 0.0V | $V_{OUT}$ = 5.25V |
| $I_{CCH}$ | Power Supply Current | | | 34 | 42 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | | 40 | 57 | mA | Max | $V_O$ = LOW |
| $I_{CCZ}$ | Power Supply Current | | | 40 | 57 | mA | Max | $V_O$ = HIGH Z |

## AC Electrical Characteristics

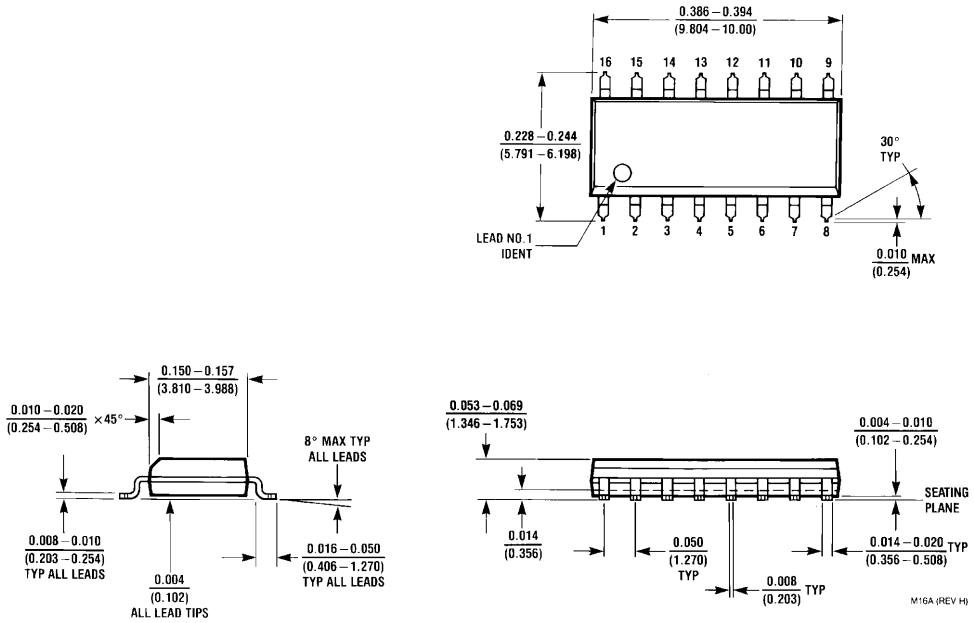
| Symbol | Parameter | 74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF | | | 74F $T_A$, $V_{CC}$ = Com, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 3.0 | 4.5 | 6.0 | 3.0 | 7.0 | ns |
| $t_{PHL}$ | $I_n$ to $O_n$ | 2.5 | 4.0 | 5.5 | 2.5 | 6.5 | |
| $t_{PLH}$ | Propagation Delay | 4.0 | 7.8 | 10.0 | 4.0 | 13.5 | ns |
| $t_{PHL}$ | $S_n$ to $O_n$ | 3.0 | 6.5 | 8.5 | 3.0 | 9.5 | |
| $t_{PZH}$ | Output Enable Time | 2.5 | 5.0 | 7.0 | 2.5 | 8.0 | ns |
| $t_{PZL}$ | | 4.0 | 7.0 | 9.0 | 4.0 | 10.0 | |
| $t_{PHZ}$ | Output Disable Time | 2.0 | 3.9 | 5.5 | 2.0 | 6.5 | |
| $t_{PLZ}$ | | 2.0 | 4.0 | 5.5 | 2.0 | 7.5 | |

## Ordering Information

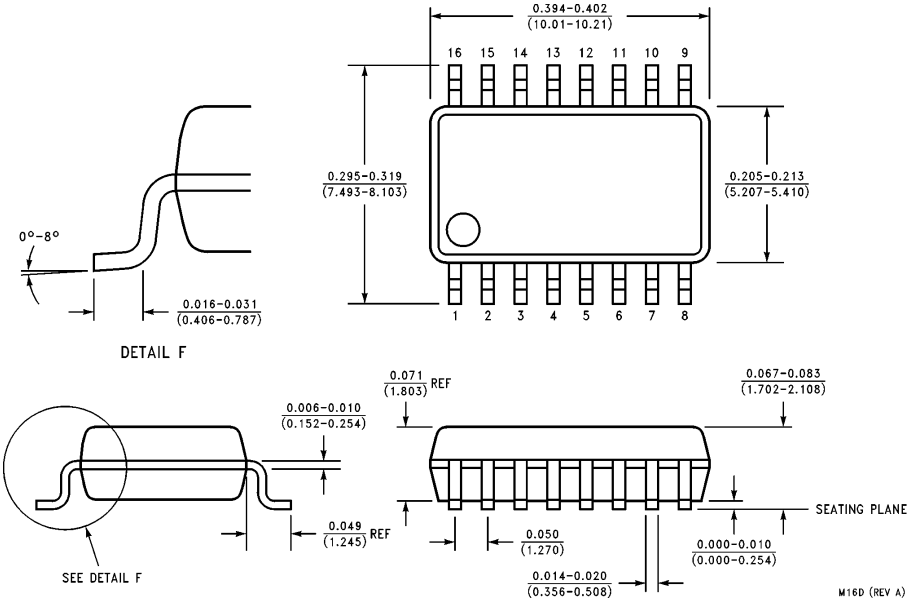
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



## Physical Dimensions inches (millimeters)

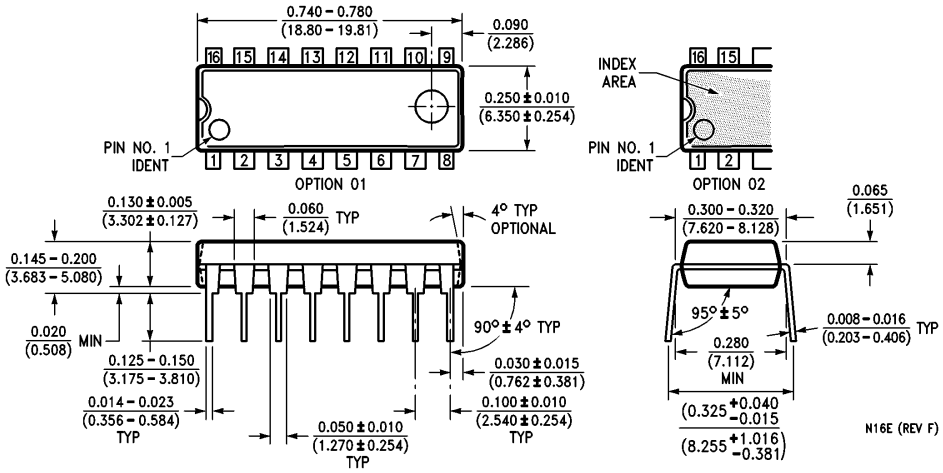



**16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)**
**NS Package Number M16A**




**16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)**
**NS Package Number M16D**

## Physical Dimensions inches (millimeters) (Continued)




**16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)**
**NS Package Number N16E**

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