

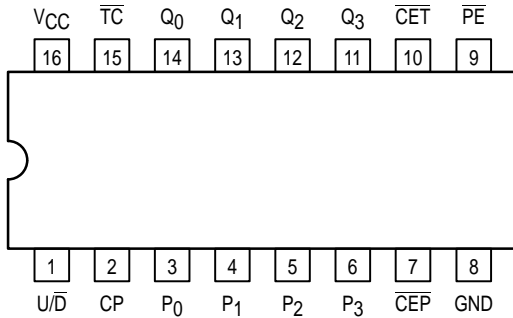


4-STAGE SYNCHRONOUS BIDIRECTIONAL COUNTERS

The MC54/74F168 and MC54/74F169 are fully synchronous 4-stage up/down counters. The F168 is a BCD decade counter; the F169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading, and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

- Asynchronous Counting and Loading
- Built-In Lookahead Carry Capability
- Presetable for Programmable Operation

CONNECTION DIAGRAM (TOP VIEW)

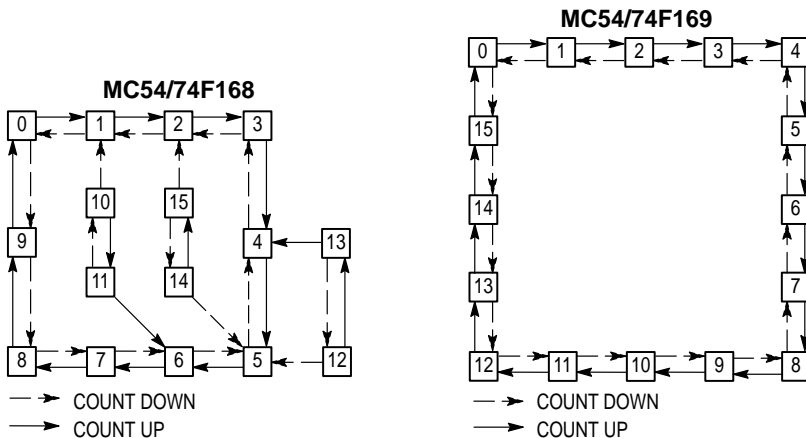


MODE SELECT TABLE

PE	CEP	CET	U/D	Action on Rising Clock Edge
L	X	X	X	Load (P_n Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

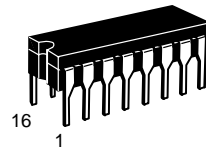
STATE DIAGRAMS



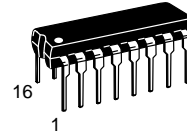
MC54/74F168
MC54/74F169

**4-STAGE SYNCHRONOUS
BIDIRECTIONAL COUNTERS**

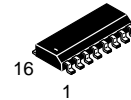
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

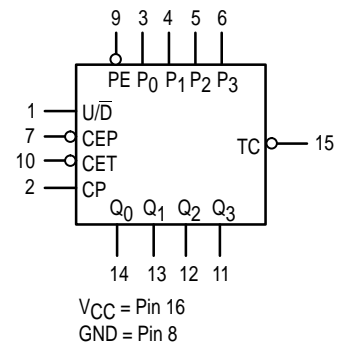


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

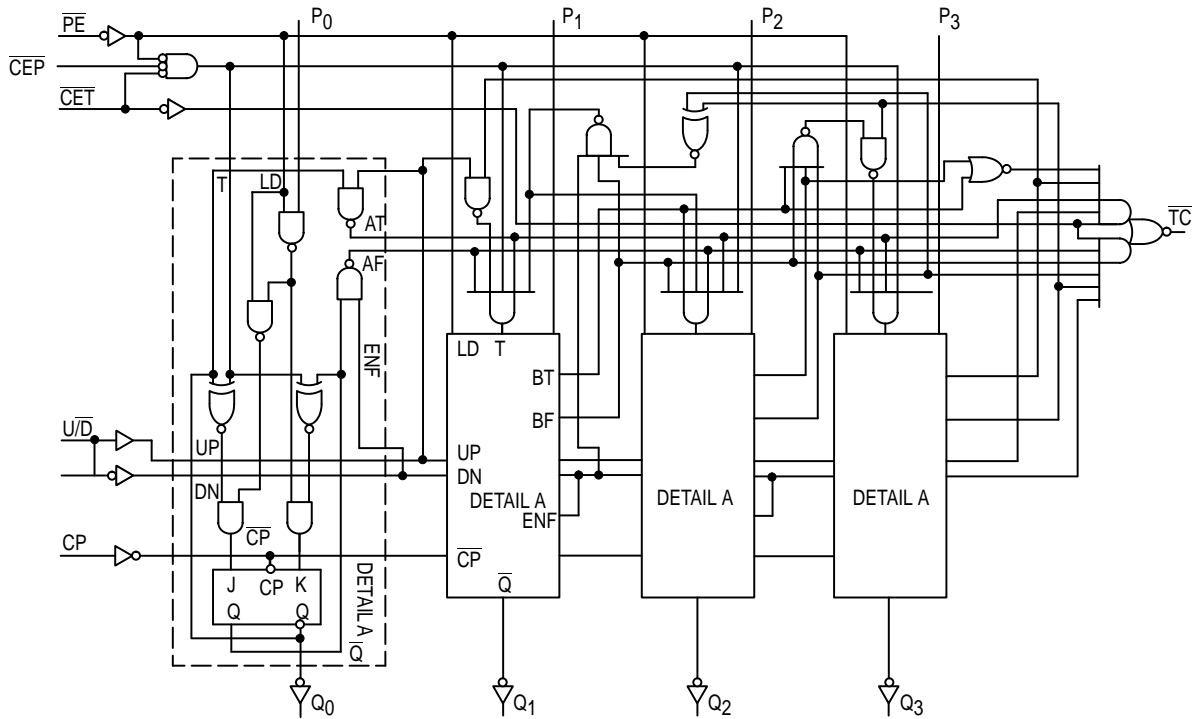
LOGIC SYMBOL



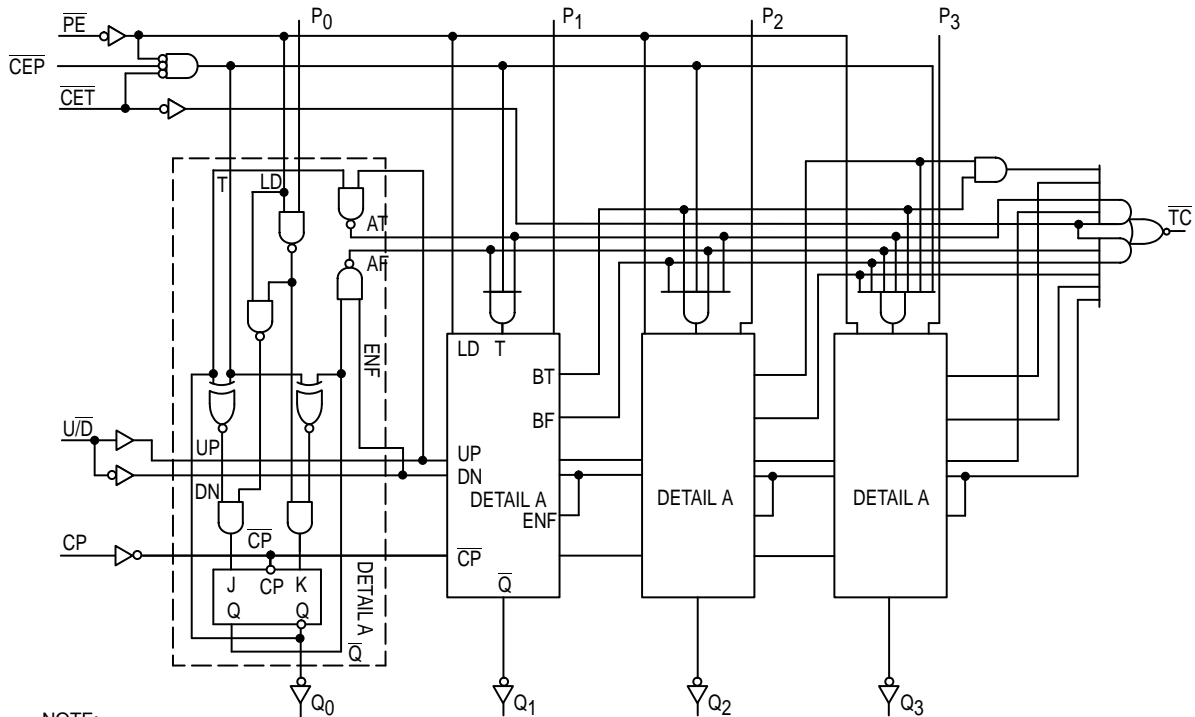
MC54/74F168 • MC54/74F169

LOGIC DIAGRAMS

MC54/74F168



MC54/74F169



NOTE:

These diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC54/74F168 • MC54/74F169

FUNCTIONAL DESCRIPTION

The F168 and F169 use edge-triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When \overline{PE} is LOW, the data on the P₀-P₃ inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both \overline{CEP} and \overline{CET} must be LOW and \overline{PE} must be HIGH; the U/ \overline{D} input then determines the direction of counting. The Terminal Count (\overline{TC}) output is normally HIGH and goes LOW, provided that \overline{CET} is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the F169) in the Count Up mode. The \overline{TC}

output state is not a function of the Count Enable Parallel (\overline{CEP}) input level. The \overline{TC} output of the F168 decade counter can also be LOW in the illegal states 11, 13, and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the F168 will return to the legitimate sequence within two counts. Since the \overline{TC} signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on \overline{TC} . For this reason the use of \overline{TC} as a clock signal is not recommended (see logic equations below).

- 1) Count Enable = $\overline{CEP} \cdot \overline{CET} \cdot PE$
- 2) Up: (F168): $\overline{TC} = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
(F169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
- 3) Down: $\overline{TC} = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (Down) \cdot \overline{CET}$

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current CET Other Inputs			-1.2	mA	V _{CC} = MAX, V _{IN} = 0.5 V
				-0.6		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current			52	mA	V _{CC} = MAX

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F168 • MC54/74F169

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100		60		85		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{\text{PE}}$ HIGH or LOW)	3.0 4.0	8.5 11.5	3.0 4.0	10.5 14	3.0 4.0	9.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{\text{TC}}$ (F168)	5.5 4.0	15.5 11	5.5 4.0	18 13.5	5.5 4.0	17 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{\text{TC}}$ (F169)	5.0 4.0	15.5 11	5.0 4.0	18 13.5	5.0 4.0	17 12.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{CET}}$ to $\overline{\text{TC}}$	2.5 2.5	6.0 8.0	2.5 2.5	8.0 10	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $U/\overline{\text{D}}$ to $\overline{\text{TC}}$ (F168)	3.5 4.0	11 16	3.5 4.0	13.5 18.5	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation Delay $U/\overline{\text{D}}$ to $\overline{\text{TC}}$ (F169)	3.5 4.0	11 10.5	3.5 4.0	13.5 13	3.5 4.0	12.5 12	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F		54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ $V_{CC} = 5.0\text{ V} \pm 10\%$		
		Min	Max	Min	Max	Min	Max	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup Time, HIGH or LOW P_n to CP	4.0 4.0		5.5 5.5		4.5 4.5		ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold Time, HIGH or LOW P_n to CP	3.0 3.0		3.5 3.5		3.5 3.5		ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	5.0 5.0		7.0 7.0		6.0 6.0		ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold Time HIGH or LOW $\overline{\text{CEP}}$ or $\overline{\text{CET}}$ to CP	0 0		0 0		0 0		ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{PE}}$ to CP	8.0 8.0		10 10		9.0 9.0		ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ to CP	0 0		0 0		0 0		ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup Time, HIGH or LOW (F168) $U/\overline{\text{D}}$ to CP	11 16.5		13.5 19		12.5 18		ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup Time, HIGH or LOW (F169) $U/\overline{\text{D}}$ to CP	11 7.0		13.5 9.0		12.5 8.0		ns
$t_{\text{H}}(\text{H})$ $t_{\text{H}}(\text{L})$	Hold time, HIGH or LOW $U/\overline{\text{D}}$ to CP	0 0		0 0		0 0		ns
$t_{\text{W}}(\text{H})$ $t_{\text{W}}(\text{L})$	CP Pulse Width HIGH or LOW	5.0 5.0		8.0 8.0		5.5 5.5		ns