

MM74C Series CMOS

Functionally equivalent to Standard 74 Series
Pin compatible with Standard 74 Series.
Dissipation typically 10 nanowatts per gate

GENERAL DESCRIPTION

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

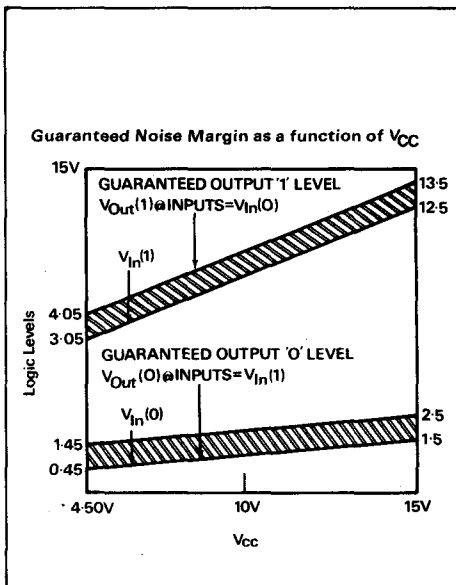
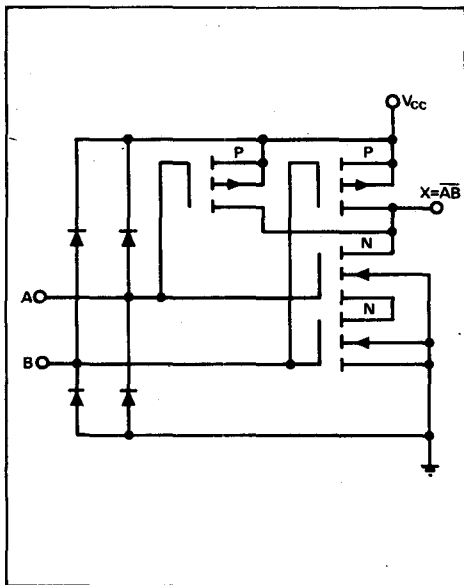
See outline drawings Nos. 109, 111 and 114 for physical dimensions.

FEATURES

| | |
|-----------------------------------|-------------------|
| Wide supply voltage range | 3V to 15V |
| Guaranteed noise margin | 1V |
| High noise immunity | 0.45 V_{CC} typ |
| Lower power TTL compatible drives | 2 x 74L loads |

APPLICATIONS

Automotive
Instrumentation
Alarm systems
Remote metering.
Data terminals
Medical electronics
Industrial controls
Computers



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TYPICAL GATE CHARACTERISTICS

Given below are details of a representative function (the MM74 COON)

ABSOLUTE MAXIMUM RATINGS

| | | | |
|-----------------------------|----------------------------------|--------------------------------------|-------------|
| Voltage at Any Pin (Note 1) | -0.3V to +V _{CC} + 0.3V | Package Dissipation | 500mW |
| Operating Temperature | 0°C to +70°C | Lead Temperature (Soldering, 10 sec) | 300°C |
| Storage Temperature | -65°C to +150°C | Operating V _{CC} Range | +3V to +15V |

ELECTRICAL CHARACTERISTICS

Min./Max. limits apply across the guaranteed temperature range unless otherwise specified.

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|--|---|-----------------------|------------|------------|-------|
| CMOS to CMOS | | | | | |
| Logical "1" Input Voltage V _{IN} (1) | V _{CC} = 5.0V V _{CC} = 10.0V | 3.5 8.0 | | | V |
| Logical "0" Input Voltage V _{IN} (0) | V _{CC} = 5.0V V _{CC} = 10.0V | | 1.5 2.0 | | V |
| Logical "1" Output Voltage V _{OUT} (1) | V _{CC} = 5.0V, V _{IN} = 1.5, I _O = -10 μA V _{CC} = 10.0V, V _{IN} = 7.0, I _O = -10 μA | 4.5 9.0 | | | V |
| Logical "0" Output Voltage V _{OUT} (0) | V _{CC} = 5.0V, V _{IN} = 3.5, I _O = 10 μA V _{CC} = 10.0V, V _{IN} = 8.0, I _O = 10 μA | | | 0.5 1.0 | V |
| Logical "1" Input Current I _{IN} (1) | V _{CC} = 15V, V _{IN} = 15V | | | 1 | μA |
| Logical "0" Input Current I _{IN} (0) | V _{CC} = 15V, V _{IN} = 0V | -1 | | | μA |
| Output Short Circuit Current I _{OS} (1) (Note 2) | V _{CC} = 5.5V, V _{IN} = 0, V _O = 0 V _{CC} = 11.0V, V _{IN} = 0, V _O = 0 | 1 7.5 | | 6 30 | mA |
| Output Short Circuit Current I _{OS} (0) (Note 2) | V _{CC} = 5.5V, V _{IN} = V _O = V _{CC} V _{CC} = 11.0V, V _{IN} = V _O = V _{CC} | 1.5 10 | | 10 40 | mA |
| Supply Current I _{CC} | V _{CC} = 15V | | | 1 | μA |
| Propagation Delay Time to a Logical "0" t _{pd0} | V _{CC} = 5.0V, C _L = 50 pF, T _A = 25°C V _{CC} = 10.0V, C _L = 50 pF, T _A = 25°C | | 50 25 | 90 60 | ns |
| Propagation Delay Time to a Logical "1" t _{pd1} | V _{CC} = 5.0V, C _L = 50 pF, T _A = 25°C V _{CC} = 10.0V, C _L = 50 pF, T _A = 25°C | | 50 30 | 90 60 | ns |
| LOW POWER TTL to CMOS | | | | | |
| Logical "1" Input Voltage V _{IN} (1) | V _{CC} = 4.75V | V _{CC} - 1.5 | | | V |
| Logical "0" Input Voltage V _{IN} (0) | V _{CC} = 4.75V | | | 0.8 | V |
| Logical "1" Output Voltage V _{OUT} (1) | V _{CC} = 4.75V, I _O = -10 μA | 4.4 | | | V |
| Logical "0" Output Voltage V _{OUT} (0) | V _{CC} = 4.75V, I _O = 10 μA | | | 0.8 | V |
| Propagation Delay Time to a Logical "0" t _{pd(0)} | V _{CC} = 5.0V, C _L = 15 pF, T _A = 25°C | | 125 | | ns |
| Propagation Delay Time to a Logical "1" t _{pd(1)} | V _{CC} = 5.0V, C _L = 15 pF, T _A = 25°C | | 125 | | ns |
| CMOS to Low Power TTL (tenth power) | | | | | |
| Logical "1" Input Voltage V _{IN} (1) | V _{CC} = 4.75V | 4.0 | | | V |
| Logical "0" Input Voltage V _{IN} (0) | V _{CC} = 4.75V | | | 1.0 | V |
| Logical "1" Output Voltage V _{OUT} (1) | V _{CC} = 4.75V, V _{IN} = 0.8, I _O = -100 μA | 2.4 | | | V |
| Logical "0" Output Voltage V _{OUT} (0) | V _{CC} = 4.75V, V _{IN} = 4.0, I _O = 360 μA | | | 0.4 | V |
| Propagation Time to a Logical "0" t _{pd(0)} | V _{CC} = 5.0V, C _L = 50 pF, R _L = 20k, T _A = 25°C | | 60 | | ns |
| Propagation Time to a Logical "1" t _{pd(1)} | V _{CC} = 5.0V, C _L = 50 pF, R _L = 20k, T _A = 25°C | | 45 | | ns |

Note 1: These devices should not be connected under power on conditions.

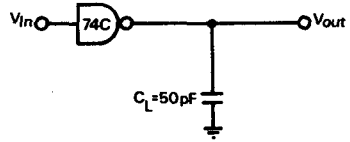
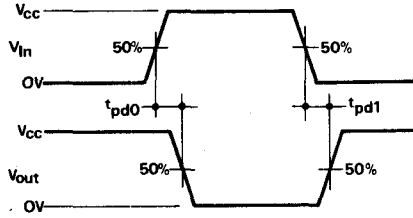
Note 2: Only one output at a time may be shorted.

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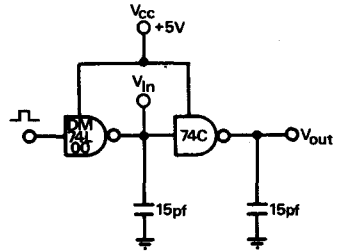
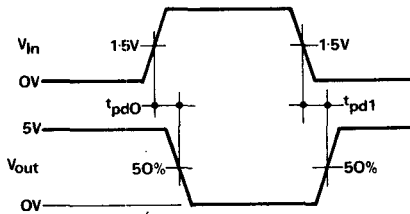
PLEASE QUOTE STOCK NO. AND MANUFACTURER'S CODE WHEN ORDERING

switching time waveforms and ac test circuits

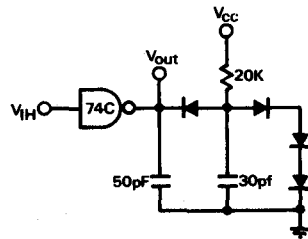
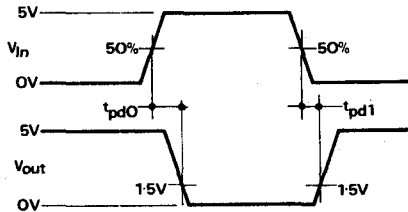
CMOS to CMOS



TTL to CMOS



CMOS to low power TTL



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MM74C Series CMOS

REFERENCE TABLE. See outline drawings Nos. 109, 111 and 114 for physical dimensions.

| Code | Function | Stock No. | Connection Diagram No. |
|------------|--|---------------|------------------------|
| MM74C00N | Quad 2-input NAND Gate | 33233R | B1 |
| MM74C02N | Quad 2-input NOR Gate | 33234G | B3 |
| MM74C04N | Hex Inverter | 33235E | B5 |
| MM74C08N | Quad 2-input AND Gate | 34685C | B9 |
| MM74C10N | Triple 3-input NAND Gate | 33236C | B11 |
| MM74C20N | Dual 4-input NAND Gate | 33237A | B19 |
| MM74C30N | 8-input NAND Gate | 34686A | B26 |
| MM74C42N | BCD-To-Decimal Decoder | 33238X | B33 |
| MM74C73N | Dual J-K Master-Slave Flip-Flop | 33239H | B54 |
| MM74C74N | Dual "D" Flip-Flop | 33240X | B55 |
| MM74C76N | Dual J-K Master-Slave Flip-Flop | 33241R | B57 |
| MM74C83N | 4-Bit Binary Full Adder | 34687X | B62 |
| MM74C85N | 4-Bit Magnitude Comparator | 34688H | B64 |
| MM74C86N | Quad 2-input EXCLUSIVE-OR Gate | 34689F | B65 |
| MM74C89N | 64-Bit TRI-STATE random access read/write memory | 34690R | B67 |
| MM74C95N | 4-Bit Parallel-In/Parallel-Out Shift Register | 33242G | B73 |
| MM74C107N | Dual J-K Master-Slave Flip-Flop | 33243E | B80 |
| MM74C123N | Retriggerable Monostable Multivibrator | 33244C | B89 |
| MM74C151N | 8-Bit Data Selections/MUX with Strobe | 33245A | B103 |
| MM74C154N | 4 to 16 Line Decoder Demultiplexer | 33246X | B106 |
| MM74C157N | Quad 2 Line to 1 Line Multiplexer | 33419X | B109 |
| MM74C160N | Synchronous Decade Counter | 33247H | B111 |
| MM74C161N | Synchronous 4-Bit Binary Counter | 33248F | B112 |
| MM74C162N | Fully Synchronous Decade Counter | 33249D | B113 |
| MM74C163N | Fully Synchronous 4-Bit Binary Counter | 33250G | B114 |
| MM74C164N | 8-Bit Parallel-Out Shift Register | 33251E | B115 |
| MM74C165N | Parallel-Load 8-Bit Shift Register | 33252C | B116 |
| MM74C173N | Quad Latch | 33254X | B120 |
| MM74C174N | Hex D Flip-Flop | 34691G | B121 |
| MM74C192N | Synchronous Up/Down Decade Counter | 33255H | B134 |
| MM74C193N | Synchronous Up/Down 4-Bit Binary Counter | 33256F | B135 |
| MM74C195N | 4-Bit Parallel-Access Shift Register | 33257D | B137 |
| *MM74C200N | 256-BIT RAM | 33258B | B142 |

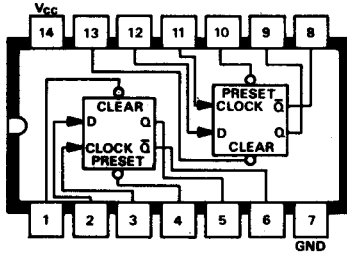
*NOTE: These are new products—check on availability with our sales desk.

PLEASE QUOTE STOCK NO. AND MANUFACTURER'S CODE WHEN ORDERING

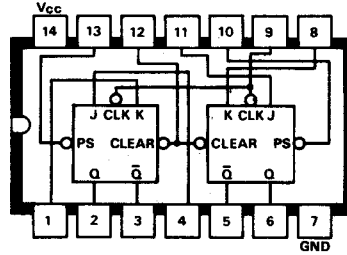
Semiconductors

Connection Diagrams

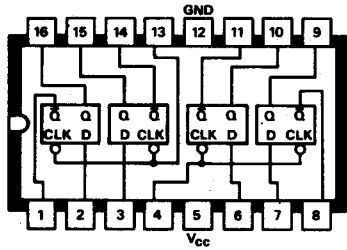
B55 SN7474N
SN74H74N/SN74S74N
SN74L74N/SN74C74N
 Dual D type flip-flop (edge triggered)



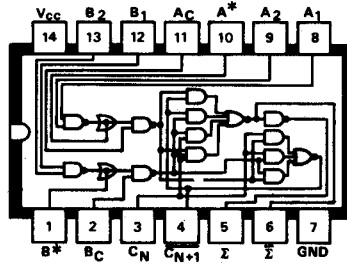
B58 SN74H78N
 Dual J-K flip-flop
 with preset and clear



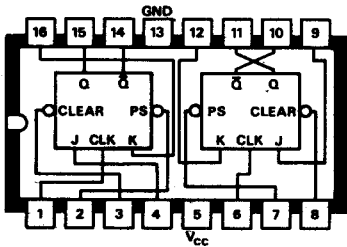
B56 SN7475N
 Quad bistable latch



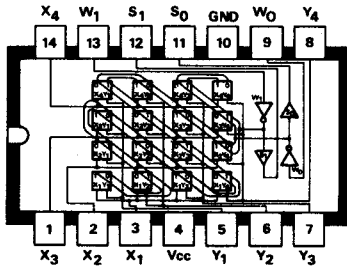
B59 SN7480N
 Gated full adder



B57 SN7476N
SN74H76N/SN74C76N
 Dual J-K master-slave flip-flop
 with preset and clear



B60 SN7481N
 16 bit read/write memory



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