

October 1987 Revised May 2002

MM74C08 Quad 2-Input AND Gate

General Description

The MM74C08 employs complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to $V_{\rm CC}$ and GND.

Features

■ Wide supply voltage range: 3.0V to 15V

■ Guaranteed noise margin: 1.0V

■ High noise immunity: 0.45 V_{CC} (typ.)

■ Low power TTL compatibility: Fan out of 2 driving 74L

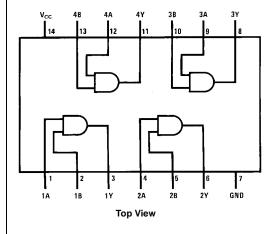
■ Low power consumption: 10 nW/package (typ.)

Ordering Code:

Order Number	Package Number	Package Description			
MM74C08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow			
MM74CD8N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide			

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Truth Table

Inputs		Outputs		
Α	В	Υ		
L	L	L		
L	Н	L		
Н	L	L		
Н	Н	Н		

H = HIGH Level L = LOW Level

Absolute Maximum Ratings(Note 1)

 $\begin{array}{lll} \mbox{Voltage at Any Pin} & -0.3\mbox{V to V}_{\mbox{CC}} + 0.3\mbox{V} \\ \mbox{Operating Temperature Range} & -55\mbox{^{\circ}C to } +125\mbox{^{\circ}C} \\ \mbox{Storage Temperature Range} & -65\mbox{^{\circ}C to } +150\mbox{^{\circ}C} \\ \end{array}$

Power Dissipation (P_D)

 $\begin{array}{cc} \text{Dual-In-Line} & 700 \text{ mW} \\ \text{Small Outline} & 500 \text{ mW} \\ \text{Operating V}_{\text{CC}} \text{ Range} & 3.0 \text{V to } 15 \text{V} \\ \end{array}$

Absolute Maximum V_{CC} 18V Lead Temperature

(Soldering, 10 seconds)

260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO C	MOS	•				
V _{IN(1)}	Logical "1" Input Voltage	V _{CC} = 5.0V	3.5			V
		V _{CC} = 10V	8.0			
V _{IN(0)}	Logical "0" Input Voltage	V _{CC} = 5.0V			1.5	V
		V _{CC} = 10V			2.0	
V _{OUT(1)}	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_{O} = -10 \mu A$	4.5			V
		$V_{CC} = 10V, I_{O} = -10 \mu A$	9.0			
V _{OUT(0)}	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_{O} = 10 \mu A$			0.5	V
		$V_{CC} = 10V, I_{O} = 10 \mu A$			1.0	
I _{IN(1)}	Logical "1" Input Current	V _{CC} = 15V, V _{IN} = 15V		0.005	1.0	μΑ
I _{IN(0)}	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μΑ
Icc	Supply Current	V _{CC} = 15V		0.01	15	μΑ
CMOS/LPT1	L INTERFACE	<u> </u>		•		•
V _{IN(1)}	Logical "1" Input Voltage	74C, V _{CC} = 4.75V	V _{CC} - 1.5			V
V _{IN(0)}	Logical "0" Input Voltage	74C, V _{CC} = 4.75V			0.8	V
V _{OUT(1)}	Logical "1" Output Voltage	74C, $V_{CC} = 4.75V$, $I_{O} = -360 \mu A$	2.4			V
V _{OUT(0)}	Logical "0" Output Voltage	74C, $V_{CC} = 4.75V$, $I_{O} = 360 \mu A$			0.4	V
OUTPUT DE	RIVE (see Family Characteristics D	Pata Sheet) T _A = 25°C (short circuit curren	t)			
I _{SOURCE}	Output Source Current	V _{CC} = 5.0V, V _{OUT} = 0V	-1.75	-3.3		mA
	(P-Channel)					
I _{SOURCE}	Output Source Current	V _{CC} = 10V, V _{OUT} = 0V	-8.0	15		mA
	(P-Channel)					
I _{SINK}	Output Sink Current	V _{CC} = 5.0V, V _{OUT} = V _{CC}	1.75	3.6		mA
	(N-Channel)					
I _{SINK}	Output Sink Current	V _{CC} = 10V, V _{OUT} = V _{CC}	8.0	16		mA
	(N-Channel)					1

AC Electrical Characteristics (Note 2)

(MM74C08) $T_A = 25^{\circ}C$, $C_L = 50$ pF, unless otherwise specified

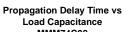
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t _{pd0} , t _{pd1}	Propagation Delay Time to	V _{CC} = 5.0V		80	140	ns
	Logical "1" or "0"	V _{CC} = 10V		40	70	113
C _{IN}	Input Capacitance	(Note 3)		5.0		pF
C _{PD}	Power Dissipation Capacitance	(Note 4) Per Gate		14		pF

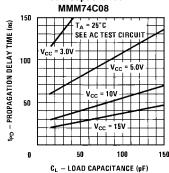
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

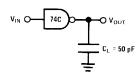
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Performance Characteristics



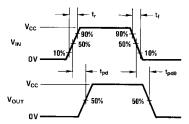


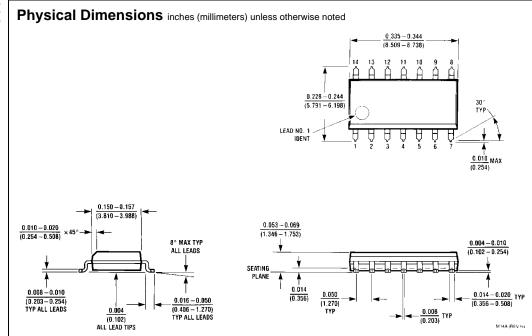
AC Test Circuit



Note: Delays measured with input $t_{\text{r}},\,t_{\text{f}}=20~\text{ns}$

Switching Time Waveforms





14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)0.090 (2.286) 14 13 12 11 10 9 8 14 13 12 0.250 ± 0.010 (6.350 ± 0.254) PIN NO. 1 IDENT 1 2 3 4 5 6 7 IDENT 1 2 3 $\frac{0.092}{(2.337)} \text{ DIA } \frac{0.030}{(0.762)} \frac{\text{MAX}}{\text{DEPTH}}$ OPTION 1 OPTION 02 0.135 ± 0.005 0.300 - 0.320 (3.429 ± 0.127) (7.620 - 8.128)0.065 0.145 - 0.2000.060 4° TYP Optional (1.651) (1.524) (3.683 - 5.080)¥ 0.008 - 0.016 TYP 0.020 $\overline{(0.203 - 0.406)}$ (0.508)0.125 - 0.150 MIN 0.075 ± 0.015 $\overline{(3.175 - 3.810)}$ 0.280 (1.905 ± 0.381)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

0.100±0.010 TYP

 (2.540 ± 0.254)

 0.050 ± 0.010

(1.270 - 0.254)

TYP

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LIFE SUPPORT POLICY

0.01<u>4-0.023</u> TYP

(0.356 - 0.584)

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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

(7.112)-MIN

 $0.325 \,{}^{+\, 0.040}_{-\, 0.015}$

 $8.255 + 1.016 \\ -0.381$

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N14A (REV F)