

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74ACT112 is an advanced high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

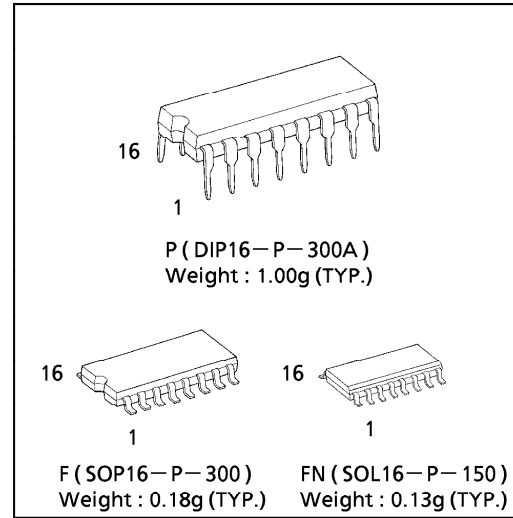
FEATURES:

- High Speed..... $f_{MAX} = 175\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs ... $V_{IL} = 0.8\text{V}$ (Max.)
 $V_{IH} = 2.0\text{V}$ (Min.)
- Symmetrical Output Impedance... $|I_{OH}| = |I_{OL}| = 24\text{mA}$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F112

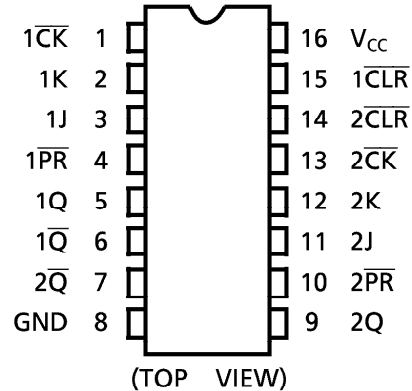
TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
CLR	PR	J	K	$\overline{\text{CK}}$	Q	$\overline{\text{Q}}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	\downarrow	Q_n	\overline{Q}_n	NO CHANGE
H	H	L	H	\downarrow	L	H	
H	H	H	L	\downarrow	H	L	
H	H	H	H	\downarrow	\overline{Q}_n	Q_n	TOGGLE
H	H	X	X	\uparrow	Q_n	\overline{Q}_n	NO CHANGE

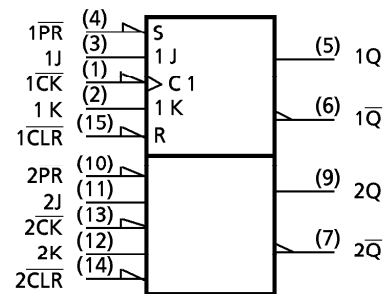
X : Don't Care



PIN ASSIGNMENT



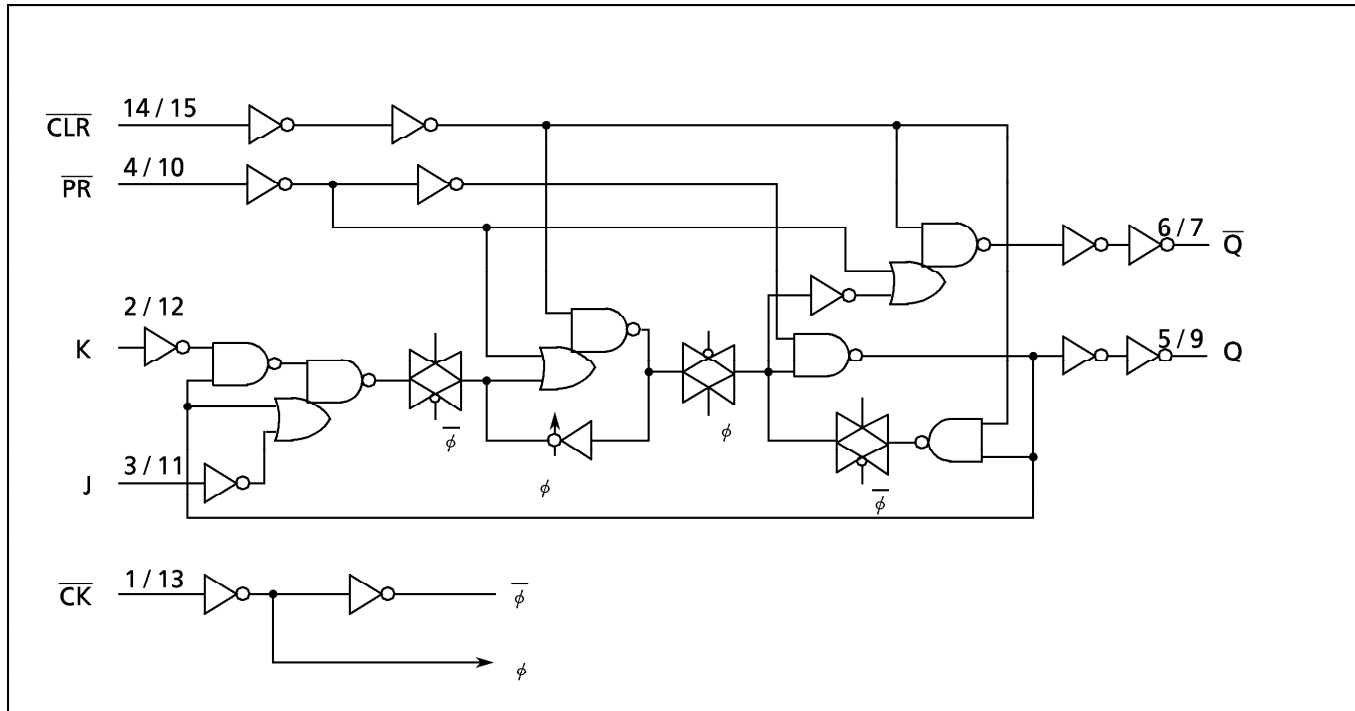
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	$^{\circ}C$

*500mW in the range of $T_a = -40^{\circ}C \sim 65^{\circ}C$. From $T_a = 65^{\circ}C$ to $85^{\circ}C$ a derating factor of $-10mW/^{\circ}C$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	$^{\circ}C$
Input Rise and Fall Time	dt/dV	0~10	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		4.5 ┆ 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	V _{IL}		4.5 ┆ 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I _{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0		
		I _C	PER INPUT : V _{IN} = 3.4V OTHER INPUT : V _{CC} or GND	5.5	—	—	1.35	—	1.5	mA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C	Ta = -40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (\overline{CK})	t _{W(L)}		5.0 ± 0.5	5.0	5.0	ns
	t _{W(H)}					
Minimum Pulse Width (\overline{CLR} , \overline{PR})	t _{W(L)}		5.0 ± 0.5	5.0	5.0	
Minimum Set - up Time	t _s		5.0 ± 0.5	5.0	5.0	
Minimum Hold Time	t _h		5.0 ± 0.5	1.0	1.0	
Minimum Removal Time (\overline{CLR} , \overline{PR})	t _{rem}		5.0 ± 0.5	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\ \Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time ($\overline{\text{CK}} - \text{Q}$, $\overline{\text{Q}}$)	t_{pLH}		5.0 ± 0.5	—	6.4	10.0	1.0	11.5	ns
	t_{pHL}								
Propagation Delay Time ($\overline{\text{CLR}}$, $\overline{\text{PR}} - \text{Q}$, $\overline{\text{Q}}$)	t_{pLH}		5.0 ± 0.5	—	6.8	10.5	1.0	12.0	ns
	t_{pHL}								
Maximum Clock Frequency	f _{MAX}		5.0 ± 0.5	85	100	—	85	—	MHz
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	32	—	—	—	

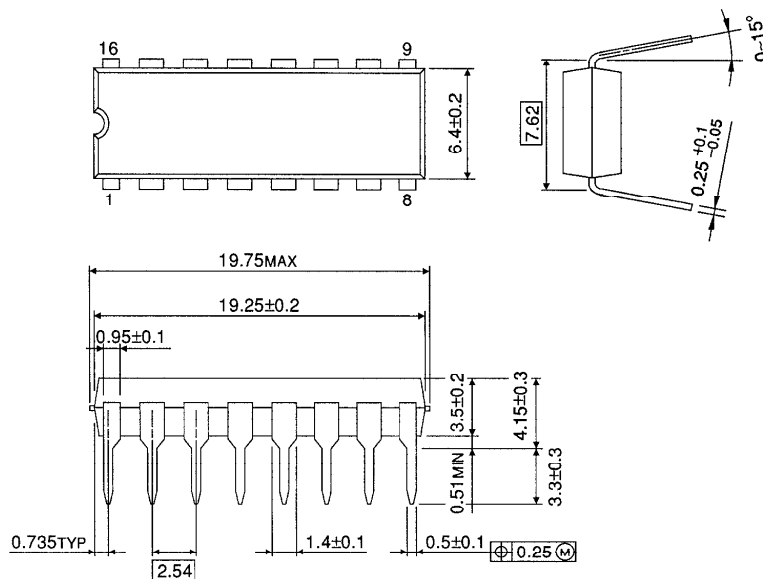
Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr.}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}} / 2 \text{ (per F/F)}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300A)

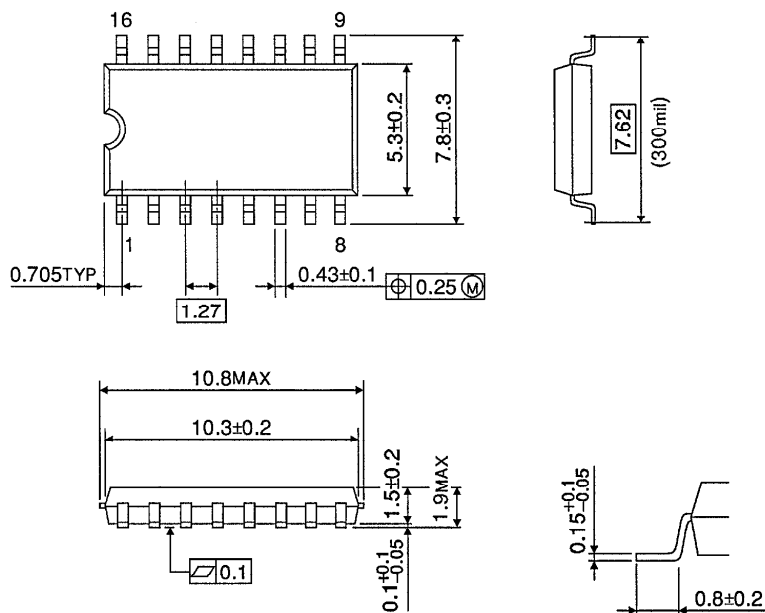
Unit in mm



Weight : 1.00g (TYP.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300)

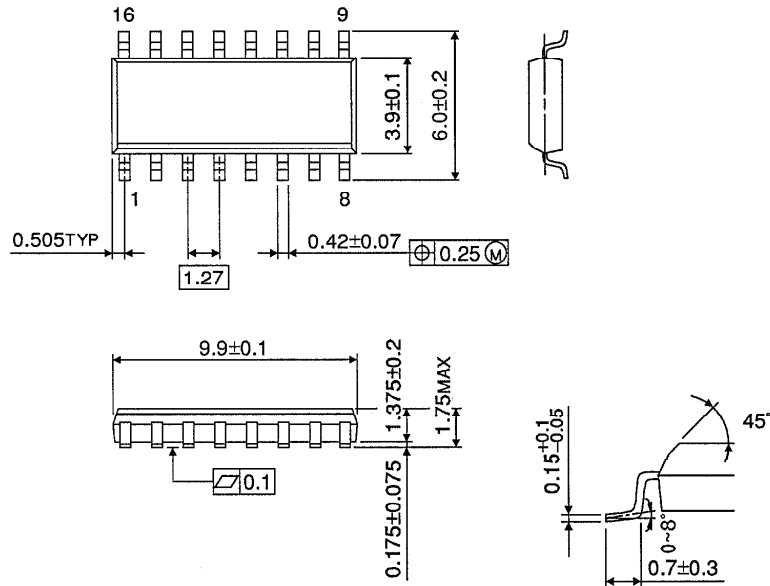
Unit in mm



Weight : 0.18g (TYP.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150)

Unit in mm



Weight : 0.13g (TYP.)