

SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

SDLS091

OCTOBER 1976 — REVISED MARCH 1988

- Four J-K Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Separate Negative-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Typical Clock Input Frequency . . . 50 MHz
- Fully Buffered Outputs

description

These quadruple TTL J-K flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by up to 50%. They feature hysteresis at each clock input, fully buffered outputs, and direct clear capability, and are presettable through a buffer that also features an input hysteresis loop. The negative-edge-triggering clocks are directly compatible with earlier Series 54/74 single and dual pulse-triggered flip-flops. These circuits can be used to emulate D- or T-type flip-flops by hard-wiring the inputs, or to implement asynchronous sequential functions.

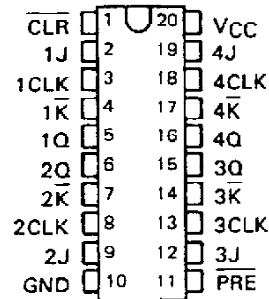
The SN54276 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74276 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE (EACH FLIP-FLOP)

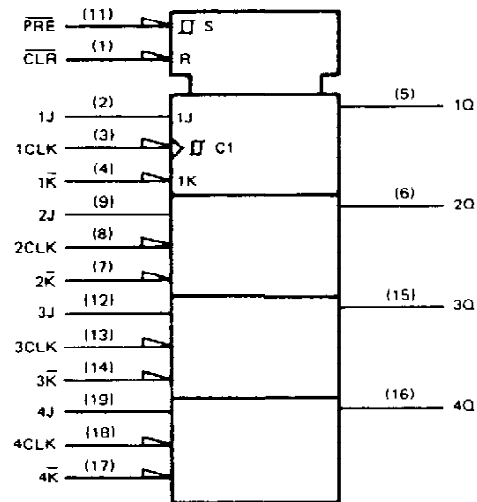
COMMON INPUTS		INPUTS			OUTPUT
PRE	CLR	CLK	J	K	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H [†]
H	H	↓	L	H	Q ₀
H	H	↓	H	H	H
H	H	↓	L	L	L
H	H	↓	H	L	TOGGLE
H	H	H	X	X	Q ₀

[†] This configuration is nonstable; that is, Q may not persist when preset and clear return to their inactive (high) level.

SN54276 . . . J PACKAGE
SN74276 . . . N PACKAGE
(TOP VIEW)



logic symbol[‡]



[‡] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

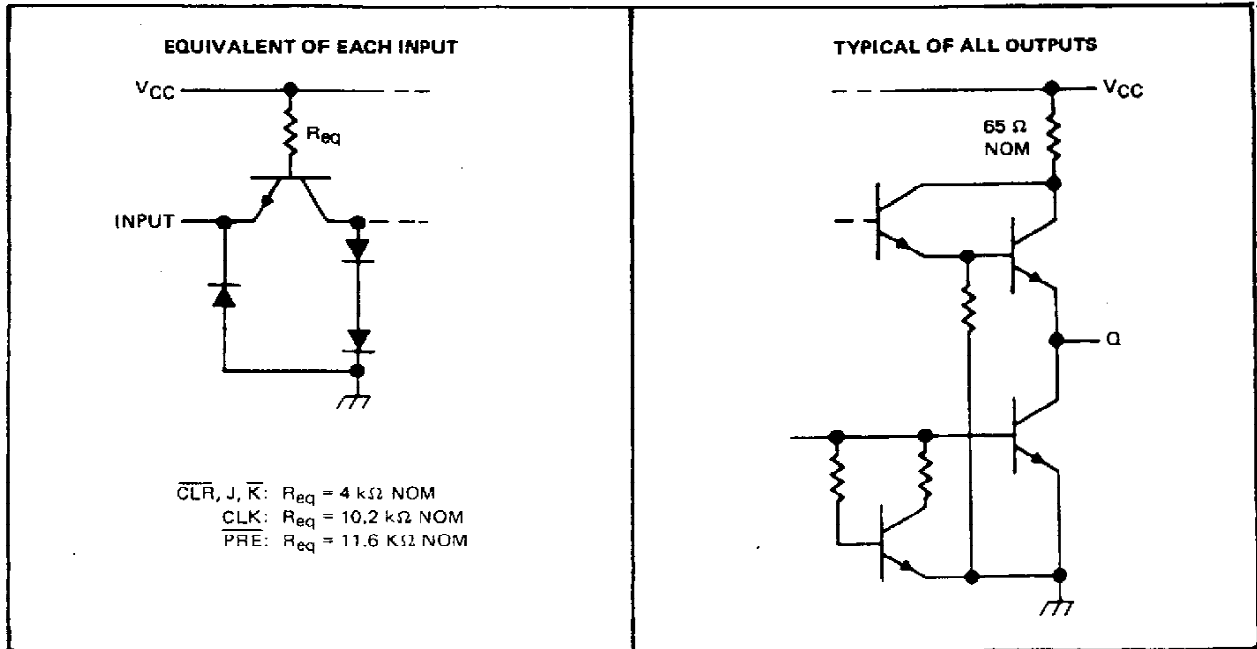
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SN54276, SN74276
QUADRUPLE J-K FLIP-FLOPS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54276	-55°C to 125°C
SN74276	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54276, SN74276 QUADRUPLE J-K FLIP-FLOPS

recommended operating conditions

		SN54276			SN74276			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				-800			-800	μ A
Low-level output current, I_{OL}				16			16	mA
Clock frequency		0		35	0		35	MHz
Pulse width, t_W	Clock high	13.5			13.5			ns
	Clock low	15			15			
	Preset or clear low	12			12			
Setup time, t_{su}	J, K inputs	3↓			3↓			ns
	Clear and preset inactive state	10↓			10↓			
Input hold time, t_h		10↓			10↓			ns
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}$ C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	μ A
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-85	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$		60	81	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency		35	50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset	$C_L = 15 \text{ pF}, R_L = 400 \Omega,$ See Note 2		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	30	ns
t_{PLH}	Propagation delay time, low-to-high level output from clock			17	30	ns
t_{PHL}	Propagation delay time, high-to-low level output from clock			20	30	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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