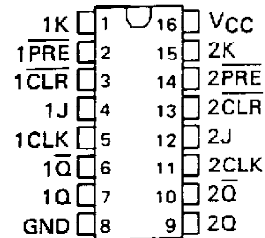


- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

SN54111 . . . J PACKAGE
 SN74111 . . . N PACKAGE
 (TOP VIEW)



description

The SN54111 and SN74111 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled to accept data only during a short period (30 nanoseconds maximum hold time) starting with, and immediately following the rising edge of the clock pulse. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. At the threshold level of the falling edge of the clock pulse, the data stored in the master will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptibility to noise is thereby effectively reduced.

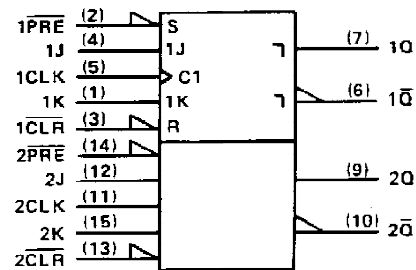
The SN54111 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74111 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q-bar
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [‡]	H [‡]
H	H		L	L	Q ₀	Q ₀ -bar
H	H		H	L	H	L
H	H		L	H	L	H
H	H		H	H	TOGGLE	

[‡]This configuration is non-stable; that is, it will not persist when preset or clear return to their inactive (high) level.

logic symbol†



[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

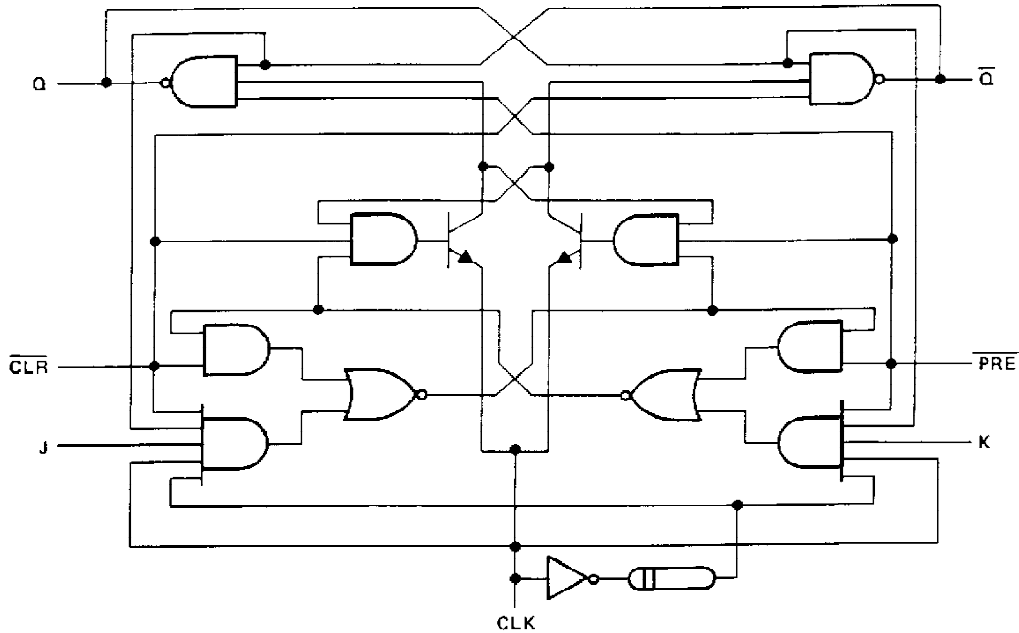
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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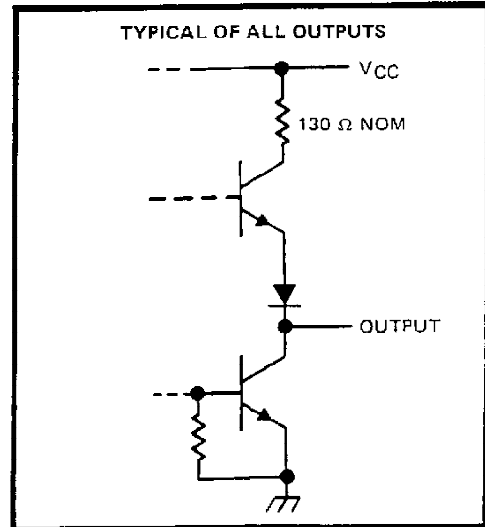
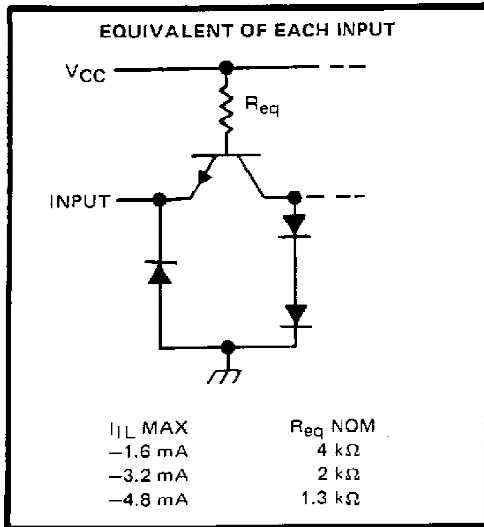
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SN54111, SN74111 DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54111	-55°C to 125°C
SN74111	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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SN54111, SN74111

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

recommended operating conditions

		SN54111			SN74111			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage	0.8			0.8			V	
I _{OH}	High-level output current	-0.8			-0.8			mA	
I _{OL}	Low-level output current	16			16			mA	
t _w	Pulse duration	CLK high or low	25		25		ns		
		PRE or CLR low	25		25				
t _{su}	Input setup time before CLK †	0			0			ns	
t _h	Input hold time data after CLK †	30			30			ns	
T _A	Operating free-air temperature	-55		125		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54111			SN74111			UNIT		
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX			
V _{IK}	V _{CC} = MIN, I _I = -12 mA	-1.5			-1.5			V		
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -0.8 mA	2.4	3.4		2.4	3.4		V		
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.2			0.2			V		
I _I	V _{CC} = MAX, V _I = 5.5 V	1			1			mA		
I _{IH}	J or K	40			40			μA		
	CLR or PRE	80			80					
	CLK	120			120					
I _{IL}	J or K	-1.6			-1.6			mA		
	CLR †	-3.2			-3.2					
	PRE †	-3.2			-3.2					
	CLK	-4.8			-4.8					
I _{OS} §	V _{CC} = MAX	-20		-57	-18		-57	mA		
I _{CC} #	V _{CC} = MAX, See Note 2	14		20.5		14		20.5		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

† Clear is tested with preset high and preset is tested with clear high.

Average per flip-flop.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				20	25		MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	R _L = 400 Ω, C _L = 15 pF	12	18		ns
t _{PHL}				21	30		ns
t _{PLH}	CLK	Q or \bar{Q}		12	17		ns
t _{PHL}				20	30		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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