

TOSHIBA PHOTOCOUPLER GaAlAs IRED & PHOTO IC

6N138, 6N139

CURRENT LOOP DRIVER.

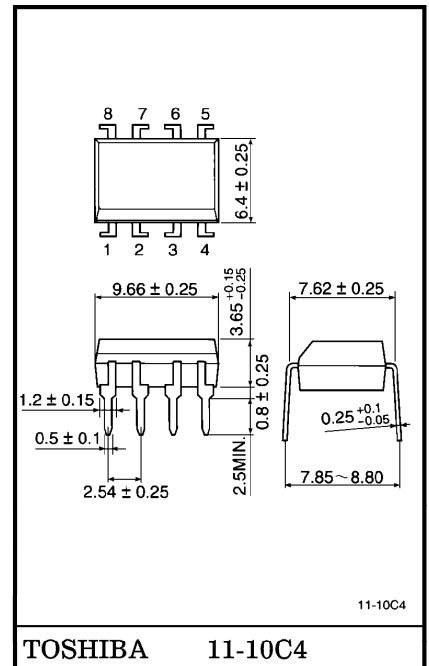
LOW INPUT CURRENT LINE RECEIVER.

CMOS LOGIC INTERFACE.

The TOSHIBA 6N138 and 6N139 consists of a GaAlAs infrared emitting diode coupled with a split-Darlington output configuration. A high speed GaAlAs IRED manufactured with an unique LPE junction, has the virtue of fast rise and fall time at low drive current.

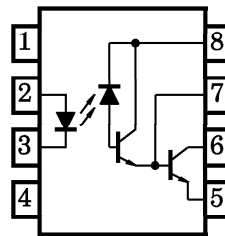
- Isolation Voltage : 2500V_{rms} (Min.)
- Current Transfer Ratio
 - : 6N138 - 300% (Min.) ($I_F = 1.6\text{mA}$)
 - : 6N139 - 400% (Min.) ($I_F = 0.5\text{mA}$)
- Switching Time: 6N138 - $t_{PHL} = 10\mu\text{s}$ (Max.)
 - $t_{PLH} = 35\mu\text{s}$ (Max.)
 6N139 - $t_{PHL} = 1\mu\text{s}$ (Max.)
 - $t_{PLH} = 7\mu\text{s}$ (Max.)
- UL Recognized : UL1577, File No. E67349

Unit in mm



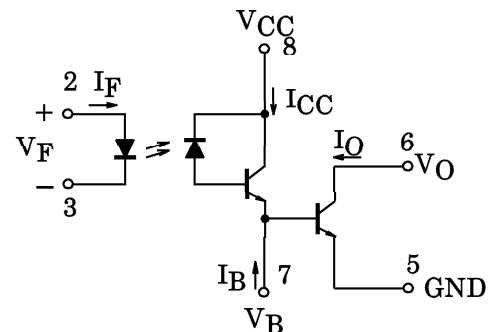
Weight : 0.54g

PIN CONFIGURATION (Top view)



- 1 : N.C.
- 2 : ANODE
- 3 : CATHODE
- 4 : N.C.
- 5 : GND
- 6 : OUTPUT
- 7 : OUTPUT BASE
- 8 : V_{CC}

SCHEMATIC



MAXIMUM RATINGS (*) (Ta = 0°C to +70°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current (Note 1)	I _F	20	mA
	Pulse Forward Current	I _{FP} ^(*)	40	mA
	Total Pulse Forward Current	I _{FP} ^(**)	1	A
	Reverse Voltage	V _R	5	V
	Diode Power Dissipation (Note 2)	P _D	35	mW
DETECTOR	Output Current (Note 3)	I _O	60	mA
	Emitter-Base Reverse Voltage	V _{EB}	0.5	V
	Supply Voltage	V _{CC} ^(*)	-0.5 to 18	V
	Output Voltage	V _O ^(**)	-0.5 to 18	V
	Output Power Dissipation (Note 4)	P _O	100	mW
Operating Temperature Range		T _{opr}	0 to 70	°C
Storage Temperature Range		T _{stg}	-55 to 125	°C
Lead Solder Temperature (10s) ^(*)		T _{sol}	260	°C
Isolation Voltage (1min., R.H. ≤ 60%)		BV _S ^(**)	2500	V _{rms}
			3540	V _{dc}

(*) JEDEC Registered Data

(**) Not Registered JEDEC

(*) 50% duty cycle, 1ms pulse width

(*) Pulse width 1μs, 300pps

(*) 6N138... -0.5 to 7V

(*) 1.6mm below seating plane

ELECTRICAL CHARACTERISTICS
OVER RECOMMENDED TEMPERATURE (Ta = 0°C to 70°C, Unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	(*)TYP.	MAX.	UNIT
Current Transfer Ratio (Note 5, 6)	6N139	CTR (*)	I _F = 0.5mA, V _O = 0.4V V _{CC} = 4.5V	400	800	—	%
	6N138		I _F = 1.6mA, V _O = 0.4V V _{CC} = 4.5V	500	900	—	
Logic Low Output Voltage (Note 6)	6N139	V _{OL}	I _F = 1.6mA, I _O = 6.4mA V _{CC} = 4.5V	—	0.1	0.4	V
			I _F = 5mA, I _O = 15mA V _{CC} = 4.5V	—	0.1	0.4	
			I _F = 12mA, I _O = 24mA V _{CC} = 4.5V	—	0.2	0.4	
	6N138		I _F = 1.6mA, I _O = 4.8mA V _{CC} = 4.5V	—	0.1	0.4	
Logic High Output Current (Note 6)	6N139	I _{OH} (*)	I _F = 0mA, V _O = V _{CC} = 18V	—	0.05	100	μA
	6N138		I _F = 0mA, V _O = V _{CC} = 7V	—	0.05	250	
Logic Low Supply Current (Note 6)		I _{CCL}	I _F = 1.6mA, V _O = Open V _{CC} = 5V	—	0.2	—	mA
Logic High Supply Current (Note 6)		I _{CCH}	I _F = 0mA, V _O = Open, V _{CC} = 5V	—	10	—	nA
Input Forward Voltage		V _F (*)	I _F = 1.6mA, Ta = 25°C	—	1.65	1.7	V
Input Reverse Breakdown Voltage		BV _R (*)	I _R = 10μA, Ta = 25°C	5	—	—	V
Temperature Coefficient of Forward Voltage		ΔV _F / ΔTa	I _F = 1.6mA	—	-1.9	—	mV / °C
Input Capacitance		C _{IN}	f = 1MHz, V _F = 0	—	60	—	pF
Resistance (Input-Output)		R _{I-O}	V _{I-O} = 500V (Note 7), R.H. ≤ 60%	—	10 ¹²	—	Ω
Capacitance (Input-Output)		C _{I-O}	f = 1MHz (Note 7)	—	0.6	—	pF

(**) JEDEC Registered Data.

(*5) All typicals at Ta = 25°C and V_{CC} = 5V, Unless otherwise noted.

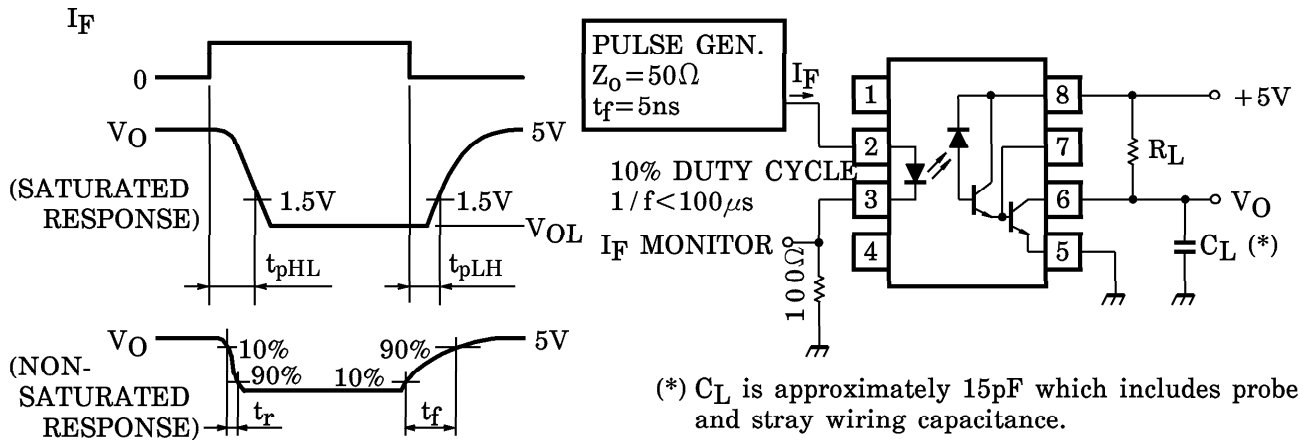
SWITCHING SPECIFICATIONS (Ta = 25°C, VCC = 5V, unless otherwise specified)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time to Logic Low at Output (Note 6, 8)	6N139	t _{pHL} (*)	1	I _F = 0.5mA, R _L = 4.7kΩ	—	5	25	μs
	6N138			I _F = 12mA, R _L = 270Ω	—	0.2	1	
				I _F = 1.6mA, R _L = 2.2kΩ	—	1	10	
Propagation Delay Time to Logic High at Output (Note 6, 8)	6N138	t _{pLH} (*)	1	I _F = 0.5mA, R _L = 4.7kΩ	—	5	60	μs
	6N139			I _F = 12mA, R _L = 270Ω	—	1	7	
				I _F = 1.6mA, R _L = 2.2kΩ	—	4	35	
Common Mode Transient Immunity at Logic High Level Output (Note 9)		CM _H	2	I _F = 0mA, R _L = 2.2kΩ V _{CM} = 400V _{p-p}	—	500	—	V / μs
Common Mode Transient Immunity at Logic Low Level Output (Note 9)		CM _L	2	I _F = 1.6mA R _L = 2.2kΩ V _{CM} = 400V _{p-p}	—	-500	—	V / μs

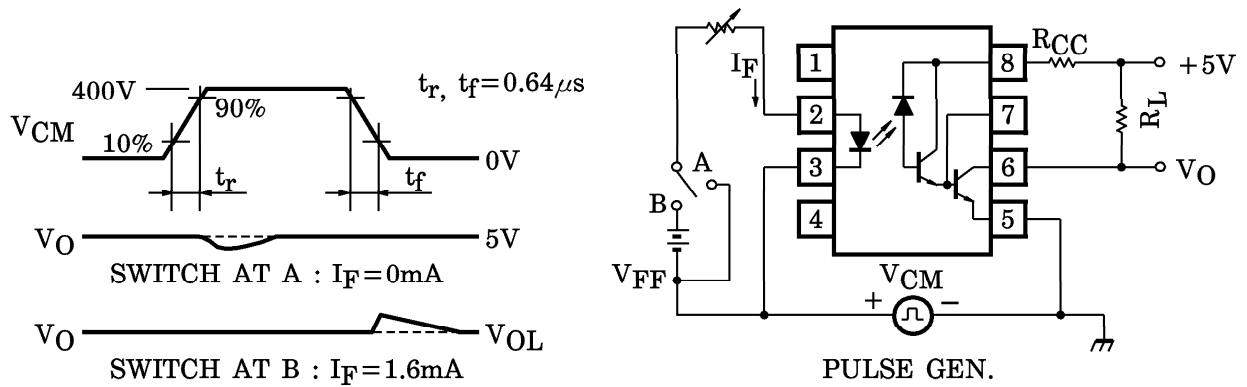
(*)JEDEC Registered Data.

- (Note 1) Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
 (Note 2) Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
 (Note 3) Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
 (Note 4) Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
 (Note 5) DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
 (Note 6) Pin 7 Open.
 (Note 7) Device considered a two-terminal device : Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
 (Note 8) Use of a resistor between pin 5 and 7 will decrease gain and delay time.
 (Note 9) Common mode transient immunity in Logic High level is the maximum tolerable (positive) dv_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V).
 Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dv_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).

TEST CIRCUIT 1.



TEST CIRCUIT 2.



RESTRICTIONS ON PRODUCT USE

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