



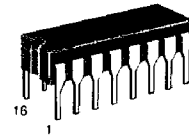
MC14569B

PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BINARY/BCD DOWN COUNTER

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14568B, MC14522B or MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOIC
CASE 751G

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

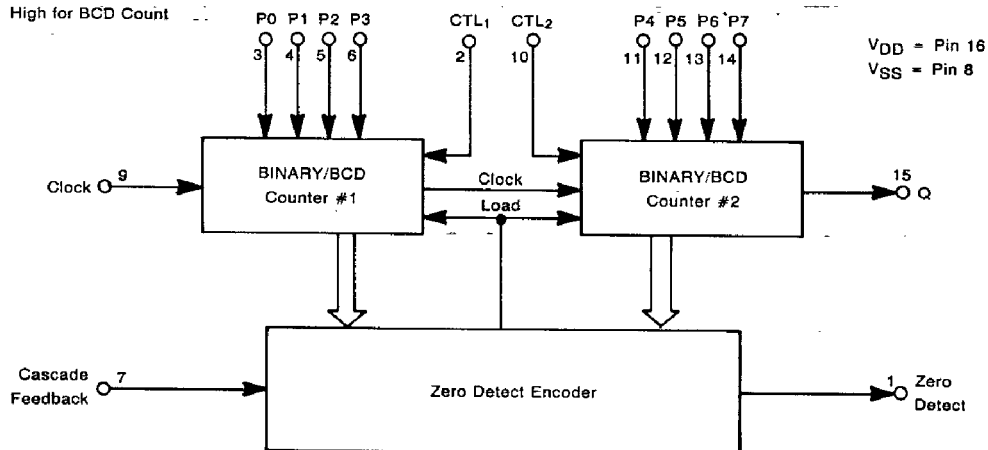
ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBDW SOIC

T_A = -55° to 125°C for all packages.

BLOCK DIAGRAM

CTL = Low for Binary Count
CTL = High for BCD Count



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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V _{in} = 0 or V _{DD}	V _{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	V _{IH}	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc
		10	-0.64	—	-0.51	-0.88	—	-0.36	—	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
15	4.2	—	3.4	—	8.8	—	2.4	—		
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (0.58 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (1.20 μA/kHz) f + I _{DD}							
		15	I _T = (1.95 μA/kHz) f + I _{DD}							

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

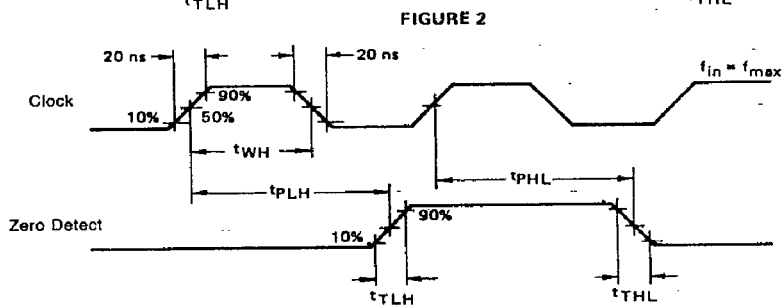
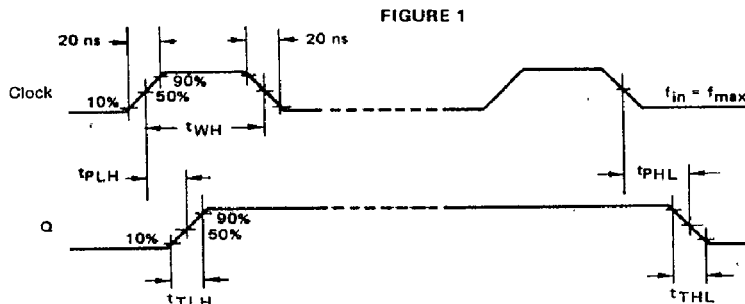
MC14569B

SWITCHING CHARACTERISTICS* ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit	
			Min	Typ #	Max		
Output Rise Time	t_{TLH}	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Output Fall Time	t_{THL}	5.0	—	100	200	ns	
		10	—	50	100		
		15	—	40	80		
Turn-On Delay Time Zero Detect Output	t_{PLH}	5.0	—	420	700	ns	
		10	—	175	300		
		15	—	125	250		
	Q Output	t_{PLH}	5.0	—	675	1200	ns
			10	—	285	500	
			15	—	200	400	
Turn-Off Delay Time Zero Detect Output	t_{PHL}	5.0	—	380	600	ns	
		10	—	150	300		
		15	—	100	200		
	Q Output	t_{PHL}	5.0	—	530	1000	ns
			10	—	225	400	
			15	—	155	300	
Clock Pulse Width	t_{WH}	5.0	300	100	—	ns	
		10	150	45	—		
		15	115	30	—		
Clock Pulse Frequency	f_{cl}	5.0	—	3.5	2.1	MHz	
		10	—	9.5	5.7		
		15	—	13.0	7.8		
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0	NO LIMIT			μs	
		10					
		15					

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS



MC14569B

PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) — Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) — Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) — Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) — This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) — Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) — This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

CTL₁ (Pin 2) — This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

CTL₂ (Pin 10) — This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

V_{SS} (Pin 18) — Negative Supply Voltage. This pin is usually connected to ground.

V_{DD} (Pin 16) — Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 volts to 18.0 volts.

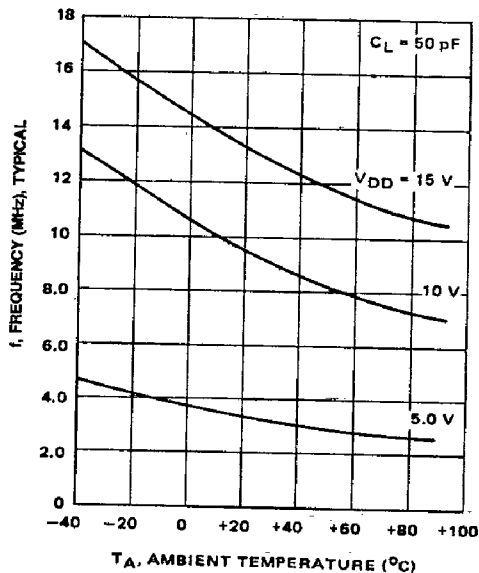
OPERATING CHARACTERISTICS

The MC14569B is a programmable divide-by-N dual 4-bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL₁ and CTL₂.

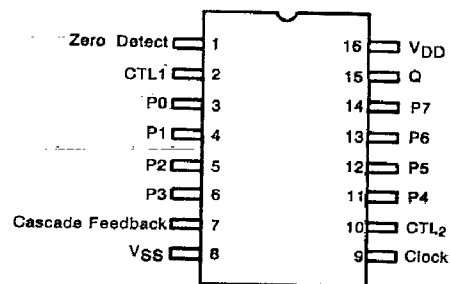
The divide ratio N (N being the value programmed on the preset inputs P0 to P7) is automatically loaded into the counter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock

cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14568B, MC14522B or the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to V_{DD}.



PIN ASSIGNMENT



MC14569B

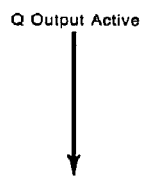
TABLE 1 — MODE CONTROLS (Cascade Feedback = Low)

Counter Control Values		Divide Ratio	
CTL ₁	CTL ₂	Zero Detect	Q
0	0	256	256
0	1	160	160
1	0	160	160
1	1	100	100

Note: Data Preset Inputs (P0-P7) are "Don't Cares" while Cascade Feedback is Low.

TABLE 2 — MODE CONTROLS (CTL₁ = Low, CTL₂ = Low, Cascade Feedback = High)

Preset Inputs								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	
0	0	0	0	0	0	0	0	256	256	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	X	
.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	X	
.	X	
0	0	1	0	0	0	0	0	32	X	
.	X	
.	X	
0	1	0	0	0	0	0	0	64	X	
.	X	
.	X	
0	1	1	1	1	1	1	1	127	X	
1	0	0	0	0	0	0	0	128	128	
.	
.	
1	0	0	0	1	0	0	0	136	136	
.	
.	
1	1	1	1	1	1	1	1	255	255	
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰			Bit Value
128	64	32	16	8	4	2	1			Counting Sequence
Counter #2 Binary				Counter #1 Binary						



X = No Output (Always Low)

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TABLE 4 — MODE CONTROLS (CTL₁ = Low, CTL₂ = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect.	Q	
0	0	0	0	0	0	0	0	160	160	Max Count Illegal State Min Count
0	0	0	0	0	0	0	1	X	X	
0	0	0	0	0	0	1	0	2	X	
0	0	0	0	0	0	1	1	3	X	
.	X	
.	X	
0	0	0	0	1	1	1	1	15	X	
0	0	0	1	0	0	0	0	16	X	
.	X	
.	X	
0	0	0	1	1	1	1	1	31	X	
0	0	1	0	0	0	0	0	32	X	
.	X	
.	X	
0	0	1	1	0	0	0	0	48	X	
.	
0	1	0	0	0	0	0	0	64	X	
.	
0	1	0	1	0	0	0	0	80	X	
.	
0	1	1	1	0	0	0	0	112	X	
.	
1	0	0	0	0	0	0	0	128	128	Q Output Active ↓
.	
1	0	0	1	0	0	0	0	144	144	
.	
1	0	0	1	1	1	1	1	159	159	
2 ⁷ 128	2 ⁶ 64	2 ⁵ 32	2 ⁴ 16	2 ³ 8	2 ² 4	2 ¹ 2	2 ⁰ 1			Bit Value
Counter #2 BCD				Counter #1 Binary						Counting Sequence

X = No Output (Always Low)



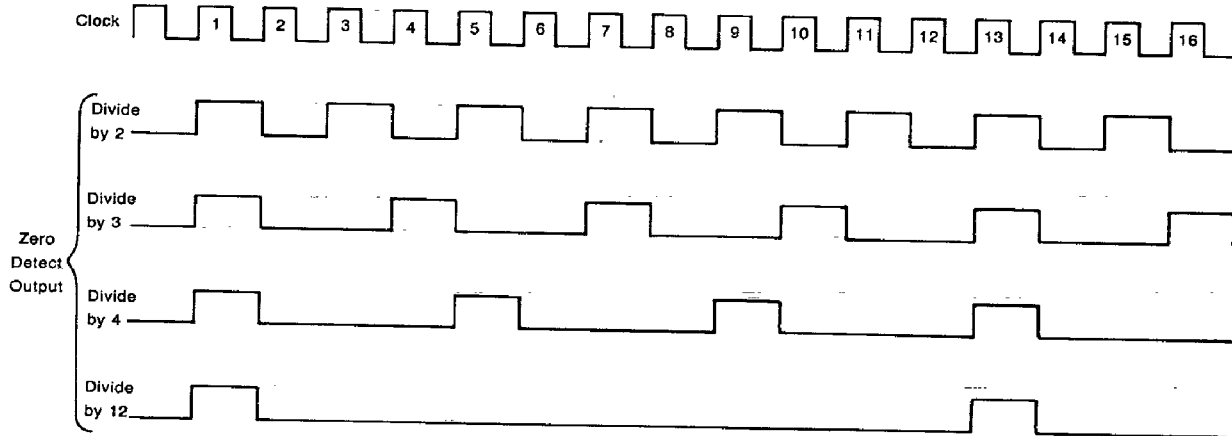
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TABLE 5 — MODE CONTROLS (CTL₁ = High, CTL₂ = High, Cascade Feedback = High)

Preset Values								Divide Ratio		Comments	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q		
0	0	0	0	0	0	0	0	100	100	Max Count Illegal State Min Count	
0	0	0	0	0	0	0	1	X	X		
0	0	0	0	0	0	1	0	2	X		
0	0	0	0	0	0	1	1	3	X		
.	X		
.	X		
.	X		
0	0	0	0	1	0	0	0	9	X		
0	0	0	1	0	0	0	0	10	X		
.	X		
.	X		
0	0	1	1	0	0	0	0	30	X		
.	X		
.	X		
0	1	0	0	0	0	0	0	40	X		
.	X		
.	X		
0	1	0	1	0	0	0	0	50	X		
.	X		
.	X		
0	1	1	1	0	0	0	0	70	X		
.	X		
.	X		
1	0	0	0	0	0	0	0	80	80	Q Output Active	
.		
.		
1	0	0	1	0	0	0	0	90	90		
.		
.		
1	0	0	1	1	0	0	1	99	99		
Counter #2 BCD				Counter #1 BCD						Bit Value	
										Counting Sequence	

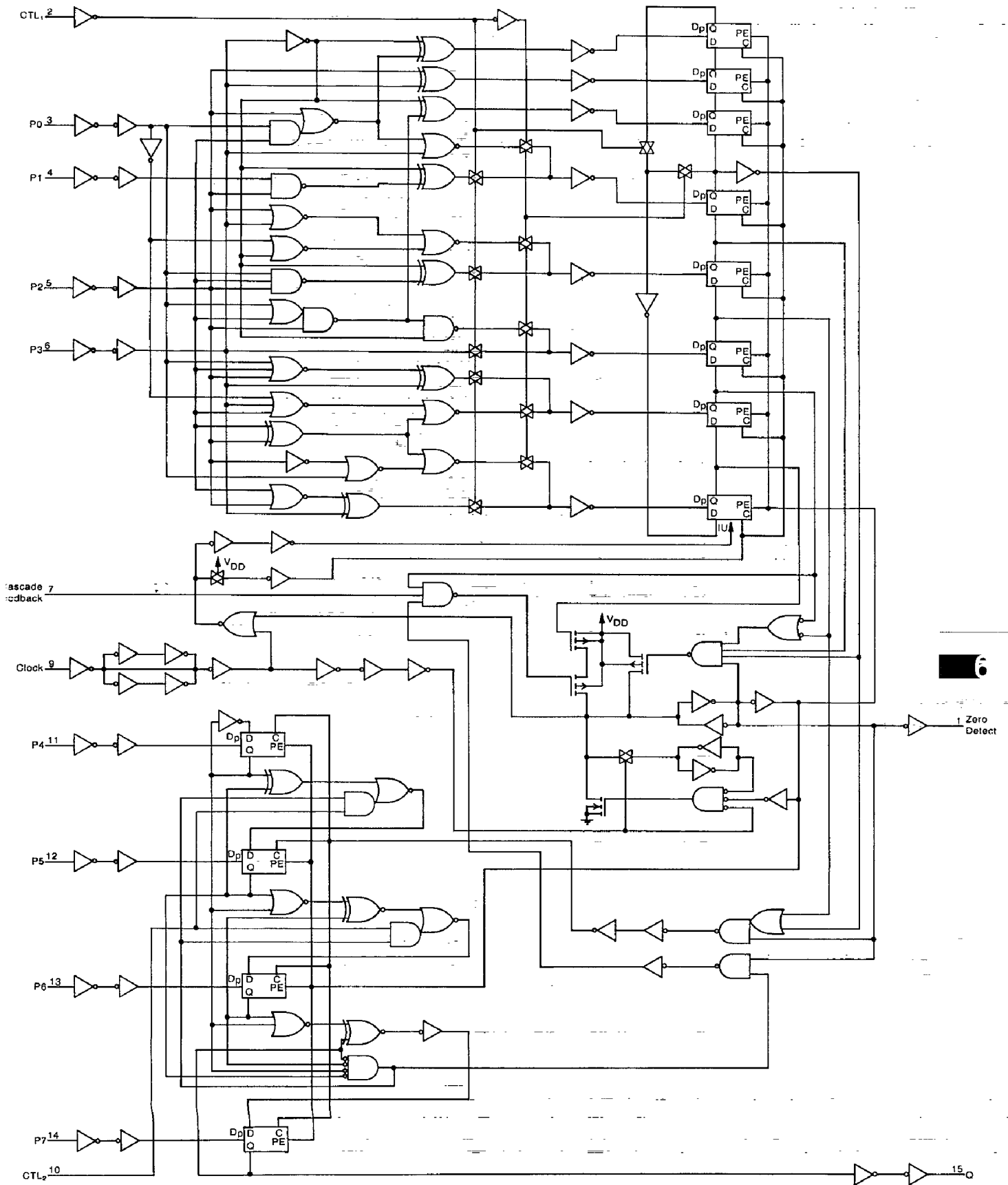
X = No Output (Always Low)

TIMING DIAGRAM MC14569B



MC14569B

LOGIC DIAGRAM



MC14569B

TYPICAL APPLICATIONS

FIGURE 6 — CASCADING MC14568B AND MC14522B OR MC14526B WITH MC14569B

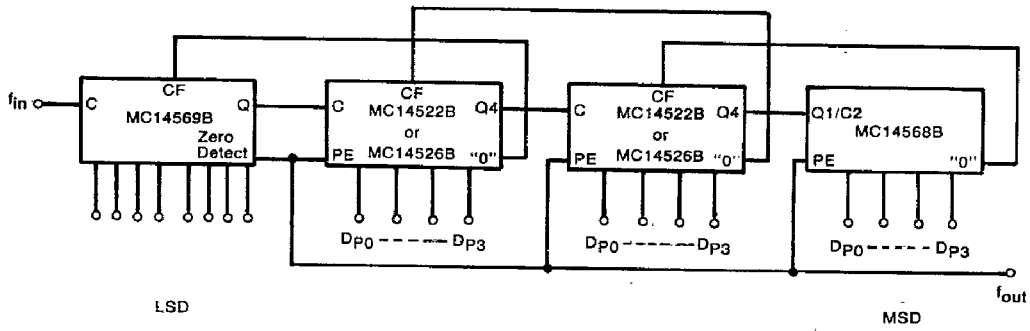
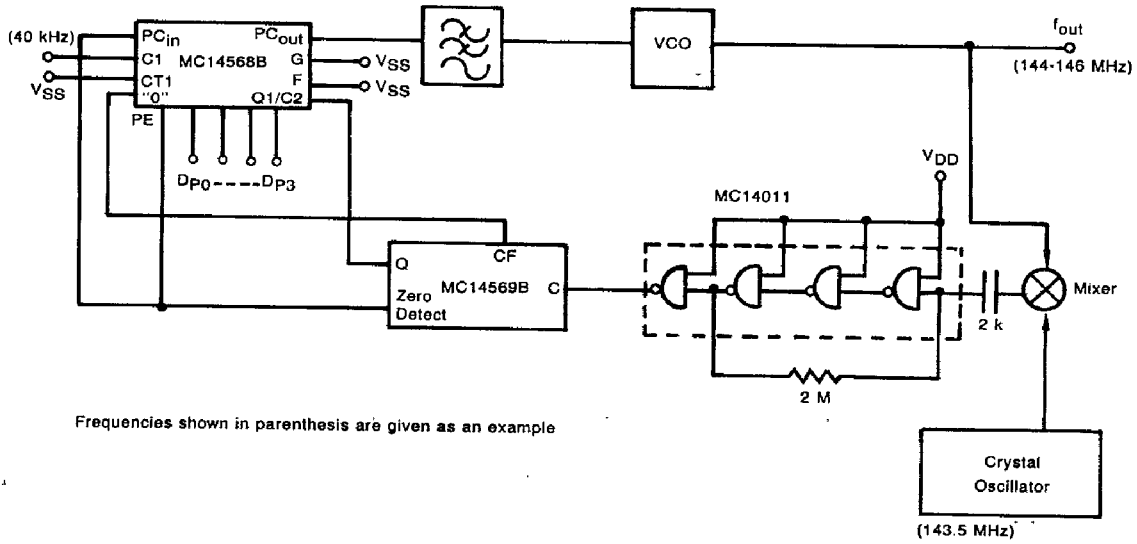


FIGURE 7 — FREQUENCY SYNTHESIZER WITH MC14568B and MC14569B USING A MIXER (Channel Spacing 10 kHz)



Frequencies shown in parenthesis are given as an example