CMOS Triple AND/OR Bi-Phase Pairs

The RCA-CD4037A consists of three AND/OR pairs driven by common control signals A and B.

Each circuit has a data input (C), and two output terminals (D and E) that provide outputs in accordance with the truth table shown in Fig. 1. The circuit is useful for coding or decoding signals for split-phase (Bi-phase) communication systems, magnetic recording, and plated wire and core memory systems. A separate V_{CC} terminal is provided to allow level conversion to any voltage from 3 volts to V_{DD}.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

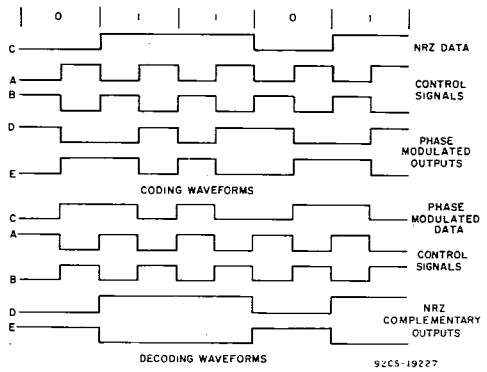
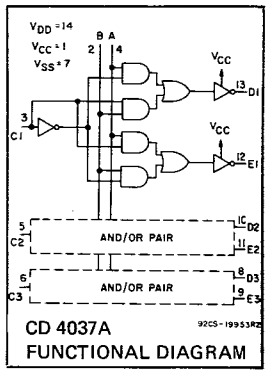
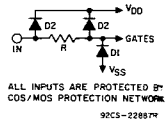


Fig. 1 — Coding and decoding waveforms.



TRUTH TABLE

INPUT		OUTPUT	
A	B	D	E
0	0	I	I
I	0	C	$\overline{C}$
0	I	$\overline{C}$	C
I	I	0	0



RECOMMENDED OPERATING CONDITIONS. For maximum reliability, nominal operating conditions should be selected to that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

CAUTION: V_{CC} VOLTAGE LEVEL MUST BE EQUAL TO OR LESS POSITIVE THAN V_{DD}

DYNAMIC ELECTRICAL CHARACTERISTICS
at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H PACKAGES			E PACKAGE			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: A and B Inputs t_{PHL}, t_{PLH}	5	–	225	450	–	325	650	ns
	10	–	75	150	–	100	200	
C Inputs t_{PHL}	5	–	250	500	–	350	700	ns
	10	–	75	150	–	100	200	
t_{PLH}	5	–	225	450	–	325	650	
	10	–	90	180	–	125	250	
Transition Time: High-to-Low Level, t_{THL}	5	–	40	80	–	60	120	ns
	10	–	15	30	–	20	40	
Low-to-High Level, t_{TLH}	5	–	75	150	–	100	200	ns
	10	–	60	120	–	90	180	
Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

Features:

- **Outputs compatible with low-power TTL systems.**
- **High sink and source current (1.6 mA typ.) capability at $V_{DD} = V_{CC}$ = 10V and V_{DS} = 0.5 V.**
- **Microwatt quiescent power dissipation: P_D = 0.5 μW/ceramic pkg. (typ.), P_D = 2 μW/plastic pkg. (typ.) at V_{DD} = 10 V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Split-phase (Bi-Phase) communication systems.**
- **Disc, drum, and tape digital recording systems.**
- **Plated wire and core memory systems.**
- **High-to-low logic level converter.**

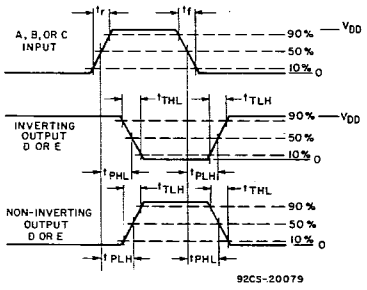


Fig. 2 — Waveforms for measurement of dynamic characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150° C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125° C
PACKAGE TYPE E . . . . . -40 to +85° C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
FOR T_A = -40 to +60° C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85° C (PACKAGE TYPE E) . . Derate Linearly at 12 mW/° C to 200 mW
FOR T_A = -55 to +100° C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125° C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265° C

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, K, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	–	5	0.85	0.7	1.2	0.45	0.4	0.35	0.7	0.3	mA
I_DN Min.	0.5	–	10	1.3	1.1	2	0.7	0.65	0.55	1.1	0.45	
P-Channel (Source):	4.5	–	5	-0.65	-0.55	-1	-0.35	-0.35	-0.3	-0.55	-0.2	
I_DP Min.	9.5	–	10	-0.9	-0.75	-1.6	-0.45	-0.5	-0.4	-0.75	-0.3	
Input Leakage Current,	Any Input											μA
I_{IL}, I_{IH}	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

For quiescent device current, noise immunity, and input leakage current test circuits see "Ratings and Characteristics" at the beginning of the CMOS section.

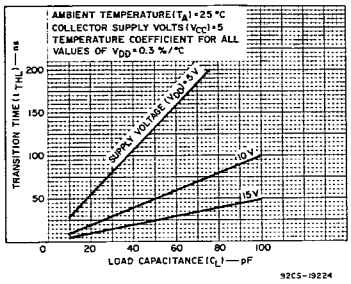


Fig. 3 — Typical transition time vs. load capacitance.

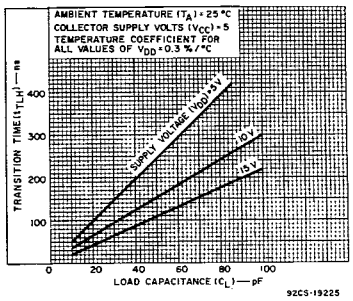


Fig. 4 — Typical transition time vs. load capacitance.

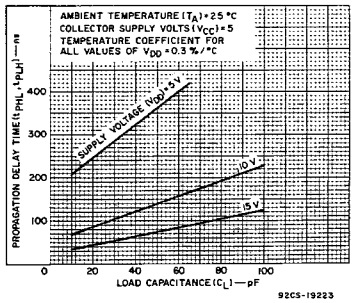


Fig. 5 — Typical propagation delay time vs. load capacitance.

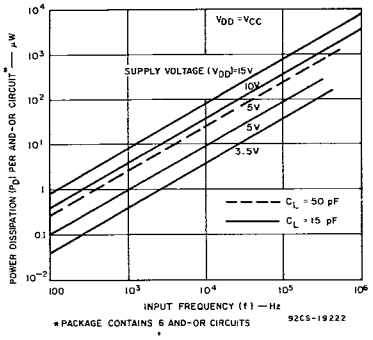


Fig. 6 — Typical dissipation characteristics.