

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4031B

MSI

64-stage static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

64-stage static shift register

HEF4031B MSI

DESCRIPTION

The HEF4031B is an edge-triggered 64-stage static shift register with two serial data inputs (D_A , D_B), a data select input \bar{A}/B , a clock input (CP), a buffered clock output (CO), and buffered outputs from the 64th bit position (O_{63} , \bar{O}_{63}). The output O_{63} is capable of driving one TTL load.

Data from D_A or D_B , as determined by the state of \bar{A}/B , is shifted into the first shift register position and all the data in

the register is shifted one position to the right on the LOW to HIGH transition of CP. D_A is selected by a LOW, and D_B by a HIGH on \bar{A}/B . Registers can be cascaded either by connecting all CP inputs together or by driving CP of the most right-hand register with the system clock and connecting CO to CP of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store O_{63} of the most right-hand register until the most left-hand register is clocked.

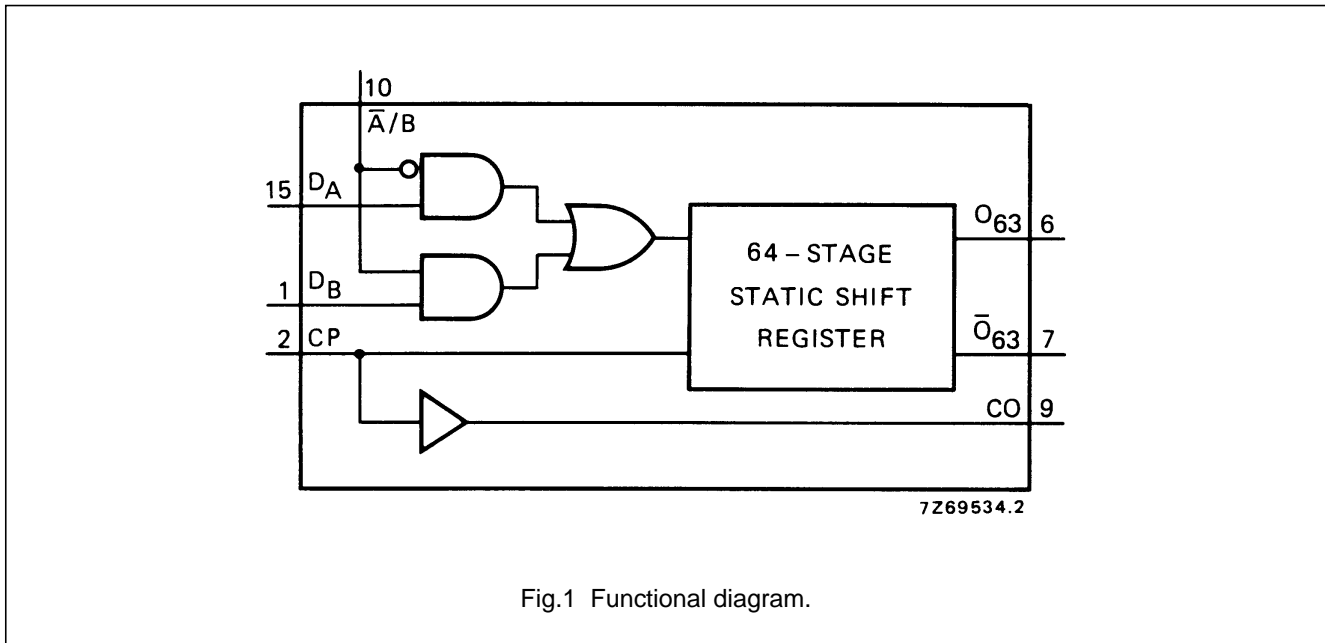


Fig.1 Functional diagram.

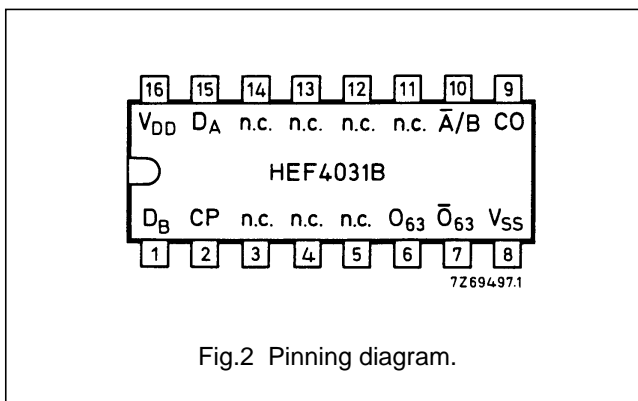


Fig.2 Pinning diagram.

PINNING

- D_A , D_B data inputs
- \bar{A}/B data select input
- CP clock input (LOW to HIGH edge-triggered)
- CO buffered clock output
- O_{63} buffered output from the 64th stage
- \bar{O}_{63} complementary buffered output from the 64th stage

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4031BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4031BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4031BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

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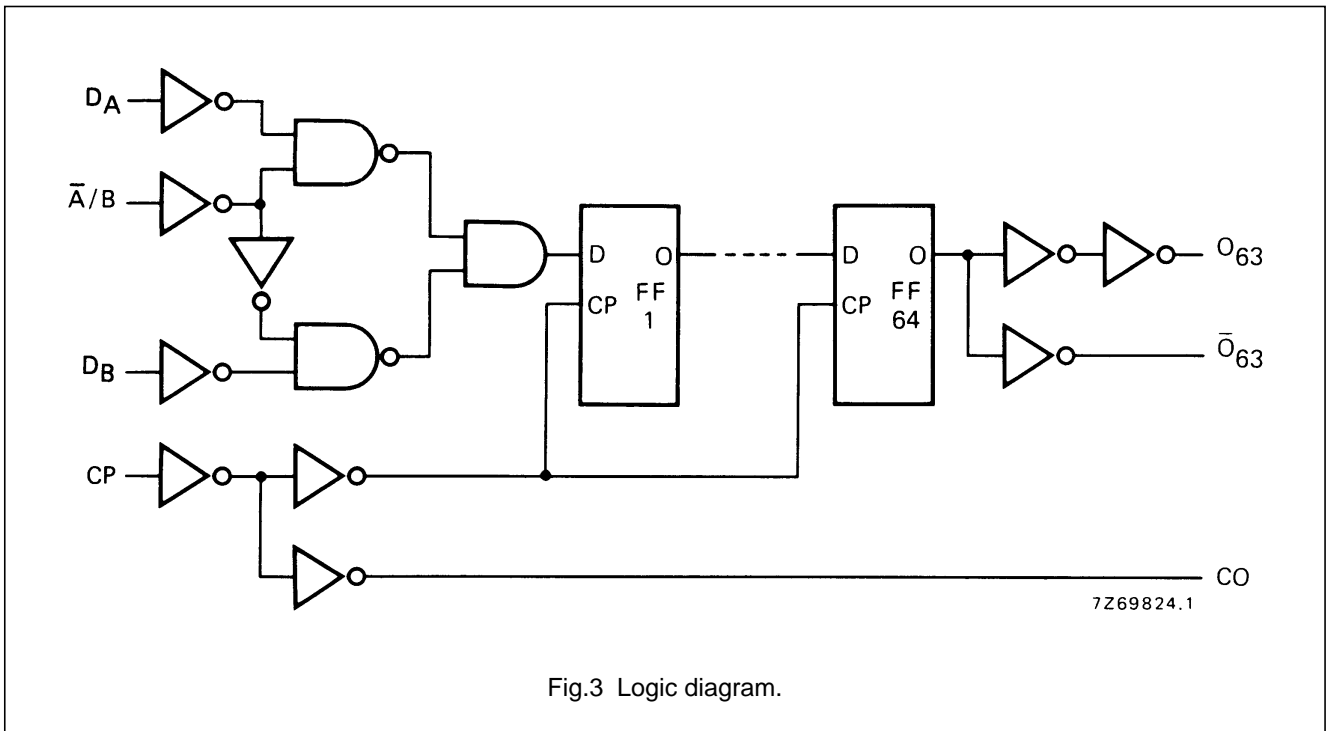


Fig.3 Logic diagram.

DC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD}

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	T_{amb} (°C)						
					-40		+ 25		+ 85		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (source) current HIGH; O_{63}	5	4, 6			1,0	0,85	0,65				mA
	10	9,5		$-I_{OH}$	3,0	2,5	2,0				mA
	15	13,5			10,0	8,5	6,5				mA
Output (sink) current LOW; O_{63}	5	2,5		$-I_{OH}$	3,0	2,5	2,0				mA
	4,75		0,4		2,7	2,3	1,8				mA
	10		0,5	I_{OL}	9,5	8,0	6,3				mA
	15		1,5		24,0	20,0	16,0				mA

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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA					
Propagation delays	5	t_{PHL}			ns						
							CP \rightarrow O_{63}	180	360	167 ns + (0,26 ns/pF) C_L	
							HIGH to LOW	65	130	57 ns + (0,16 ns/pF) C_L	
	5	t_{PLH}			ns						
								LOW to HIGH	170	340	148 ns + (0,45 ns/pF) C_L
									65	130	56 ns + (0,19 ns/pF) C_L
	10	t_{PHL}			ns						
								HIGH to LOW	45	90	40 ns + (0,11 ns/pF) C_L
									190	380	163 ns + (0,55 ns/pF) C_L
	10	t_{PLH}			ns						
								LOW to HIGH	75	150	64 ns + (0,23 ns/pF) C_L
									45	90	39 ns + (0,13 ns/pF) C_L
15	t_{PHL}			ns							
							HIGH to LOW	190	380	163 ns + (0,55 ns/pF) C_L	
								75	150	64 ns + (0,23 ns/pF) C_L	
15	t_{PLH}			ns							
							LOW to HIGH	50	100	42 ns + (0,16 ns/pF) C_L	
								190	380	163 ns + (0,55 ns/pF) C_L	
15	t_{PHL}			ns							
							CP \rightarrow \overline{O}_{63}	70	140	43 ns + (0,55 ns/pF) C_L	
							HIGH to LOW	35	70	24 ns + (0,23 ns/pF) C_L	
15	t_{PLH}			ns							
							LOW to HIGH	25	50	17 ns + (0,16 ns/pF) C_L	
								55	110	28 ns + (0,55 ns/pF) C_L	
15	t_{PLH}			ns							
							CP \rightarrow CO	30	60	19 ns + (0,23 ns/pF) C_L	
							HIGH to LOW	25	50	17 ns + (0,16 ns/pF) C_L	
15	t_{PLH}			ns							
							LOW to HIGH	55	110	28 ns + (0,55 ns/pF) C_L	
								30	60	19 ns + (0,23 ns/pF) C_L	
Output transition times; O_{63}	5	t_{THL}			ns						
							HIGH to LOW	25	50	5 ns + (0,40 ns/pF) C_L	
								12	24	3 ns + (0,18 ns/pF) C_L	
	10	t_{TLH}			ns						
								LOW to HIGH	40	80	8 ns + (0,65 ns/pF) C_L
									20	40	5 ns + (0,30 ns/pF) C_L
15	t_{TLH}			ns							
							HIGH to LOW	13	26	3 ns + (0,20 ns/pF) C_L	
								60	120	10 ns + (1,0 ns/pF) C_L	
15	t_{THL}			ns							
							Output transition times; \overline{O}_{63} , CO	30	60	9 ns + (0,42 ns/pF) C_L	
							HIGH to LOW	20	40	6 ns + (0,28 ns/pF) C_L	
15	t_{TLH}			ns							
							LOW to HIGH	60	120	10 ns + (1,0 ns/pF) C_L	
								30	60	9 ns + (0,42 ns/pF) C_L	
15	t_{TLH}			ns							
							LOW to HIGH	20	40	6 ns + (0,28 ns/pF) C_L	
								60	120	10 ns + (1,0 ns/pF) C_L	

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Set-up times D _A , D _B → CP A̅/B → CP	5	t _{su}	25	0	ns	see also waveforms Fig.4
	10		25	-5	ns	
	15		10	-10	ns	
	5	t _{su}	30	10	ns	
	10		15	0	ns	
	15		10	-5	ns	
Hold times D _A , D _B → CP A̅/B → CP	5	t _{hold}	40	10	ns	
	10		40	10	ns	
	15		40	10	ns	
	5	t _{hold}	40	10	ns	
	10		40	10	ns	
	15		40	10	ns	
Minimum clock pulse width; LOW	5	t _{WCPL}	180	90	ns	
	10		70	35	ns	
	15		50	25	ns	
Maximum clock pulse frequency	5	f _{max}	2,5	5	MHz	
	10		7	14	MHz	
	15		10	20	MHz	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	4000 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	19 000 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	54 000 f _i + ∑ (f _o C _L) × V _{DD} ²	

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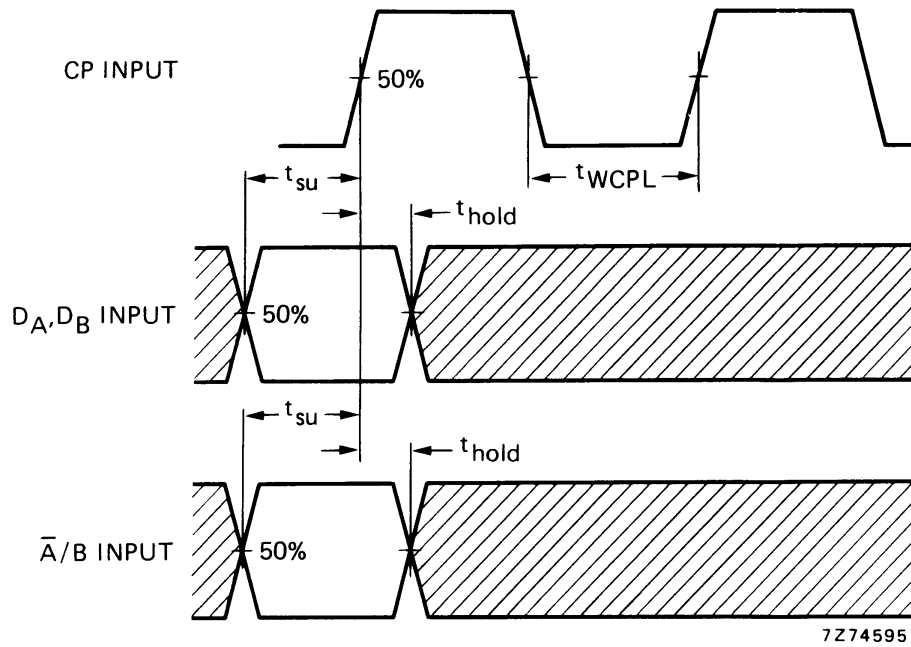


Fig.4 Waveforms showing minimum clock pulse width, set-up and hold times for D_A, D_B to CP and \bar{A}/B to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

An example of an application for the HEF4031B is:

- Serial shift register.

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APPLICATION INFORMATION

