Z86L04/L08

Z8 8-BIT COST-EFFECTIVE MICROCONTROLLERS

FEATURES

Device	ROM (KB)	RAM* (Bytes)	Speed (MHz)	Auto Latch	Permanent WDT
Z86L04	1K	125	8	Optional	Optional
Z86L08	2K	125	8	Optional	Optional

Note: *General-Purpose

- 18-Pin DIP and SOIC Packages
- 0 °C to + 70 °C Standard Temperature
- 2.0V to 3.9V Operating Range
- 14 Input / Output Lines
- Five Vectored, Prioritized Interrupts from Five Different Sources
- Two On-Board Comparators
- Software Enabled Watch-Dog Timer (WDT)
- Programmable Interrupt Polarity
- Two Standby Modes: STOP and HALT
- Low-Voltage Protection
- ROM Mask/OTP Options:
  - ROM Protect
  - Auto Latch Disable
  - Permanent Watch-Dog Timer (WDT)
  - RC Oscillator
  - 32 kHz Crystal Operation
  - Low EMI
  - WDT Clock Source (Z86L04 only)
- Two Programmable 8-Bit Counter/Timers with 6-Bit Programmable Prescalers
- Power-On Reset (POR) Timer
- On-Chip Oscillator that Accepts RC, Crystal, Ceramic Resonator, LC, or External Clock Drive
- Clock-Free WDT Reset
- Low-Power Consumption (40 mw)
- Fast Instruction Pointer (1.5 µs @ 8 MHz)
- Fourteen Digital Inputs at CMOS Levels; Schmitt-Triggered

GENERAL DESCRIPTION

Zilog's Z86L04/L08 microcontrollers (MCUs) are members of the Z8 single-chip MCU family, which offer easy software/hardware system expansion.

For applications demanding powerful I/O capabilities, the MCU's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

One on-chip counter/timer, with a large number of user-selectable modes, off-load the system of administering real-time tasks such as counting/timing and I/O data communications. Additionally, two on-board comparators process analog signals with a common reference voltage (Figure 1).

GENERAL DESCRIPTION (Continued)

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

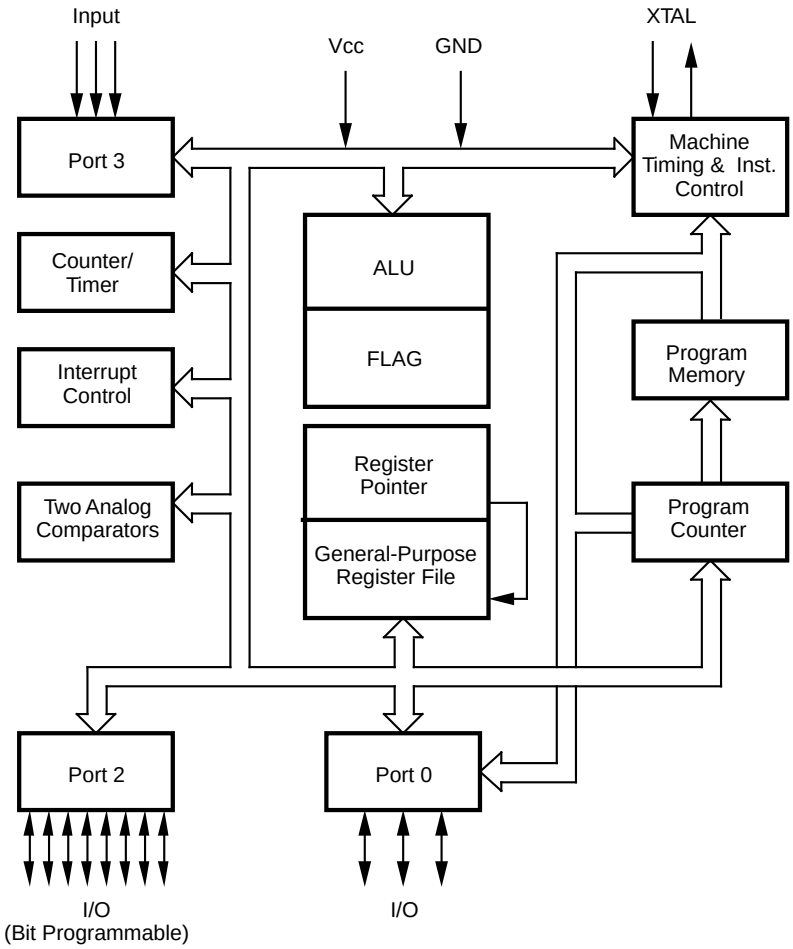


Figure 1. Z86L04/L08 Functional Block Diagram

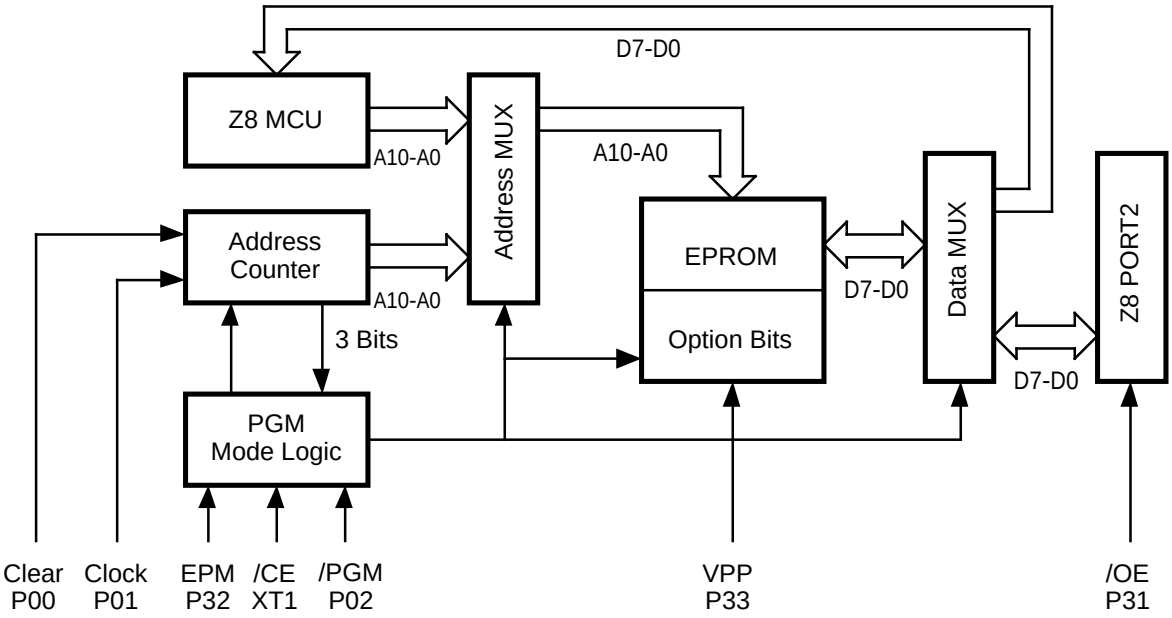


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTIONS

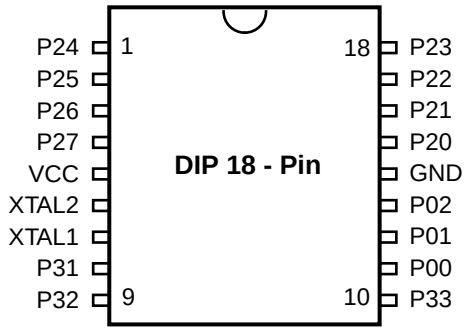


Figure 3. 18-Pin Standard Mode Configuration

Table 1. 18-Pin Standard Mode Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4, 5, 6, 7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Oscillator Clock	Output
7	XTAL1	Crystal Oscillator Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0, 1, 2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0, 1, 2, 3	In/Output

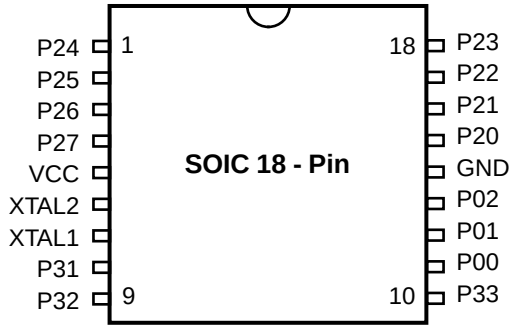


Figure 4. 18-Pin SOIC Configuration

Table 2. 18-Pin SOIC Pin Identification

Pin #	Symbol	Function	Direction
1-4	P24-P27	Port 2, Pins 4,5,6,7	In/Output
5	V_{CC}	Power Supply	
6	XTAL2	Crystal Osc. Clock	Output
7	XTAL1	Crystal Osc. Clock	Input
8	P31	Port 3, Pin 1, AN1	Input
9	P32	Port 3, Pin 2, AN2	Input
10	P33	Port 3, Pin 3, REF	Input
11-13	P00-P02	Port 0, Pins 0,1,2	In/Output
14	GND	Ground	
15-18	P20-P23	Port 2, Pins 0,1,2,3	In/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Ambient Temperature under Bias	–40	+105	°C
Storage Temperature	–65	+150	°C
Voltage on any Pin with Respect to V_{SS} [Note 1]	–0.7	+12	V
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V
Voltage on Pin 7 with Respect to V_{SS} [Note 2] (Z86C02/L02)	–0.7	V_{DD}+1	V
Voltage on Pin 7,8,9,10 with Respect to V_{SS} [Note 2] (Z86E02)	–0.7	V_{DD}+1	V
Total Power Dissipation		462	mW
Maximum Allowed Current out of V_{SS}		300	mA
Maximum Allowed Current into V_{DD}		270	mA
Maximum Allowed Current into an Input Pin [Note 3]	–600	+600	µA
Maximum Allowed Current into an Open-Drain Pin [Note 4]	–600	+600	µA
Maximum Allowed Output Current Sinked by Any I/O Pin		20	mA
Maximum Allowed Output Current Sourced by Any I/O Pin		20	mA
Maximum Allowed Output Current Sinked by Port 2, Port 0		80	mA
Maximum Allowed Output Current Sourced by Port 2, Port 0		80	mA

Notes:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Total power dissipation should not exceed 462 mW for the package. Power dissipation is calculated as follows:

1. This applies to all pins except where otherwise noted.
2. Maximum current into pin must be ±600 µA. There is no input protection diode from pin to V_{DD}.
3. This excludes Pin 6 and Pin 7.
4. Device pin is not at an output Low state.

Total Power dissipation = V_{DD} x [I_{DD} – (sum of I_{OH})] + sum of [(V_{DD} – V_{OH}) x I_{OH}] + sum of (V_{0L} x I_{0L})

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 5).

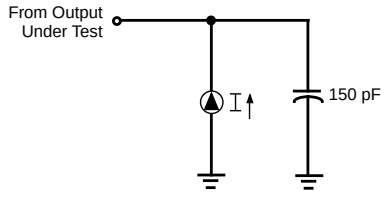


Figure 5. Test Load Diagram

Capacitance

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	15 pF
Output capacitance	0	20 pF
I/O capacitance	0	25 pF

DC CHARACTERISTICS

Z86L04/L08

Sym.	Parameter	V_{CC} [3]	T_A = 0 °C to +70 °C Min	Max	Typical @ 25 °C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	2.0V	0.9 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
		3.9V	0.9 V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.0V	V_{SS}–0.3	0.1 V_{CC}		V	Driven by External Clock Generator	
		3.9V	V_{SS}–0.3	0.1 V_{CC}		V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.0V	0.9 V_{CC}	V_{CC}+0.3		V		1
		3.9V	0.9 V_{CC}	V_{CC}+0.3		V		1
V_{IL}	Input Low Voltage	2.0V	V_{SS}–0.3	0.1 V_{CC}		V		1
		3.9V	V_{SS}–0.3	0.1 V_{CC}		V		1
V_{OH}	Output High Voltage	2.0V	V_{CC}–0.4		3.0	V	I_{OH} = – 500 µA	4,5
		3.9V	V_{CC}–0.4		3.0	V	I_{OH} = – 500 µA	4,5
V_{OL1}	Output Low Voltage	2.0V		0.8	0.2	V	I_{OL} = +1.0 mA	4,5
		3.9V		0.4	0.1	V	I_{OL} = +1.0 mA	4,5
V_{OL2}	Output Low Voltage	2.0V		1.0	0.8	V	I_{OL} = + 3.0 mA	4,5
		3.9V		0.8	0.3	V	I_{OL} = + 3.0 mA	4,5
V_{OFFSET}	Comparator Input Offset Voltage	2.0V		25	10	mV		
		3.9V		25	10	mV		
V_{LV}	V_{CC} Low Voltage Auto Reset		1.4	2.15		V		
I_{IL}	Input Leakage (Input Bias Current of Comparator)	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	2.0V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
		3.9V	–1.0	1.0		µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	2.0 3.9	0 0	V_{CC} –1.0 V_{CC} –1.0		V V		

Sym	Parameter	V_{CC} [3]	T_A = 0 °C to +70 °C Min	Max	Typical @ 25 °C	Units	Conditions	Notes
I_{CC}	Supply Current	2.0V		3.3		mA	@ 2 MHz	5,6
		3.9V		6.8		mA	@ 2 MHz	5,6
		2.0V		6.0		mA	@ 8 MHz	5,6
		3.9V		9.0		mA	@ 8 MHz	5,6
I_{CC1}	Standby Current (Halt Mode)	2.0V		2.3		mA	@ 2 MHz	5,6,7
		3.9V		3.8		mA	@ 2 MHz	5,6,7
		2.0V		3.8		mA	@ 8 MHz	5,6,7
		3.9V		4.8		mA	@ 8 MHz	5,6,7
I_{CC2}	Standby Current (Stop Mode)	2.0V		10	1.0	µA		6,7
		3.9V		10	1.0	µA		6,7
I_{ALL}	Auto Latch Low Current	2.0V		12	3.0	µA	$0V < V_{IN} < V_{CC}$	
		3.9V		32	16	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	2.0V		–8	-1.5	µA	$0V < V_{IN} < V_{CC}$	
		3.9V		–16	-8.0	µA		

Notes:

1. Port 0, 2, and 3 only.
2. V_{SS} = 0V = GND. The device operates down to V_{LV}. The minimum operational V_{CC} is determined by the value of the voltage V_{LV} at the ambient temperature.
3. V_{CC} = 2.0V to 3.9V, typical values measured at V_{CC} = 3.3 V.
4. Standard Mode (not Low EMI mode).
5. Inputs at V_{CC} or V_{SS}, outputs are unloaded.
6. WDT is not running.
7. Comparator inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

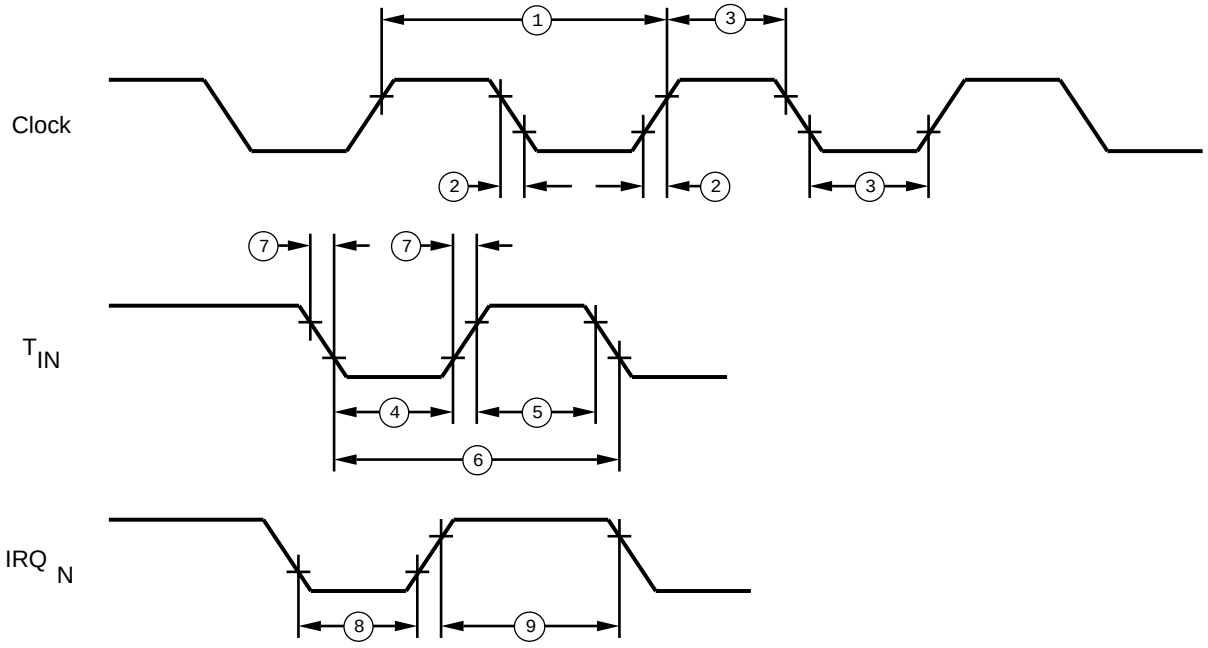


Figure 6. AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A= 0 °C to +70 °C 8 MHz			
No.	**Symbol**	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	2.0V	125	DC	ns	1
			3.9V	125	DC	ns	1
2	TrC,TfC	Clock Input Rise and Fall Times	2.0V		25	ns	1
			3.9V		25	ns	1
3	TwC	Input Clock Width	2.0V	62		ns	1
			3.9V	62		ns	1
4	TwTinL	Timer Input Low Width	2.0V	70		ns	1
			.39V	70		ns	1
5	TwTinH	Timer Input High Width	2.0V	5TpC			1
			3.9V	5TpC			1
6	TpTin	Timer Input Period	2.0V	8TpC			1
			3.9V	8TpC			1
7	TrTin, TtTin	Timer Input Rise and Fall Time	2.0V		100	ns	1
			3.9V		100	ns	1
8	TwIL	Int. Request Input Low Time	2.0V	70		ns	1,2,3
			3.9V	70		ns	1,2,3
9	TwIH	Int. Request Input High Time	3.0V	5TpC			1,2,3
			3.9V	5TpC			1,2,3
10	Twdt	Watch-Dog Timer Delay Time Before Time-Out	2.0V	25		ms	
			3.9V	10		ms	
11	Tpor	Power-On Reset Time	2.0V	70		ms	4
			3.9V	50		ms	4
			2.0V	20		ms	5
			3.9V	6		ms	5

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31).
3. IRQ 0,1,2 only.
4. For Z86L08 using internal RC oscillator.
5. For Z86L04 using internal RC oscillator.

Precaution: Maximum frequency in Low EMI mode is 1 MHz.

PIN FUNCTIONS

XTAL1, XTAL2 Crystal In, Crystal Out (time-based input and output, respectively). These pins connect a parallel-resonant crystal, LC, RC, or an external single-phase clock (8 MHz max) to the on-chip clock oscillator and buffer.

Port 0, P02-P00. Port 0 is a 3-bit bidirectional, Schmitt-triggered CMOS compatible I/O port. These three I/O lines can be globally configured under software control to be inputs or outputs (Figure 7).

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33, P32, P31) that are not externally driven. A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer. On Power-up and Reset, the Auto Latch will set the ports to an undetermined state of 0 or 1. Default condition is Auto Latches enabled.

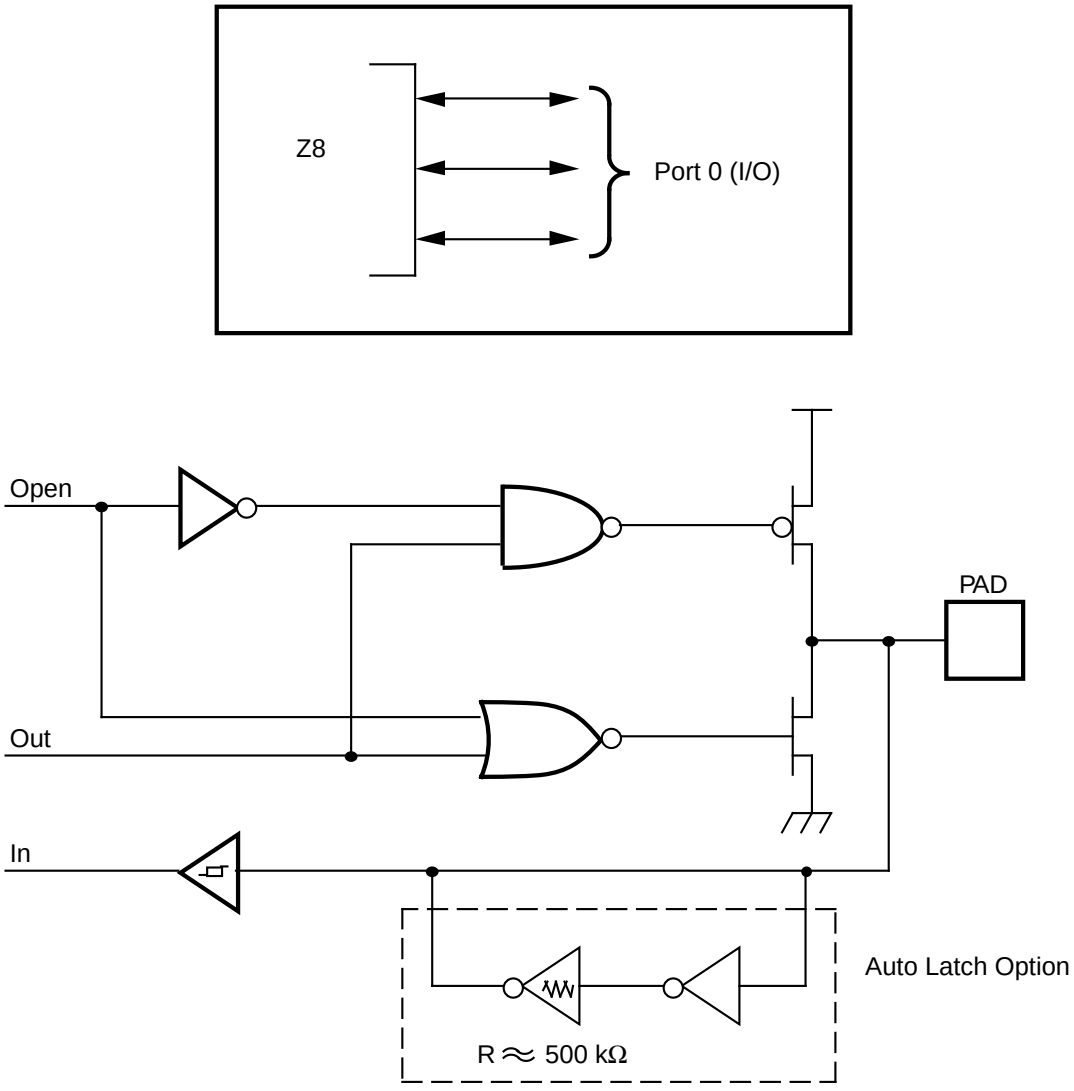


Figure 7. Port 0 Configuration

Port 2, P27-P20. Port 2 is an 8-bit, bit-programmable, bidirectional, Schmitt-triggered, CMOS, compatible I/O port. These eight I/O lines can be configured under software control to be inputs or outputs, independently. Bits programmed as outputs can be globally programmed as either push-pull or open-drain (Figure 8).

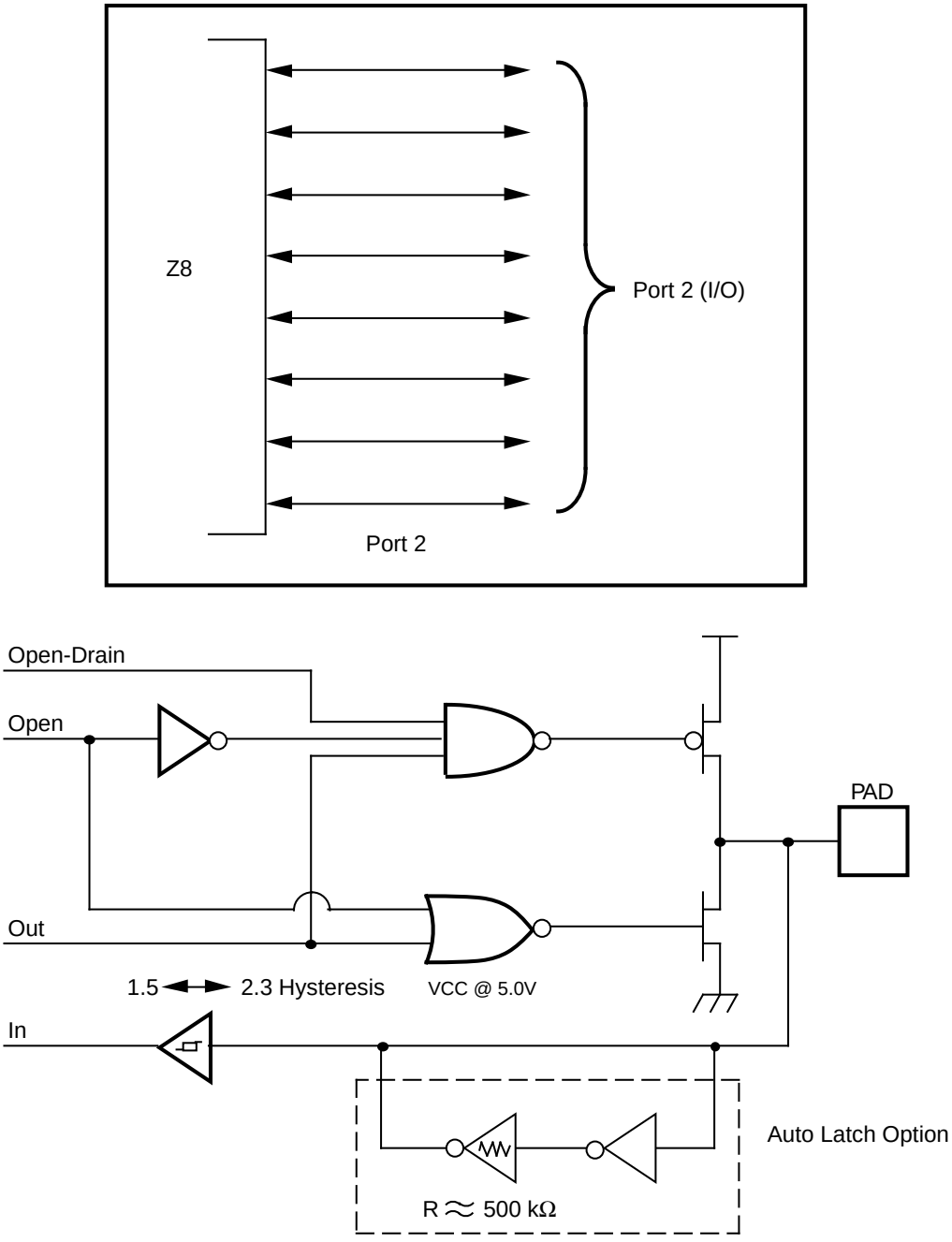


Figure 8. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3, P33-P31. Port 3 is a 3-bit, CMOS, compatible port with three fixed input (P33-P31) lines. These three input lines can be configured under software control as digital Schmitt-trigger inputs or analog inputs. These three input lines are also used as the interrupt sources IRQ0-IRQ3 and as the timer input signal T_{IN} (Figure 9).

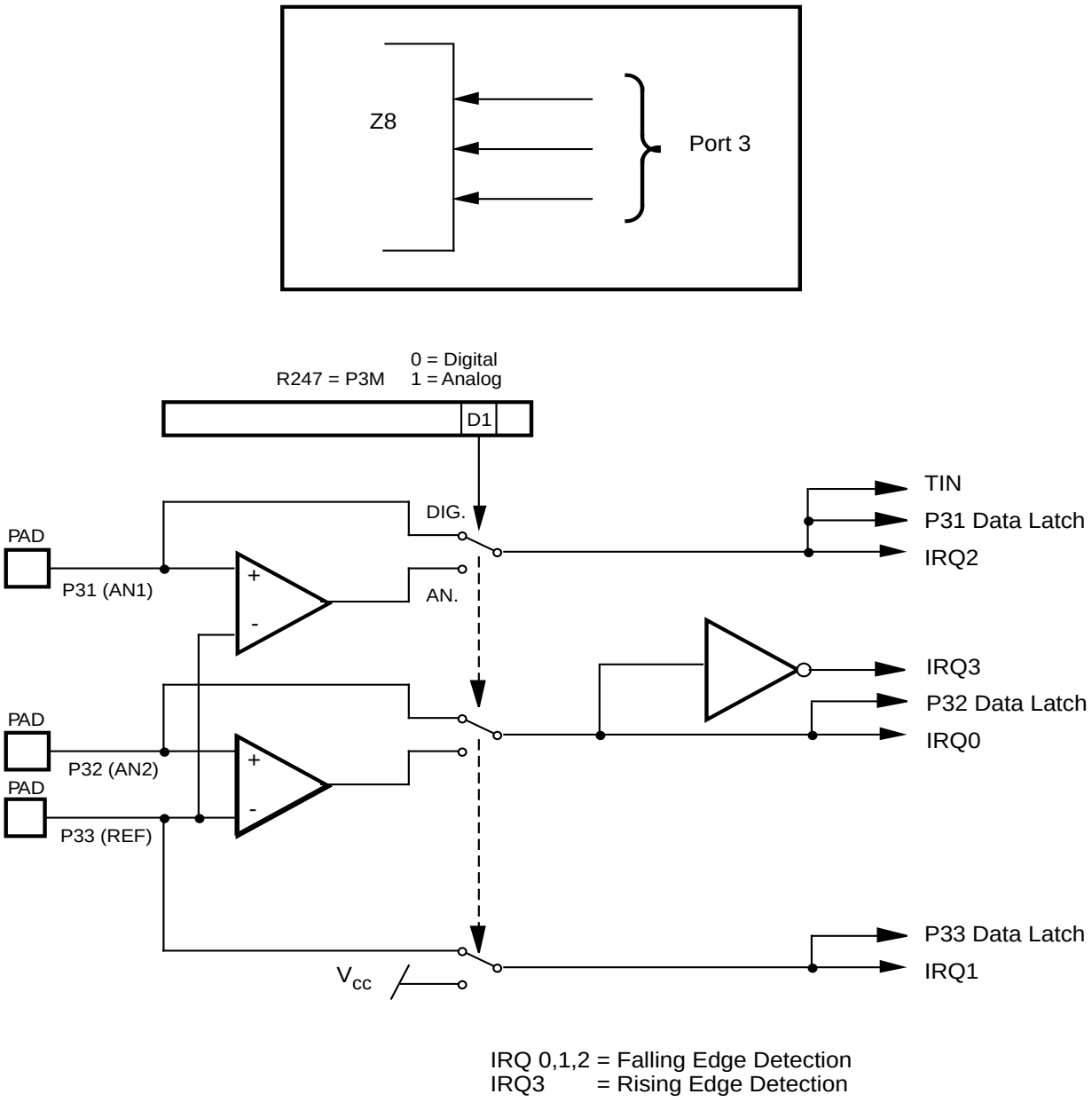


Figure 9. Port 3 Configuration

Comparator Inputs. Two analog comparators are added to input of Port 3, P31 and P32, for interface flexibility. The comparators reference voltage P33 (REF) is common to both comparators.

Typical applications for the on-board comparators; Zero crossing detection, A/D conversion, voltage scaling, and threshold detection. In analog mode, P33 input functions serve as a reference voltage to the comparators.

The dual comparator (common inverting terminal) features a single power supply which discontinues power in STOP mode. The common voltage range is 0-4V when the V_{CC} is 5.0V; the power supply and common mode rejection ratios are 90 dB and 60 dB, respectively.

Interrupts are generated on either edge of Comparator 2's output, or on the falling edge of Comparator 1's output. The comparator output is used for interrupt generation, Port 3 data inputs, or T_{IN} through P31. Alternatively, the comparators can be disabled, freeing the reference input (P33) for use as IRQ1 and/or P33 input.

FUNCTIONAL DESCRIPTION

The following special functions have been incorporated into the Z86L04/L08 devices to enhance the standard Z8 core architecture to provide the user with increased design flexibility.

RESET. This function is accomplished by means of a Power-On Reset or a Watch-Dog Timer Reset. Upon power-up, the Power-On Reset circuit waits for T_{POR} ms, plus 18 clock cycles, then starts program execution at address 000C (Hex) (Figure 10). The control registers' reset values are shown in Table 3.

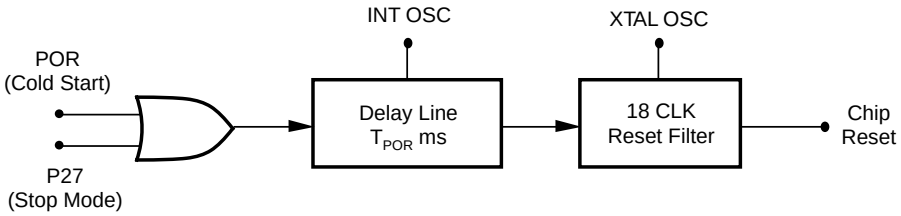


Figure 10. Internal Reset Configuration

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for a POR timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. The POR timer circuit is a one-shot timer triggered by one of the five following conditions:

- Power bad to power good status
- Stop-Mode Recovery
- WDT time-out
- WDT time-out (in HALT Mode)
- WDT time-out (in STOP Mode)

Watch-Dog Timer Reset. The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and is retriggered on subsequent execution of the WDT instruction. The timer circuit is driven by an on-board RC oscillator. If the permanent WDT option is selected then the WDT is enabled after reset and operates in RUN Mode, HALT mode, STOP mode and cannot be disabled. If the permanent WDT option is not selected then the WDT, when enabled by the user's software, does not operate in STOP Mode, but it can operate in HALT Mode by using a WDH instruction.

Table 3. Control Register Reset Values

		Reset Condition								
Addr	**Reg.**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comments**
FF	SPL	0	0	0	0	0	0	0	0	
FE	GPR	0	0	0	0	0	0	0	0	
FD	RP	0	0	0	0	0	0	0	0	
FC	FLAGS	U	U	U	U	U	U	U	U	
FB	IMR	0	U	U	U	U	U	U	U	
FA	IRQ	U	U	0	0	0	0	0	0	IRQ3 is used for positive edge detection
F9	IPR	U	U	U	U	U	U	U	U	
F8*	P01M	U	U	U	0	U	U	0	1	
F7*	P3M	U	U	U	U	U	U	0	0	P2 open-drain
F6*	P2M	1	1	1	1	1	1	1	1	Inputs after reset
F5	PRE0	U	U	U	U	U	U	U	0	
F4	T0	U	U	U	U	U	U	U	U	
F3	PRE1	U	U	U	U	U	U	0	0	
F2	T1	U	U	U	U	U	U	U	U	
F1	TMR	0	0	0	0	0	0	0	0	

Notes:
*Registers are not reset after a STOP-Mode Recovery using P27 pin. A subsequent reset will cause these control registers to be reconfigured as shown in Table 4 and the user must avoid bus contention on the port pins or it may affect device reliability.

Program Memory. The Z8 addresses up to 1024,2048 bytes of internal program memory (Figure 11). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Bytes 0-1023/0-2047 are on-chip mask programmable ROM.

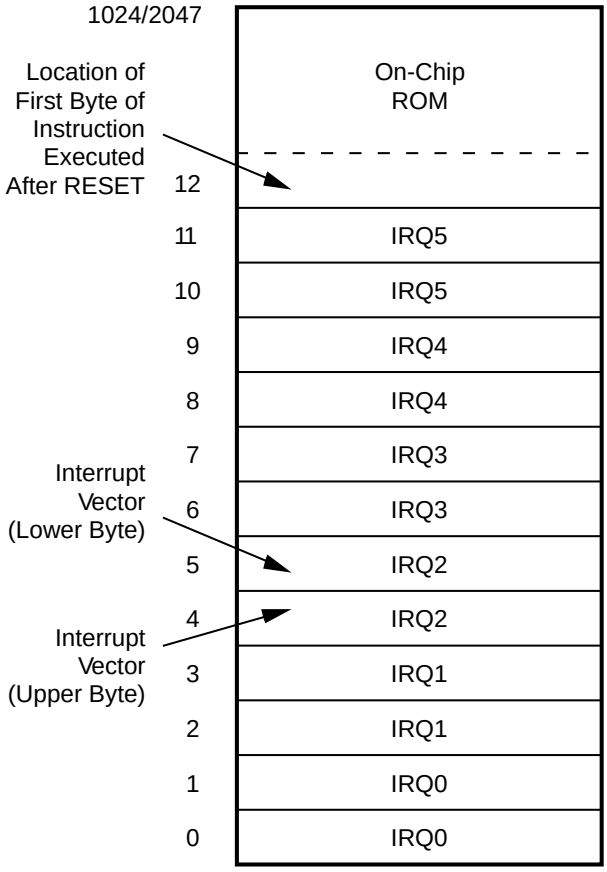


Figure 11. Program Memory Map

Register File. The Register File consists of three I/O port registers, 61 general-purpose registers, and 12 control and status registers R0-R3, R4-R127 and R241-R255, respectively (Figure 12). General-purpose registers occupy the 04H to 7FH address space. I/O ports are mapped as per the existing CMOS Z8. The instructions can access registers directly or indirectly through an 8-bit address field. This allows short 4-bit register addressing using the Register Pointer. In the 4-bit mode, the register file is divided into eight working register groups, each occupying 16 continuous locations. The Register Pointer (Figure 13) addresses the starting location of the active working-register group.

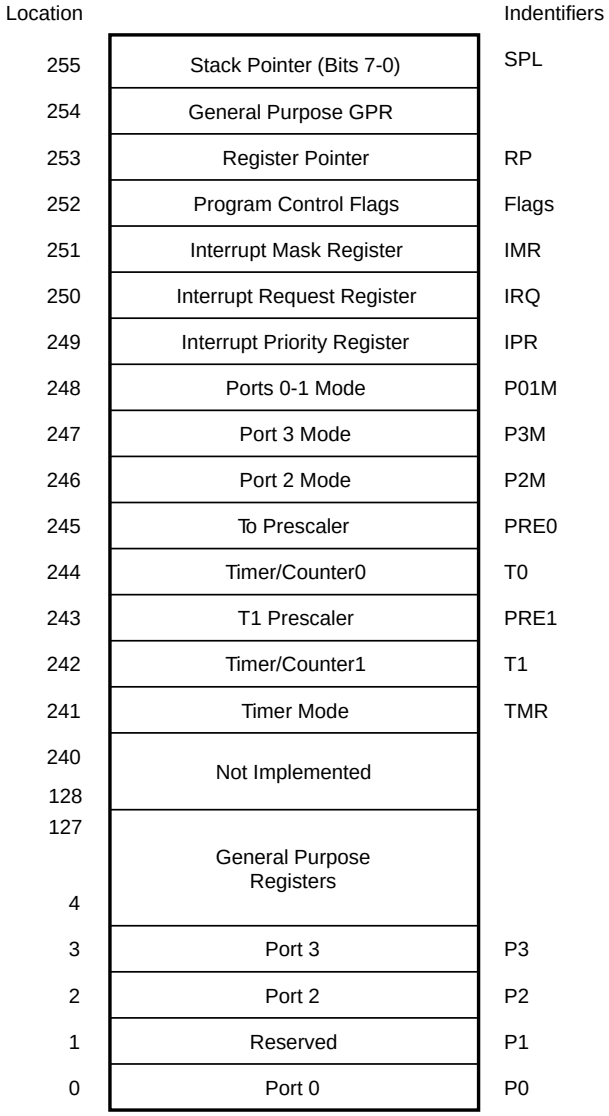


Figure 12. Register File

FUNCTIONAL DESCRIPTION (Continued)

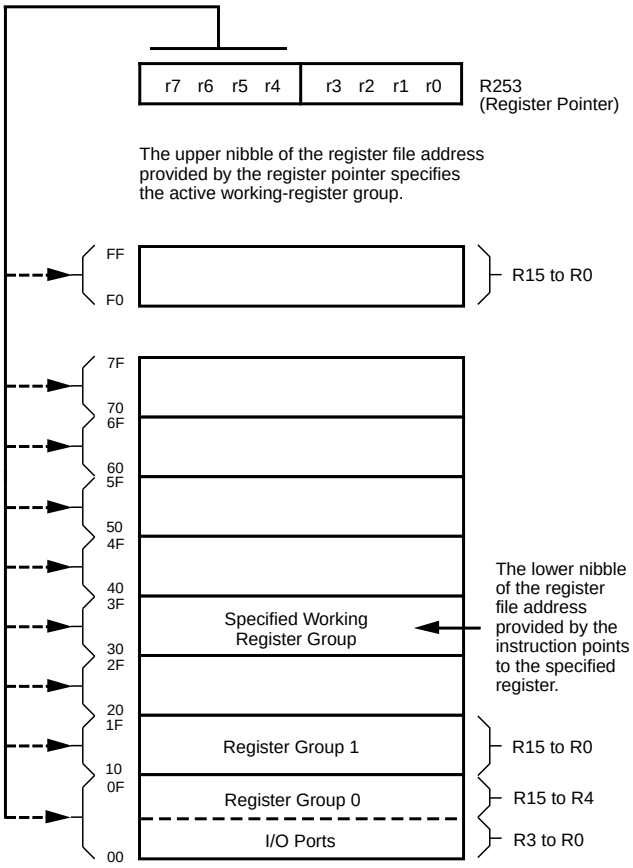


Figure 13. Register Pointer

Stack Pointer. The Z8 has an 8-bit Stack Pointer (R255) used for the internal stack that resides within the 60 general-purpose registers. It is set to 00Hex after any reset.

General-Purpose Registers (GPR). These registers are undefined after the device is powered up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general-purpose register. But is set to 00Hex after any reset.

Counter/Timer. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its 6-bit programmable prescaler. The T1 prescaler is driven by internal or external clock sources. (Figure 14).

The 6-bit prescaler divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both counter and prescaler reach the end of count, a timer interrupt request IRQ5 (T1 or IRQ4 (T0) is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters are also programmed to stop upon reaching zero (Single-Pass mode) or to automatically reload the initial value and continue counting (Modulo-N Continuous Mode).

The counters, but not the prescaler, are read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and is either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that is retriggerable or non-retriggerable, or used as a gate input for the internal clock.

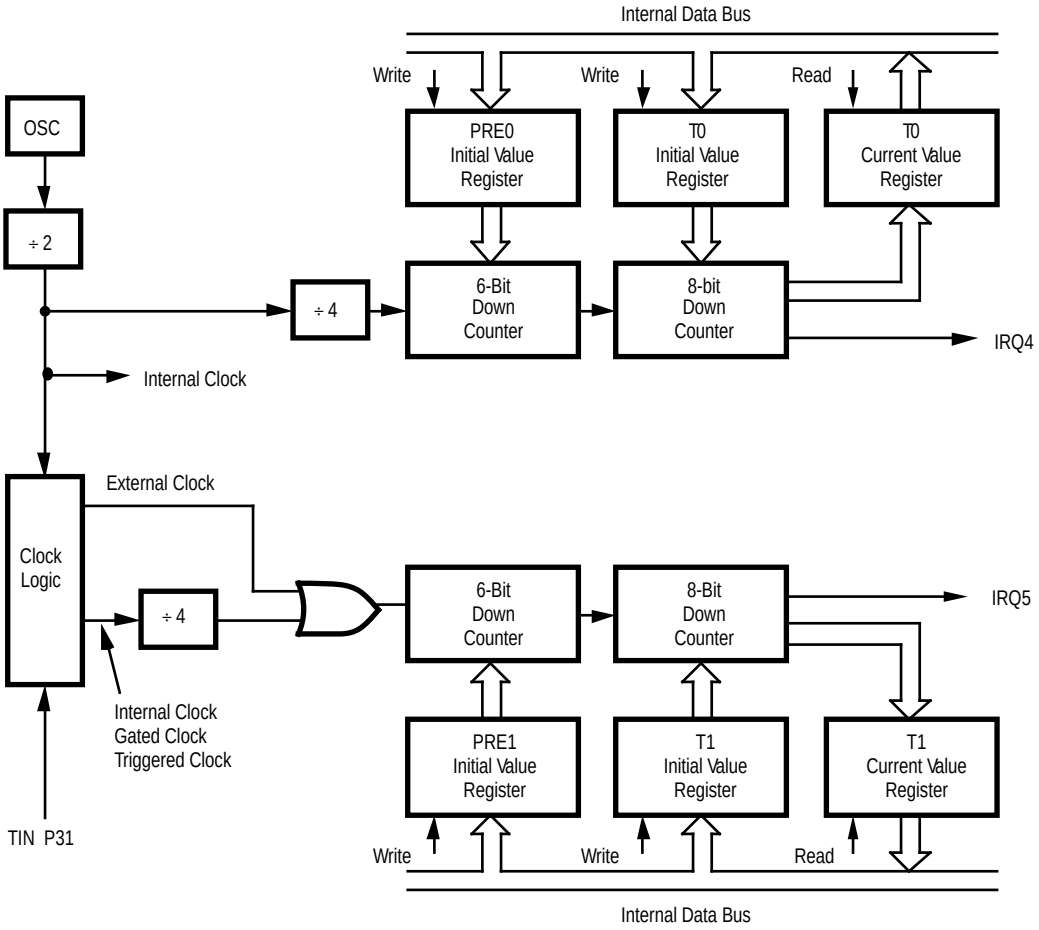


Figure 14. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z8 has five interrupts from four different sources. These interrupts are maskable and prioritized (Figure 15). The sources are divided as follows: the falling edge of P31 (AN1), P32 (AN2), P33 (REF), the rising edge of P32 (AN2), and one counter/timer. The Interrupt Mask Register globally or individually enables or disables the five interrupt requests (Table 4).

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z8 interrupts are vectored through locations in program memory. When an Interrupt machine cycle is activated, an Interrupt Request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests needs service.

User must select any Z86E08 mode in Zilog's C12 ICE-BOX™ emulator. The rising edge interrupt is not directly supported on the Z86CCP00ZEM emulator.

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	AN2(P32)	0,1	External (F)Edge
IRQ1	REF(P33)	2,3	External (F)Edge
IRQ2	AN1(P31)	4,5	External (F)Edge
IRQ3	AN2(P32)	6,7	External (R)Edge
IRQ4	T0	8,9	Internal
IRQ5	T1	10,11	Internal

Note:
F = Falling edge triggered
R = Rising edge triggered

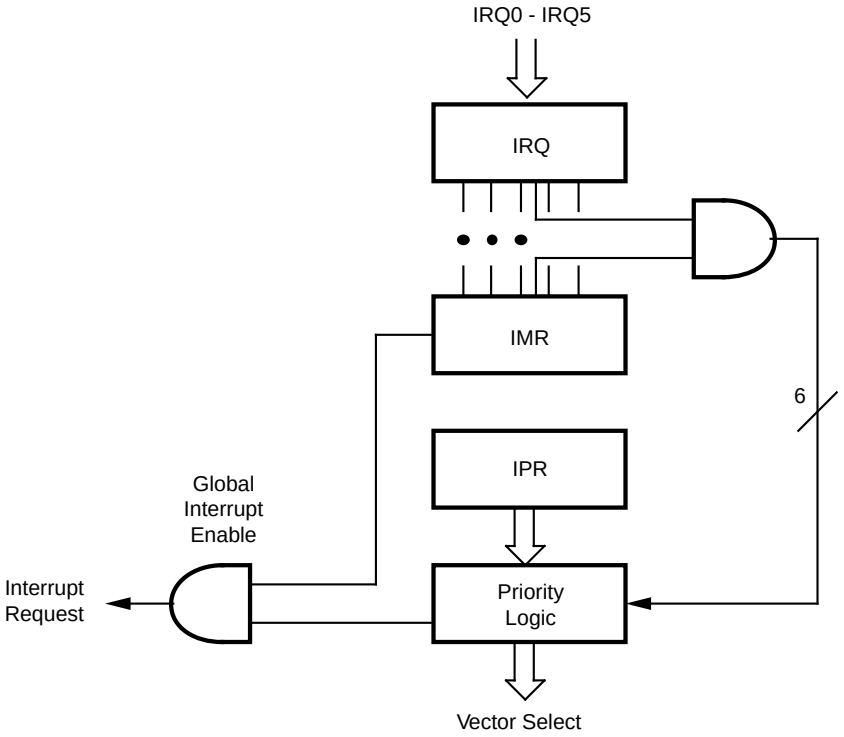
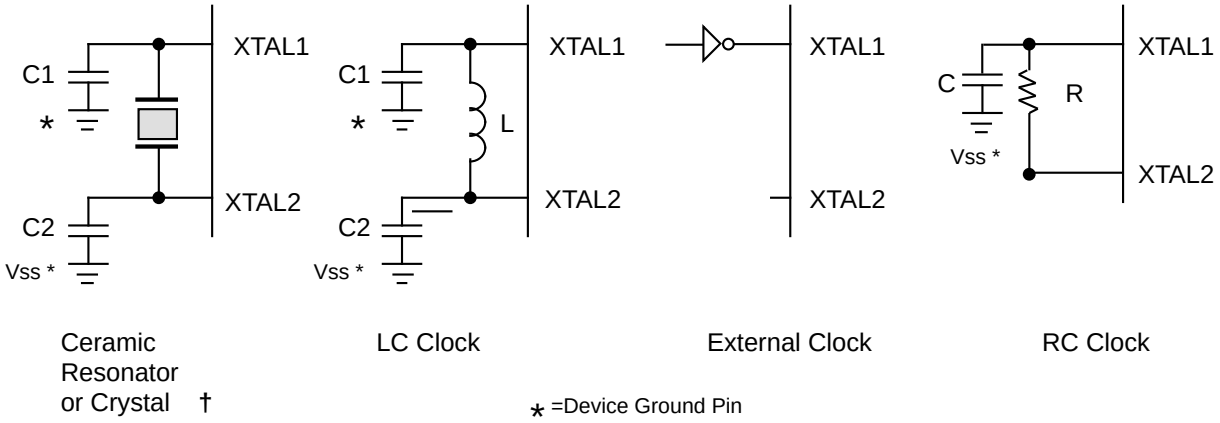


Figure 15. Interrupt Block Diagram

Clock. The Z8 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, ceramic resonator, or any suitable external clock source (XTAL1 = INPUT, XTAL2 = OUTPUT). The crystal should be AT cut, 8 MHz max, with a series resistance (RS) of less than or equal to 100 Ohms.

The crystal or ceramic resonator should be connected across XTAL1 and XTAL2 using the vendors crystal or ceramic resonator recommended capacitors from each pin directly to device ground pin 14 (Figure 16). Note that the crystal capacitor loads should be connected to V_{SS}, Pin 14 to reduce Ground noise injection.



† **Note:** If 32 KHz oscillator is selected then an external 10 Megohm resistor must be connected between XTAL1 and XTAL2 pins.

Figure 16. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

HALT Mode. This instruction turns off the internal CPU clock but not the crystal oscillation. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2 and IRQ3 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP Mode. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 μA. The STOP mode is released by a RESET through a Stop-Mode Recovery (pin P27). A Low condition on pin P27 releases the STOP mode even if P27 is an output. Program execution begins at location 000C(Hex). However, when P27 is used to release the STOP mode, the I/O port mode registers are not reconfigured to their default power-on conditions. This prevents any I/O, configured as output when the STOP instruction was executed, from glitching to an unknown state. To use the P27 release approach with STOP mode, use the following instruction:

```
LD      P2M, #1XXX XXXXB
NOP
STOP
```

Notes:
X = Dependent on user's application.
Stop-Mode Recovery pin P27 is not edge triggered.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user executes a NOP (opcode=FFH) immediately before the appropriate SLEEP instruction, such as:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

Watch-Dog Timer (WDT). The Watch-Dog Timer is enabled by instruction WDT. When the WDT is enabled, it cannot be stopped by the instruction. With the WDT instruction, the WDT is refreshed when it is enabled within every 1 Twdt period; otherwise, the controller resets itself, The WDT instruction affects the flags accordingly; Z=1, S=0, V=0. WDT = 5F (Hex)

Opcode WDT (5FH). The first time opcode 5FH is executed, the WDT is enabled and subsequent execution clears the WDT counter. This must be done at least every T_{WDT}; otherwise, the WDT times out and generates a reset. The generated reset is the same as a power-on reset of T_{POR}, plus 18 XTAL clock cycles. The internal RC driven WDT does not run in stop mode, unless the permanent WDT enable option is selected. The WDT does not run in halt mode unless WDH instruction is executed or permanent WDT enable option is selected.

Opcode WDH (4FH). When this instruction is executed it enables the WDT during HALT. If not, the WDT stops when entering HALT. This instruction does not clear the counters, it just makes it possible to have the WDT running during HALT mode. A WDH instruction executed without executing WDT (5FH) has no effect.

Note: Opcode WDH and permanently enabled WDT is not directly supported by the Z86CCP00ZEM.

WDT Clock Source. The WDT clock source option selects the clock source for the WDT. It can be the internal on-board RC oscillator or the internal system clock (SCLK). If the SCLK is selected, then the WDT time out (T_{WDT}) is 130,416 x SCLK and the T_{POR} is 16,362 x SCLK. Also, if the permanent WDT option is selected in this case; the WDT will not run in STOP mode. (Z86L04 only)

Auto Reset Voltage (V_{LV}). The Z8 has an auto-reset built-in. The auto-reset circuit resets the Z8 when it detects the V_{CC} below V_{LV}. Figure 17 shows the Auto Reset Voltage versus temperature.

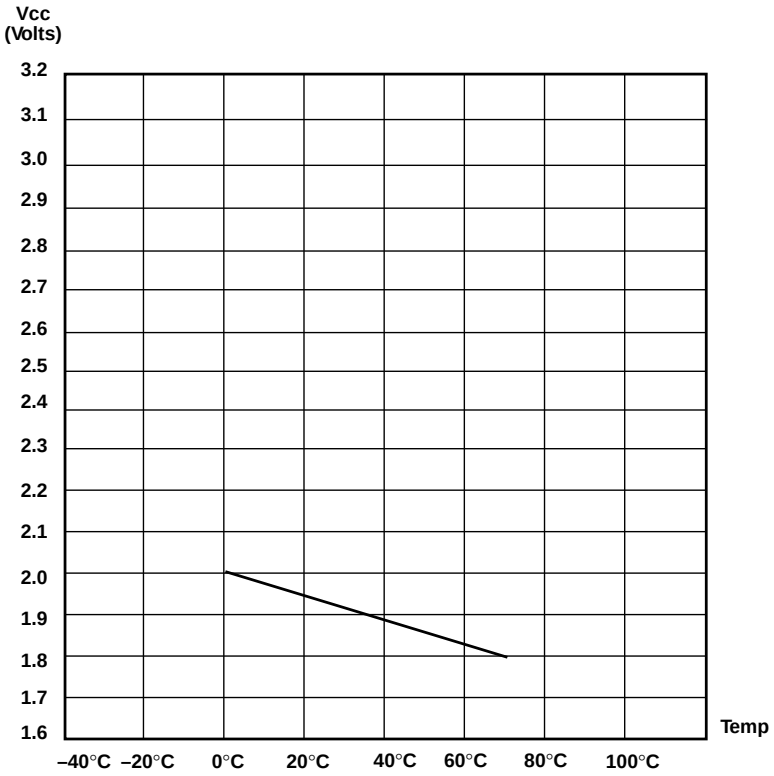


Figure 17. Typical Auto Reset Voltage (V_{LV}) vs. Temperature

OPTIONS

ROM protect, Low Noise, Auto Latch Disable, RC Oscillator, 32 kHz Crystal and Permanent WDT enable features as options and must be selected at the time of ROM code submissions.

ROM Protect. ROM Protect fully protects the Z8 ROM code from being read externally. When ROM Protect is selected, the instructions LDC and LDCI are supported. (However, instructions LDE and LDEI are not supported.)

Auto Latch Disable. Auto Latch Disable option when Selected will globally disable all Auto Latches.

RC. RC Oscillator option when selected will allow using a resistor (R) and a capacitor (C) as a clock source.

WDT Clock Source. This selects the clock source of the WDT and POR counter chain to be driven by either the internal system clock or the internal on-board RC oscillator. (Z86L04 only).

Low EMI. The Low EMI (Low noise) mode by passes the divide by two clock circuit (SCLK = XTAL/1) and lowers the output sink and drive currents by 75 percent. The maximum oscillator frequency at XTAL pins is 1MHz.

WDT Enable. WDT Enable option bit when selected will have the WDT permanently enabled in all modes and can not be stopped in HALT or STOP Mode, if the internal RC oscillator is selected as the clock source. If the system clock (SCLK) is the clock source, the WDT will be stopped in STOP mode.

Please note that when using the device in a noisy environment, it is suggested that the voltages on the EPM and CE pins be clamped to V_{CC} through a diode to V_{CC} to prevent accidentally entering the OTP mode. The V_{PP} requires both a diode and a 100 pF capacitor.

32 kHz Crystal. This disables the internal feedback resistor on the crystal oscillator circuit (not for RC oscillator circuit) so that a 32 kHz crystal can be connected to the XTAL1 and XTAL2 pins.

Z8 CONTROL REGISTERS

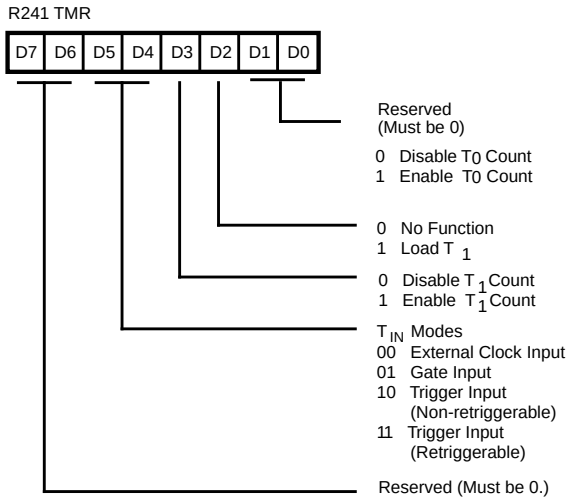


Figure 18. Timer Mode Register ($F1_H$: Read/Write)

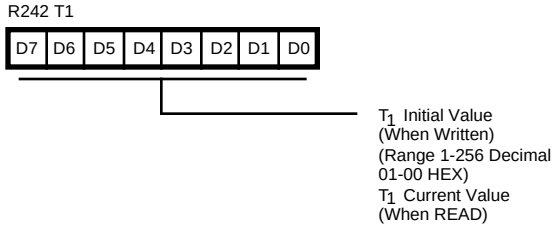


Figure 19. Counter Timer 1 Register ($f2_H$:Read/Write)

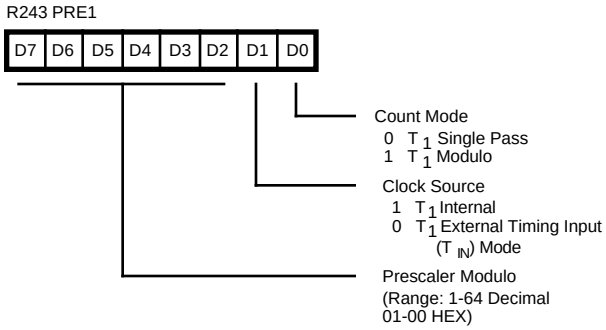


Figure 20. Prescaler1 Register ($F3_H$: Write Only)

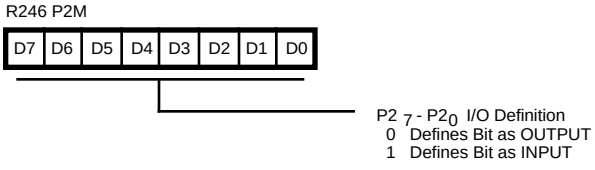


Figure 21. Port 2 Mode Register ($F6_H$: Write Only)

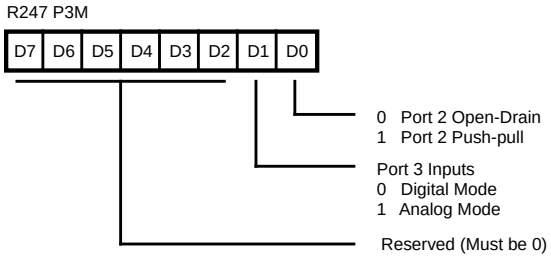


Figure 22. Port 3 Mode Register ($F7_H$: Write Only)

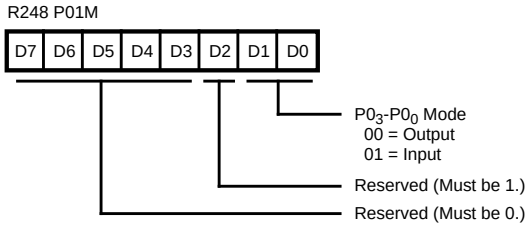


Figure 23. Port 0 and 1 Mode Register ($F8_H$: Write Only)

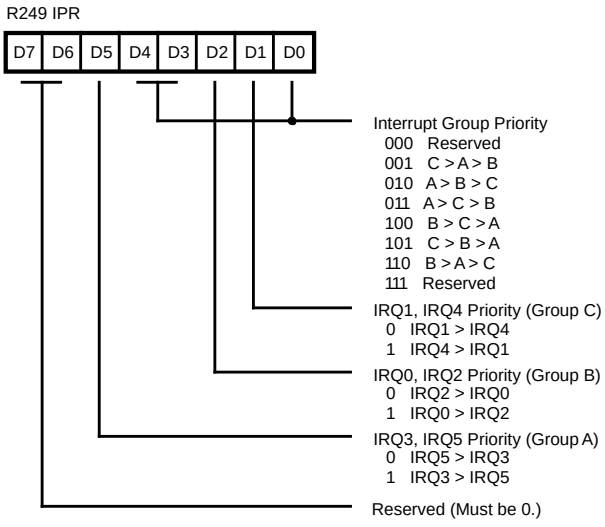


Figure 24. Interrupt Priority Register ($F9_H$: Write Only)

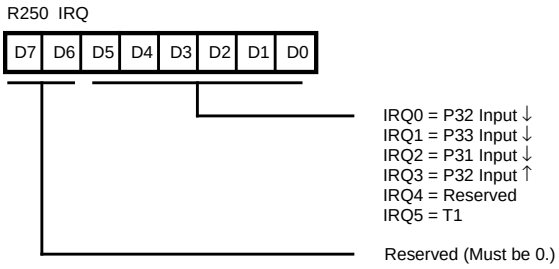


Figure 25. Interrupt Request Register (FA_H: Read/Write)

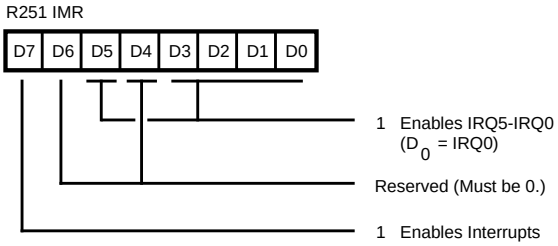


Figure 26. Interrupt Mask Register (FB_H: Read/Write)

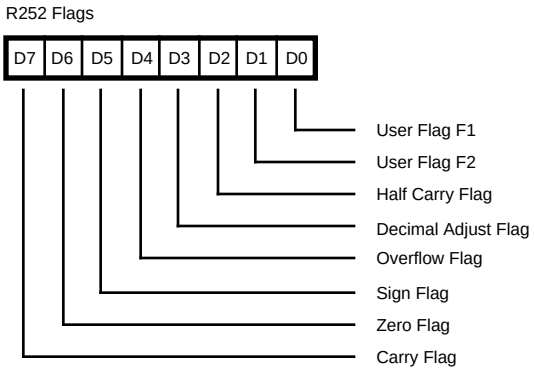


Figure 27. Flag Register (FC_H: Read/Write)

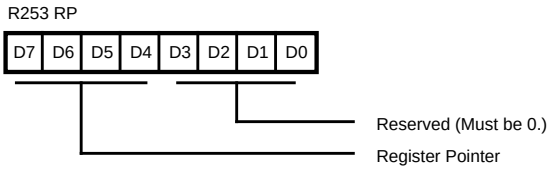


Figure 28. Register Pointer FD_H: Read/Write)

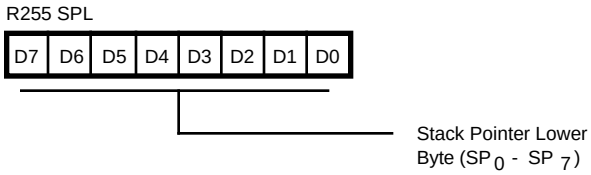
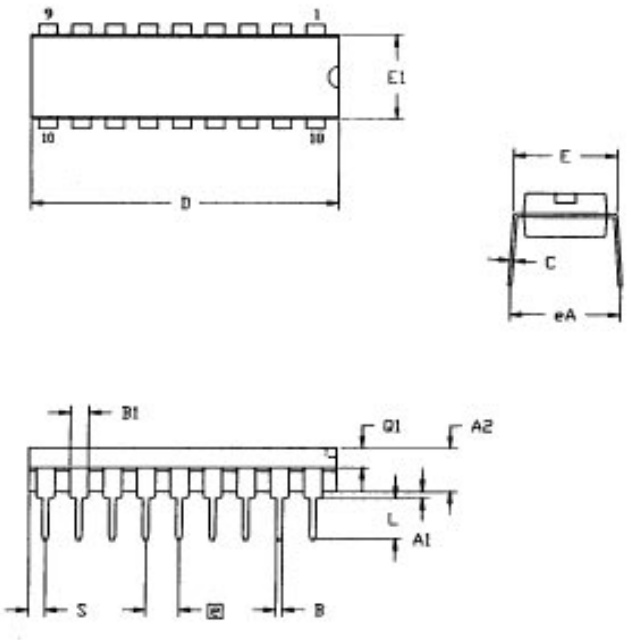


Figure 29. Stack Pointer (FF_H: Read/Write)

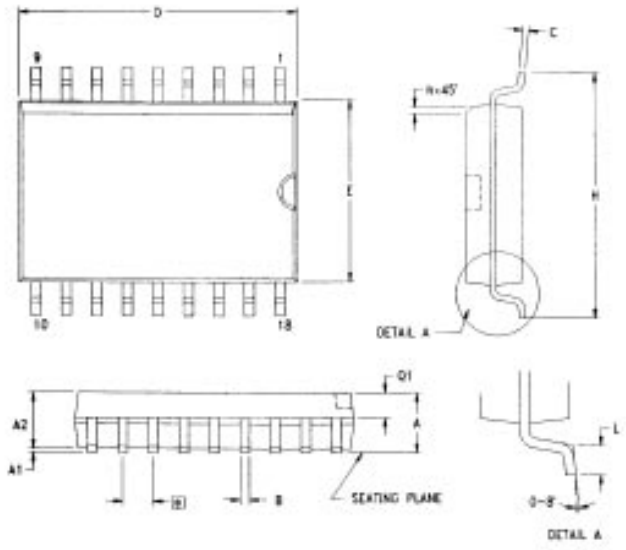
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
[e]	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 30. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
[e]	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 31. 18-Pin SOIC Package Diagram

ORDERING INFORMATION

Standard Temperature

18-Pin DIP	18-Pin SOIC
Z86L0408PSC	Z86L0408SSC
Z86L0808PSC	Z86L0808SSC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package

P = Plastic DIP

Longer Lead Time

S = SOIC

Preferred Temperature

S = 0 °C to +70 °C

Speed

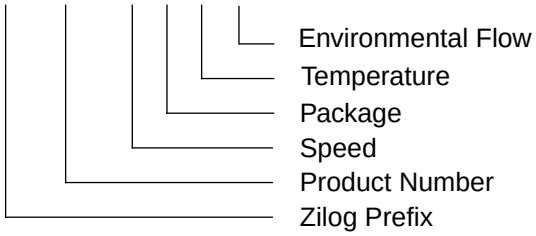
08 = 8 MHz

Environmental

C = Plastic Standard

Example:

Z 86L08 08 P S C is a Z86L08, 08 MHz, Plastic DIP, 0 °C to +70 °C, Plastic Standard Flow



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