Z86E30/E31

CMOS 8-BIT Z8® OTP CCP™ CONSUMER CONTROLLER PROCESSORS

FEATURES

- The Z86E30 and Z86E31 Have the Following General Characteristics:

Part	EPROM	RAM	Speeds
Z86E30	4K	236	12 MHz
Z86E31	2K	124	8 MHz

- 28-Pin Packages (DIP, Cerdip Window Lid)
- 4.5V to 5.5V Operating Range
- Clock Speeds up to 8 MHz (E31) and 12 MHz (E30)
- Software Programmable Low EMI Mode
- Pull-Up Active/Open-Drain Programmable on Ports 0 and 2
- EPROM Protect Option
- RAM Protect Programmable
- RC Oscillator Programmable
- Low Power Consumption: 60 mW
- Two Standby Modes: STOP and HALT
- 24 Input/Output Lines (Three with Comparator Inputs)
- 17 Digital Inputs with CMOS Levels, Schmitt-Triggered
- Three Digital Inputs with CMOS Levels Only
- Three Expanded Register File Control Registers
- Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler
- Six Vectored, Priority Interrupts from Six Different Sources
- Software Enabled Watch-Dog Timer
- Auto Power-On Reset
- Auto Latches
- Two Comparators with Programmable Interrupt Polarity
- On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive

GENERAL DESCRIPTION

The Z86E30/E31 CCP™ (Consumer Controller Processors) are members of Zilog's the Z8® single-chip microcontroller family with enhanced wake-up circuitry, programmable watch-dog timers and low noise/EMI options. These enhancements result in a more efficient, cost-effective design and provide the user with increased design flexibility over the standard Z8 microcontroller core. With 4K/2K bytes of EPROM and 236/124 bytes of general-purpose RAM, respectively, these low cost, low power consumption CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion.

Manufactured in CMOS technology and offered in 28-pin DIP and Cerdip Window Lid package styles, these devices allow easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version.

For applications demanding powerful I/O capabilities, the Z86E30/E31 provides 24 pins dedicated to input and output. These lines are grouped into three ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake.

GENERAL DESCRIPTION (Continued)

Three basic address spaces are available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File (ERF). The Register File is composed of 236/124 bytes of general-purpose registers, three I/O port registers and 15 control and status registers. The Expanded Register File consists of three control resisters.

To unburden the system from coping with the real-time tasks such as counting/timing and input/output data communication, the Z86E30/31 offers two on-chip counter/timers with a large number of user-selectable modes, and two on-board comparators to process analog signals with a common reference voltage (Figures 1 and 2).

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B/W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

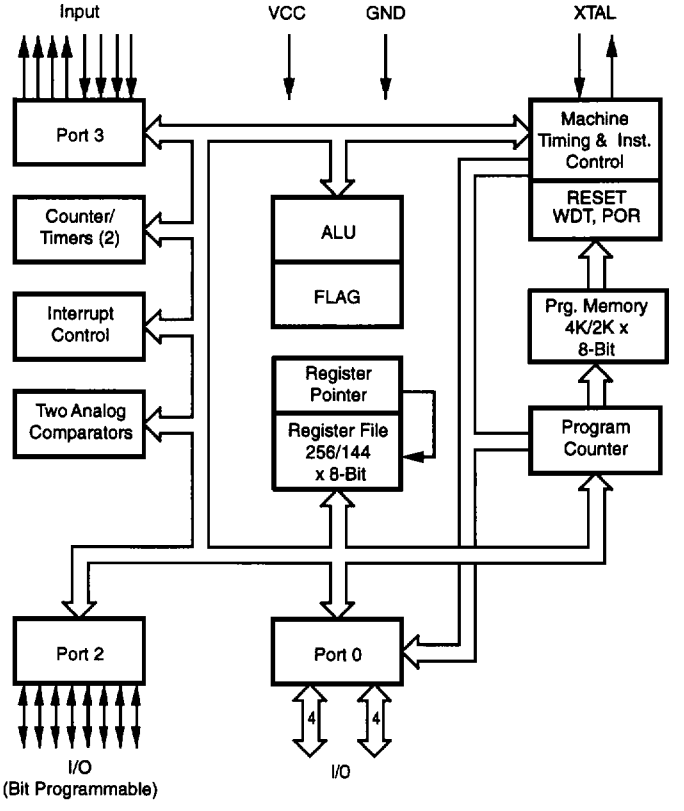

Figure 1. Z86E30/E31 Functional Block Diagram

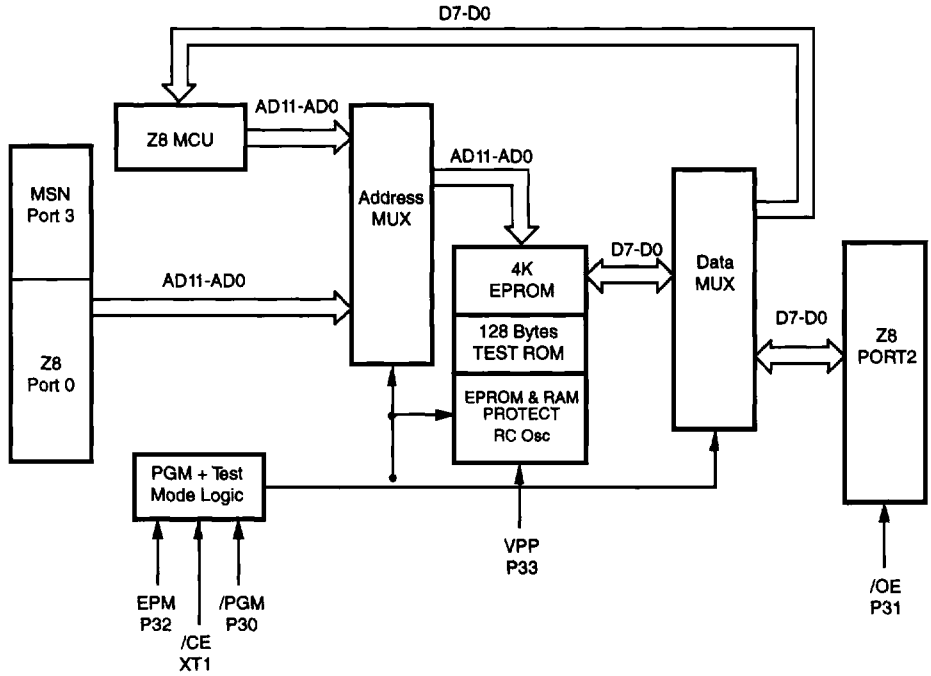

Figure 2. Z86E30/E31 EPROM Programming Block Diagram

PIN DESCRIPTION

Table 1. Z86E30/E31 28-Pin DIP Pin Identification*

Standard Mode Pin #	Symbol	Function	Direction
1-3	P25-P27	Port 2, Pins 5,6,	In/Output
4-7	P04-P07	Port 0, Pins 4,5,6,7	In/Output
8	V_{CC}	Power Supply	
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-P33	Port 3, Pins 1,2,3	Input
14-15	P34-P35	Port 3, Pins 4,5	Output
16	P37	Port 3, Pin 7	Output
17	P36	Port 3, Pin 6	Output
18	P30	Port 3, Pin 0	Input
19-21	P00-P02	Port 0, Pins 0,1,2	In/Output
22	V_{SS}	Ground	
23	P03	Port 0, Pin 3	In/Output
24-28	P20-P24	Port 2, Pins 0,1,2,3,4	In/Output

Note:
* Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

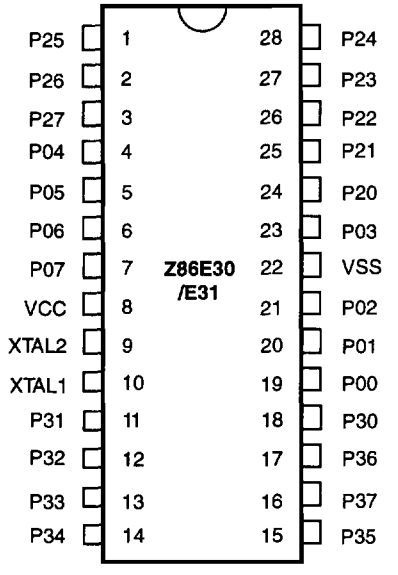

Figure 3. Z86E30/31 Standard Mode 28-Pin DIP Pin Configuration*

Table 2. Z86E30/E31 28-Pin DIP Pin Identification*

EPROM Programming Mode Pin #	Symbol	Function	Direction
1-3	D5-D7	Data 5,6,7	In/Output
4-7	A4-A7	Address 4,5,6,7	Input
8	V_{CC}	Power Supply	
9	NC	No connection	
10	/CE	Chip Select	Input
11	/OE	Output Enable	Input
12	EPM	EPROM Prog. Mode	Input
13	V_{PP}	Prog. Voltage	Input
14-15	A8-A9	Address 8,9	Input
16	A11	Address 11	Input
17	A10	Address 10	Input
18	/PGM	Prog. Mode	Input
19-21	A0-A2	Address 0,1,2	Input
22	V_{SS}	Ground	
23	A3	Address 3	Input
24-28	D0-D4	Data 0,1,2,3,4	In/Output

Note:
* Pin Identification and Configuration identical on DIP and Cerdip Window Lid style packages.

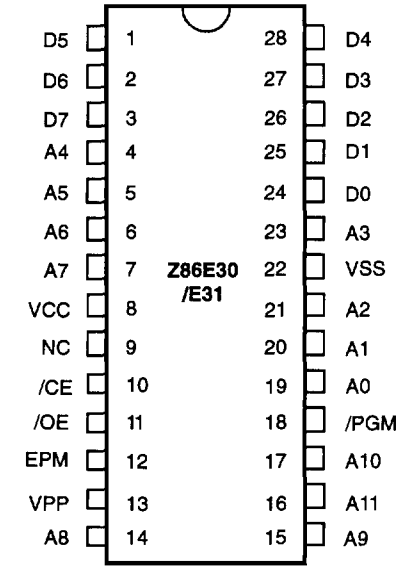

Figure 4. Z86E30/31 EPROM Programming Mode 28-Pin DIP Pin Configuration*

PIN FUNCTIONS

Z86E30/31 Standard Mode

XTAL1 *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC, RC network or external single-phase clock to the on-chip oscillator input.

XTAL2 *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 0 (P07-P00). Port 0 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be nibble programmed as P03-P00 input/output and P07-P04 input/output, separately. The input buffers are Schmitt-triggered and nibbles programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. Port 0 can also be used as a handshake I/O port.

In Handshake Mode, Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to Port 0's upper nibble. The lower nibble must have the same direction as the upper nibble (Figure 5).

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EPROM Programming Mode

D7-D0 *Data Bus.* The data can be read from or written to the EPROM through the data bus.

A11-A0 *Address Bus.* During programming, the EPROM address is written to the address bus.

V_{CC} *Power Supply.* This pin must be supply 5V during the EPROM Read Mode and 6V during other modes.

/CE *Chip Enable* (active Low). This pin is active during EPROM Read Mode, Program Mode and Program Verify Mode.

/OE *Output Enable* (active Low). This pin drives the direction of the Data Bus. When this pin is Low, the Data Bus is output, when High, the Data Bus is input.

EPM *EPROM Program Mode.* This pin controls the different EPROM Program Mode by applying different voltages.

V_{PP} *Program Voltage.* This pin supplies the program voltage.

/PGM *Program Mode* (active Low). When this pin is Low, the data is programmed to the EPROM through the Data Bus.

Application Precaution

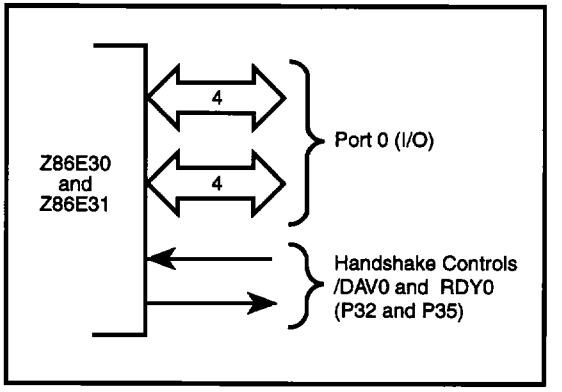
The production test-mode environment may be enabled accidentally during normal operation if ***excessive noise surges above V_{cc}*** occur on the XTAL1 pin.

In addition, processor operation of Z8 OTP devices may be affected by excessive noise surges on the V_{pp}, /CE, /EPM, /OE pins while the microcontroller is in Standard Mode.

Recommendations for dampening voltage surges in both test and OTP mode include the following:

- Using a clamping diode to V_{cc}
- Adding a capacitor to the affected pin.

PIN FUNCTIONS (Continued)



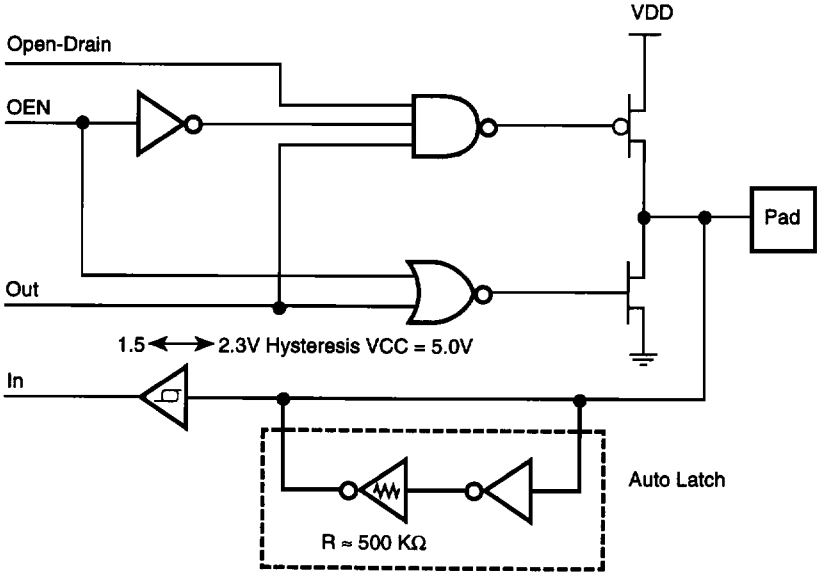
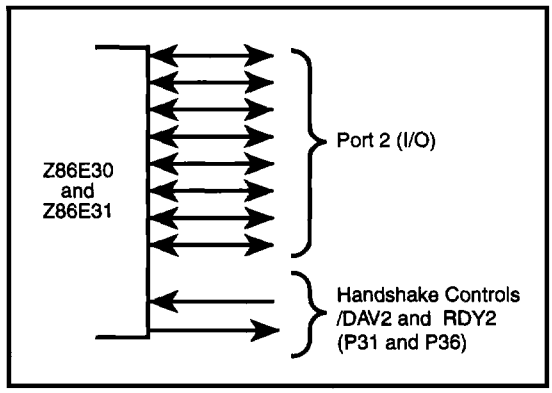


Figure 5. Port 0 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit, bi-directional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. All input buffers are Schmitt-triggered. Bits programmed as outputs can be globally programmed as either push-pull or open-drain. Low EMI output buffers can be globally programmed by the software. When used as an I/O port, Port 2 can be placed under handshake control. In Handshake Mode, Port 3 lines P31 and P36 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to bit 7 of Port 2 (Figure 6).



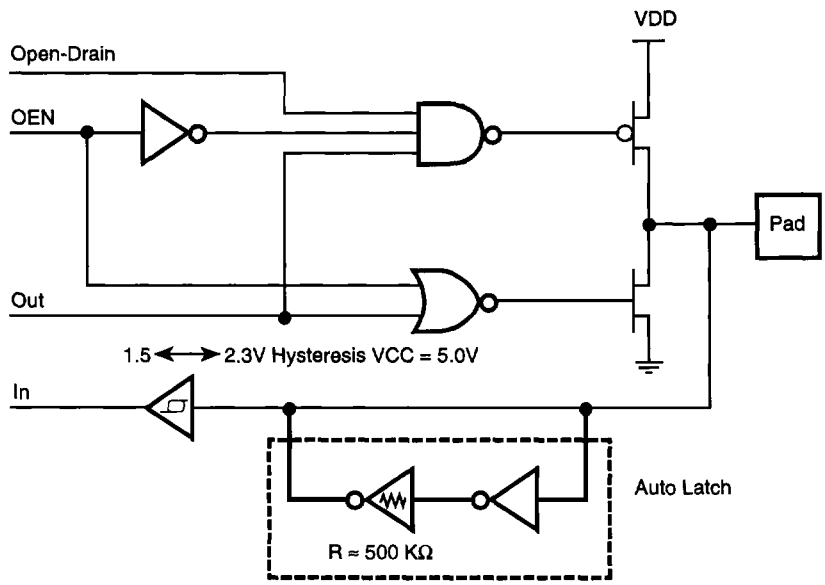


Figure 6. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS compatible port with four fixed inputs (P33-P30) and four fixed outputs (P37-P34), and can be configured under software for interrupt and handshake control functions. Port 3, pin 0 is Schmitt-triggered. Pins P31, P32, and P33 are standard CMOS inputs (no Auto Latches) and pins P34, P35, P36, and P37 are push-pull output lines. Low EMI output buffers can be globally programmed by software. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The comparator output can be outputted from P34 and P37, respectively, by setting PCON register (PCON) bit D0 to 1.

The analog function is enabled by setting the D1 of Port 3 Mode Register (P3M). For the interrupt function, P30 and P33 are falling edge triggered interrupt inputs. P31 and P32 can be programmed as falling, rising or both edge triggered interrupt inputs (Figure 7). Access to Counter/Timer 1 is made through P31 (T_{IN}) and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are also available on Port 3 (Table 3). T_{IN} Modes are enabled by setting R243 PRE1 Bit D1 to 0.

Table 3. Port 3 Pin Assignments

Pin	I/O	CTC1	AN IN	Int.	P0 HS	P2 HS
P30	IN			IRQ3		
P31	IN	T_{IN}	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT					
P35	OUT				R/D	
P36	OUT	T_{OUT}				R/D
P37	OUT					

Note: P33-P30 inputs differ from the Z86C30/31 in that there is no clamping diode to V_{CC} due to the EPROM high-voltage detection circuits. Exceeding the V_{IH} maximum specification during standard operating mode may cause the device to enter EPROM mode.

Comparator Inputs. Port 3, pins P31 and P32 each have a comparator front end. The comparator reference voltage (pin P33) is common to both comparators. In analog mode, P31 and P32 are the positive inputs, and P33 is the reference voltage of the comparators.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs (except P33-P31) that are not externally driven. Whether this is 0 or 1, cannot be determined.

A valid CMOS level, rather than a floating node, reduces excessive supply current flow in the input buffer.

Low EMI Emission. The Z86E30/31 can be programmed to operate in a low EMI emission mode in the PCON register. The oscillator and all I/O ports can be programmed as low EMI emission mode independently. Use of this feature results in:

- The pre-drivers slew rate reduced to 10 ns typical.
- Low EMI output drivers have resistance of 200 ohms (typical).
- Low EMI Oscillator.
- Internal SCLK/TCLK = XTAL operation limited to a maximum of 4 MHz - 250 ns cycle time, when Low EMI Oscillator is selected and system clock (SCLK = XTAL, SMR Reg. Bit D1 =1).

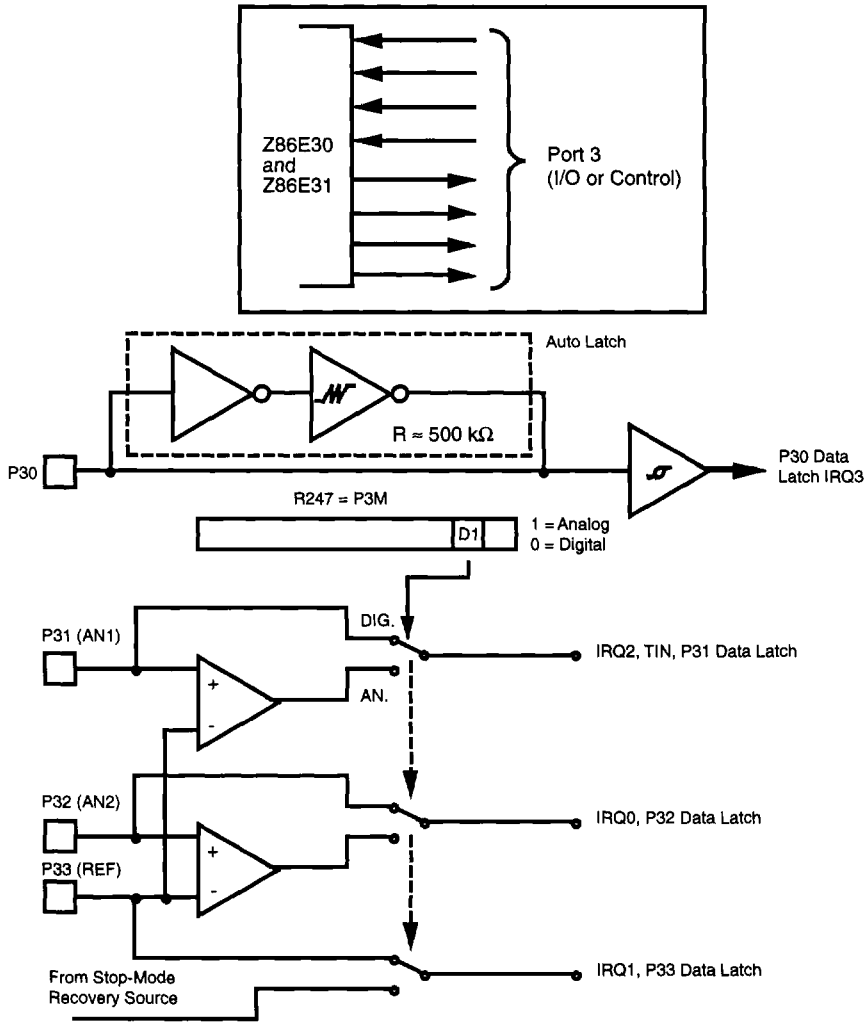


Figure 7. Port 3 Configuration

FUNCTIONAL DESCRIPTION

The Z86E30/E31 CCP™'s incorporate the following special functions to enhance the standard Z8® architecture to provide the user with increased design flexibility.

RESET. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP-Mode Recovery Source

Having the Auto Power-on Reset circuitry built in, the Z86E30/E31 does not need to be connected to an external power-on reset circuit. The reset time is 5 ms (typical) plus 18 clock cycles. The Z86E30/31 does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP-Mode Recovery operation.

Program Memory. The Z86E30/E31 can address up to 4K/2K bytes of internal program memory (Figure 8). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. Address 12 (000CH) to address 4095 (0FFFH)/2047(07FFH) are reserved for the user program. After reset, the program counter points at the address 000CH which is the starting address of the user program.

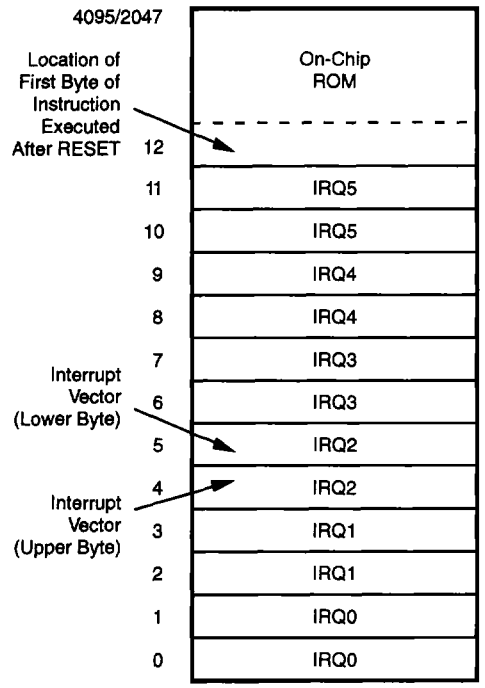


Figure 8. Program Memory Map

EPROM Protect. The 4K/2K bytes program memory is a One-Time-PROM. An EPROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC and LDCI instructions (LDE and LDEI instructions are not available in Z86E30/E31) to program memory in all modes. In EPROM protect mode, the instructions of LDC and LDCI are disabled globally. ROM look-up tables cannot be used with this option.

Expanded Register File (ERF). The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices, and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 11). These register groups are known as the Expanded Register File (ERF).

The low nibble (D3-D0) of the Register Pointer (RP) selects the active ERF group, and the high nibble (D7-D4) of register RP selects the working register group (Figure 9).

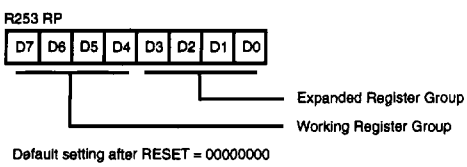


Figure 9. Register Pointer Register

Three system configuration registers reside in the Expanded Register File at bank FH: PCON, SMR, and WDTMR. The rest of the Expanded Register is not physically implemented and is reserved for future expansion.

Register File. The register file consists of three I/O port registers, 236/124 general-purpose registers, 15 control and status registers, and three system configuration registers in the expanded register group. The instructions can access registers directly or indirectly through an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 10). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working register and indirect addressing modes. (This bank is available in Z86C30 only.)

General Purpose Register (GPR). The general purpose registers are undefined after the device is powered-up. The registers keep their last value after any reset, as long as the reset occurs in the V_{CC} voltage-specified operating range. **Note:** Register R254 has been designated as a general purpose register.

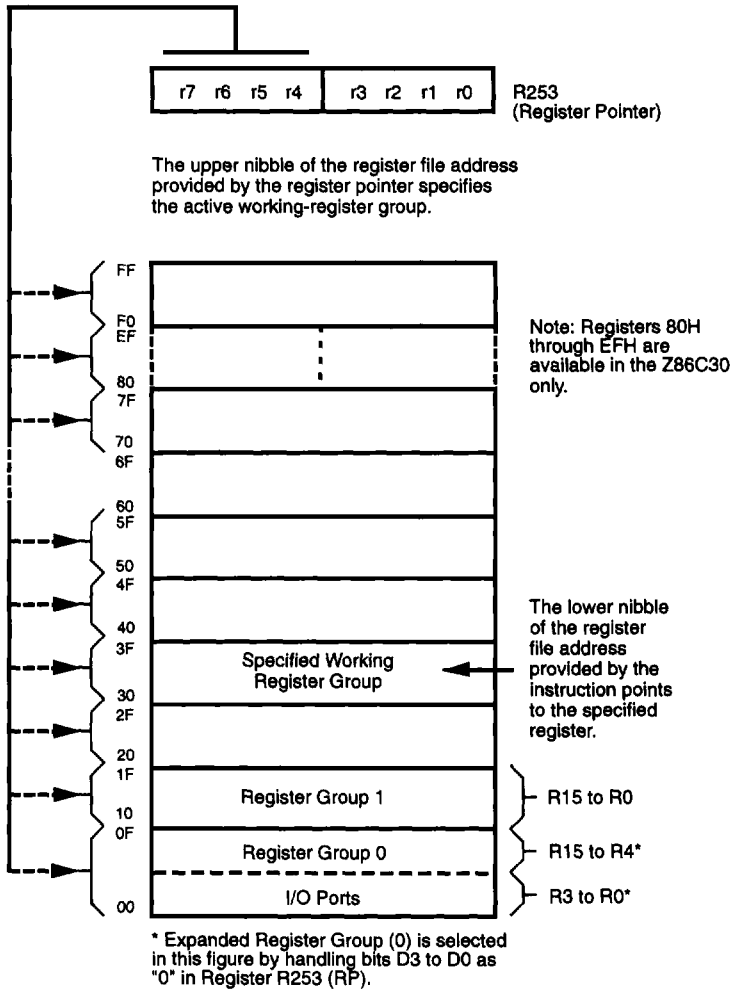


Figure 10. Register Pointer

FUNCTIONAL DESCRIPTION (Continued)

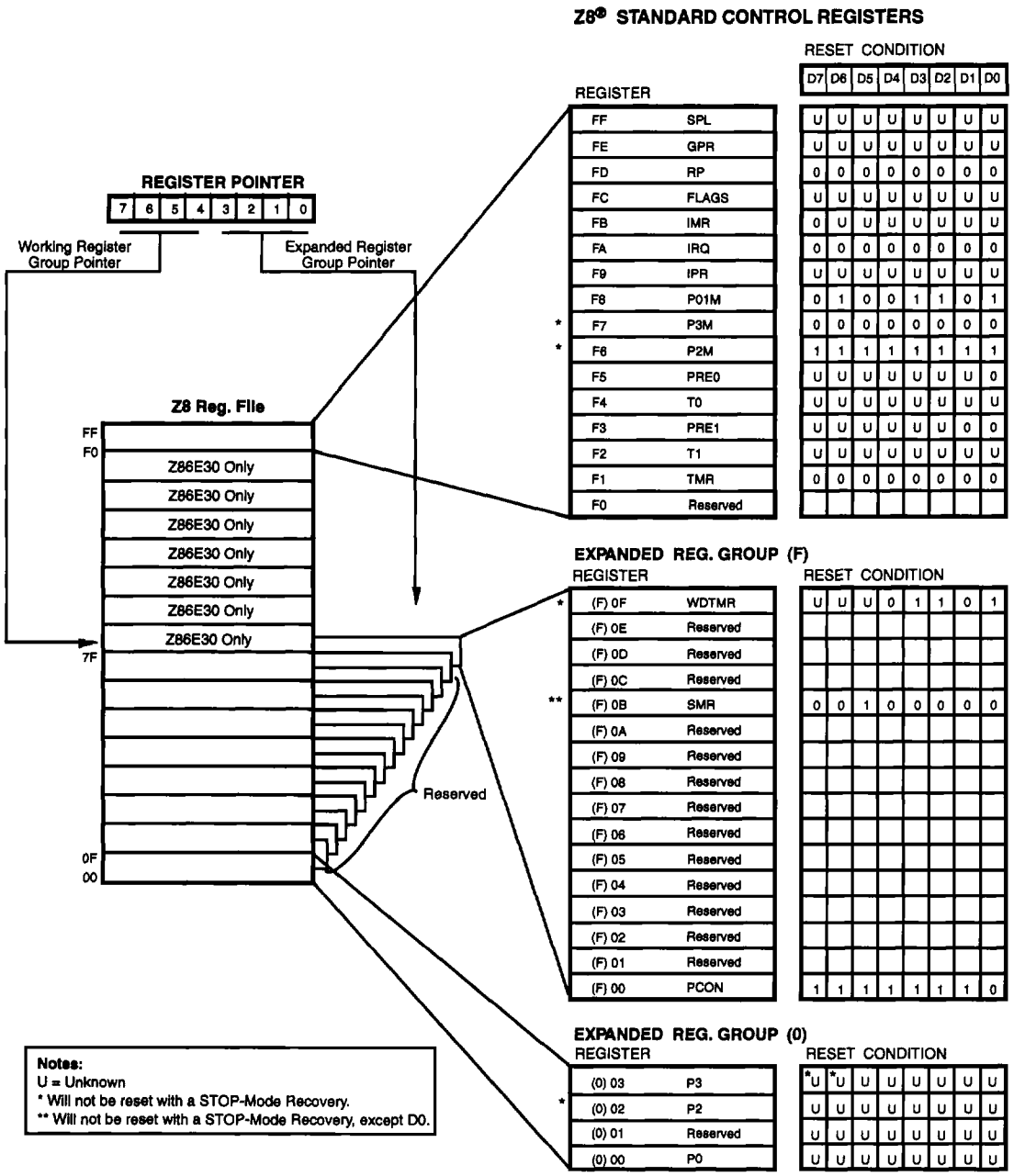


Figure 11. Expanded Register File Architecture

RAM Protect (Z86E30 Only). The upper portion of the RAM's address spaces %7F to %EF (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is EPROM-programmable. After the EPROM option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or 1, respectively. A 1 in D6 indicates RAM Protect enabled. This option is only available in the Z86E30.

Stack. The Z86E30/E31 has 236/124 general-purpose registers. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the general-purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0 and T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 12).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided by four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P30) as an external clock, a trigger input that can be retriggerable or not-retriggerable, or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (T_{OUT}) through which T0, T1 or the internal clock is output. The counter/timers are cascaded by connecting the T0 output to the input of T1.

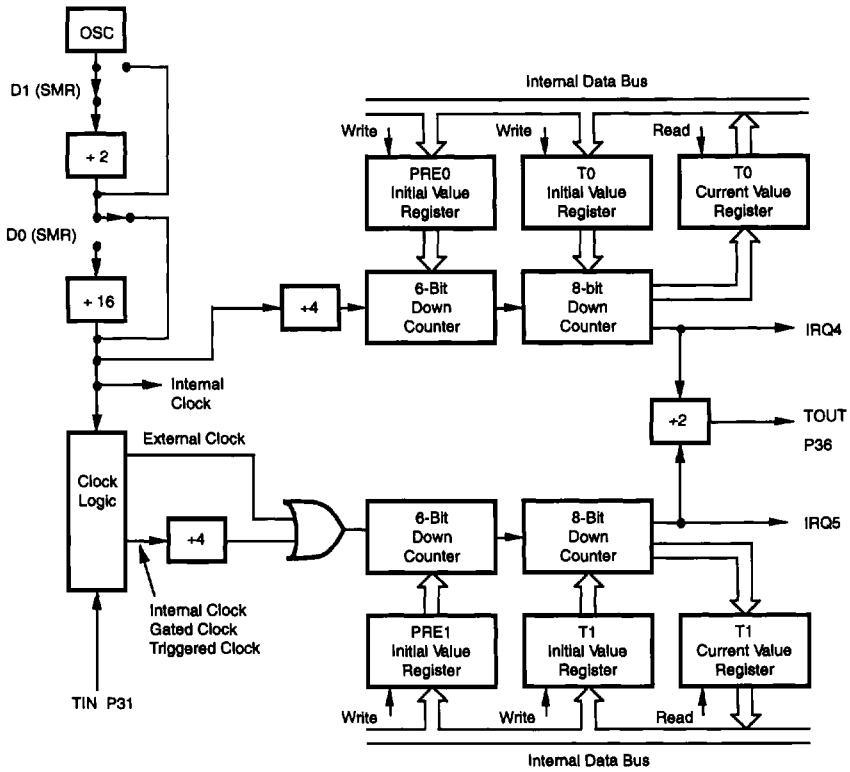


Figure 12. Counter/Timer Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Interrupts. The Z86E30/E31 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 13). The six sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 4).

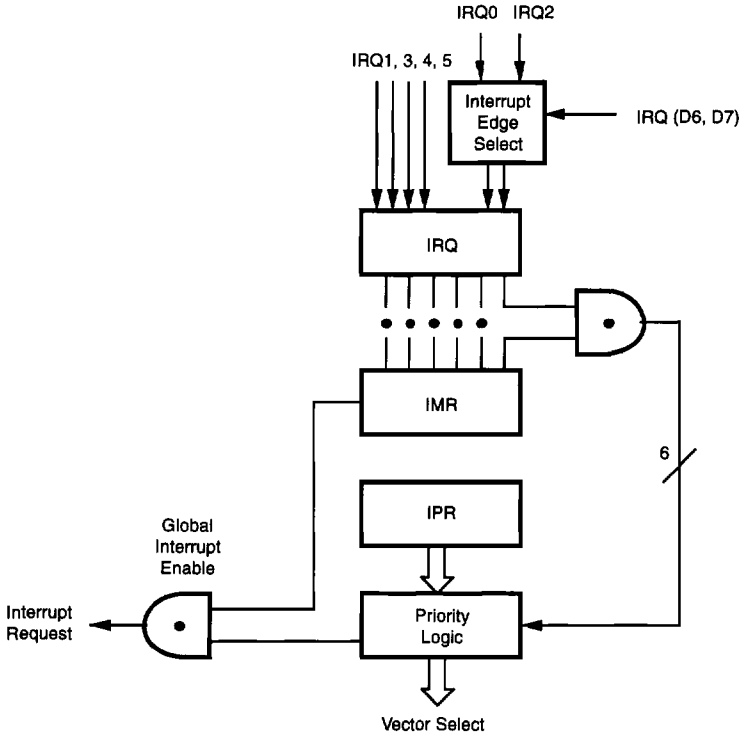


Figure 13. Interrupt Block Diagram

Table 4. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	/DAV0, IRQ0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ1	IRQ1	2, 3	External (P33), Falling Edge Triggered
IRQ2	/DAV2, IRQ2, T_{IN}	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ4	T0	8, 9	Internal
IRQ5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E30/E31 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software may poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in bits D7 and D6 of the IRQ Register (R250). The configuration is shown in Table 5.

Table 5. IRQ Register Configuration

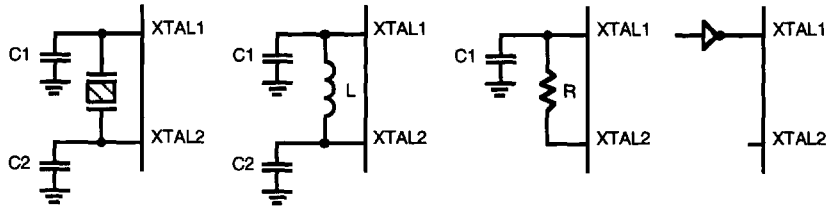
IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86E30/E31 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 kHz to 12 MHz max, with a series resistance (RS) less than or equal to 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the vendor's recommended capacitors from each pin directly to device pin 22 to reduce injection of system ground noise. The RC oscillator option is selected in the programming mode. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 14).

Note: RC OSC does not support 12 MHz.



Ceramic Resonator or Crystal
C1, C2 = 47 pF TYP *
f = 8 MHz

LC
C1, C2 = 22 pF

L = 130 uH *
f = 3 MHz *

RC
@ 5V VCC (TYP)

C1 = 33 pF *
R = 1k *
f = 6.6 MHz *

External Clock

* Typical value including pin parasitics

Figure 14. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power bad to Power OK status
2. STOP-Mode Recovery (if D5 of SMR=0)
3. WDT time-out

The POR time is a nominal 5 ms. Bit 5 of the STOP Mode Register (SMR) determines whether the POR timer is bypassed after STOP-Mode Recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. This instruction turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, and IRQ2 remain active. The device is recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

In order to enter STOP or HALT mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP instruction (opcode=FFH) immediately before the appropriate SLEEP instruction, i.e.:

```
FF  NOP   ; clear the pipeline
6F  STOP  ; enter STOP mode
or
FF  NOP   ; clear the pipeline
7F  HALT  ; enter HALT mode
```

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. STOP mode is terminated by one of the following resets: WDT time-out, POR, or STOP-Mode Recovery Source which is defined by SMR register . This causes the processor to restart the application program at address 000C (HEX).

Port Configuration Register (PCON). The PORT Configuration Register (PCON) configures the ports ndividually: Comparator Output on Port 3, Open-Drain on Port 0, Low EMI Noise on Ports 0, 2, and 3, and Low EMI Noise Oscillator. The PCON Register is located in the Expanded Register File at bank F, location 00 (Figure 15).

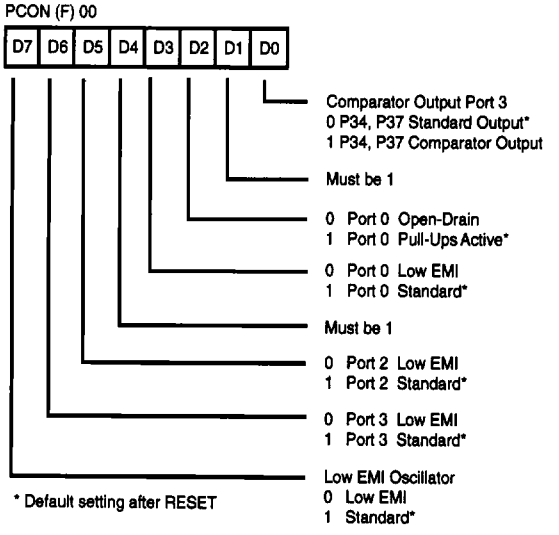


Figure 15. Port Configuration Register (PCON) (Write Only)

Comparator Output Port 3 (D0). Bit 0 controls the comparator use in Port 3. A 1 in this location brings the comparator outputs to P34 and P35 and a 0 releases the Port to its standard I/O configuration.

Port 0 Open-Drain (D1). Port 0 is configured as an open-drain by resetting this bit (D1 = 0) and configured as pull-up active by setting D1 = 1. The default value is 1.

Low EMI Port 0 (D3). Port 0 is configured as a Low EMI Port by resetting this bit (D3 =0) and configured as a Standard Port by setting D3 =1. The default value is 1.

Low EMI Port 2 (D5). Port 2 is configured as a Low EMI Port by resetting this bit (D5 = 0) and configured as a Standard Port by setting D5 = 1. The default value is 1.

Low EMI Port 3 (D6). Port 3 is configured as a Low EMI Port by resetting this bit (D6 = 0) and configured as a Standard Port by setting D6 = 1. The default value is 1.

Low EMI OSC (D7). This bit of the PCON Register controls the low EMI noise oscillator. A1 in this location configures the oscillator with standard drive. While a 0 configures the oscillator with low noise drive; however, it does not affect the relationship of SCLK and XTAL.

STOP-Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP mode recovery (Figure 16). All bits are Write Only except Bit 7 which is a Read Only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the STOP-Mode Recovery Source (Table 7). The SMR is located in Bank F of the Expanded Register Group at address 0BH.

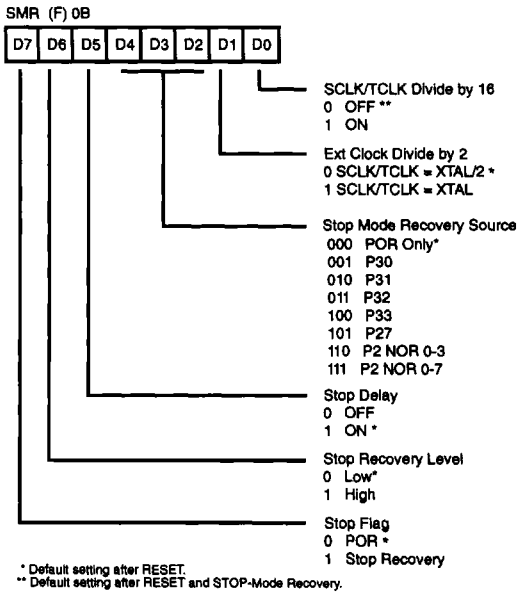


Figure 16. STOP-Mode Recovery Register (Write Only Except D7 Which is Read Only)

FUNCTIONAL DESCRIPTION (Continued)

SCLK/TCLK Divide-by-16 Select (D0). This bit of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (where TCLK sources counter/timers and interrupt logic).

External Clock Divide-By-Two (D1). This bit can eliminate the oscillator divide-by-two circuitry. When this bit is 0, SCLK (System Clock) and TCLK (Timer Clock) are equal to the external clock frequency divided by two. The SCLK/TCLK is equal to the external clock frequency when this bit is set (D1 = 1). Using this bit, together with D7 of PCON, further helps lower EMI [i.e., D7 (PCON) = 0, D1 (SMR) = 1]. The default setting is 0. Maximum frequency is 4 MHz with D1 = 1

STOP-Mode Recovery Source (D2, D3, and D4). These three bits of the SMR register specify the wake-up source of the STOP-Mode Recovery (Figure 17). Table 6 shows the SMR source selected with the setting of D2 to D4. P33-P31 cannot be used to wake up from STOP mode when programmed as analog inputs.

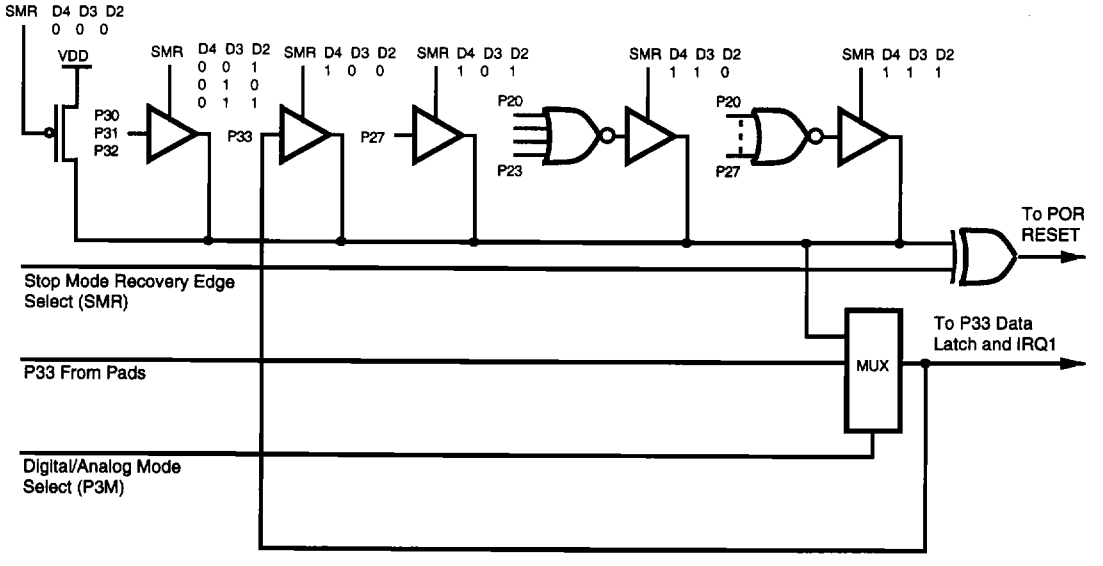


Figure 17. STOP-Mode Recovery Source

Table 6. STOP-Mode Recovery Source

D4	D3	D2	SMR Source selection
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition (Not in analog mode)
0	1	1	P32 transition (Not in analog mode)
1	0	0	P33 transition (Not in analog mode)
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0-3
1	1	1	Logical NOR of Port 2 bits 0-7

STOP-Mode Recovery Delay Select (D5). The 5 ms RESET delay after STOP-Mode Recovery is disabled by programming this bit to a zero. A1 in this bit causes a 5 ms RESET delay after STOP-Mode Recovery. The default condition of this bit is 1. If the fast wake up mode is selected, the STOP-Mode Recovery source must be kept active for at least 5 TpC.

STOP-Mode Recovery Level Select (D6). A 1 in this bit defines that a high level on any one of the recovery sources wakes the Z86E30/E31 from STOP Mode. A 0 defines the low level recovery. The default value is 0.

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit indicates that the device has been reset by POR (cold). A 1 in this bit indicates the device was awakened by a SMR source (warm). This bit is read only.

Watch-Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches terminal count (Figure 18). The WDT is disabled after Power-On Reset and initially enabled by executing the WDT instruction. It is refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled when it has been enabled. The WDT is driven either by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register (Figure 19).

Note: Execution of the WDT instruction affects the Z (Zero), S (Sign), and V (Overflow) flags.

WDTMR Register Accessibility. The WDTMR register is accessible only during the first 64 processor cycles (128 XTAL clock cycles) from the execution of the first instruction after Power-On Reset, Watch-Dog Reset, or a STOP-Mode Recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH.

WDT Time-out Period (D0 and D1). Bits 0 and 1 control a tap circuit that determines the time-out periods that can be obtained. Table 7 shows the time-out period. The default value of D0 and D1 are 1 and 0, respectively.

Table 7. Time-out Period of the WDT

D1	D0	Time-Out of Internal RC OSC	Time-Out of the Crystal Clock
0	0	5 ms	256TpC
0	1	15 ms	512TpC
1	0	25 ms	1024TpC
1	1	100 ms	4096TpC

Notes:
TpC = crystal clock cycle
The default setting is 15 ms.
Values shown are for V_{CC} = 5.0V.

WDT During the HALT Mode (D2). This bit determines whether or not the WDT is active during HALT mode. A1 indicates that the WDT is active during HALT. A 0 disables the WDT in HALT mode. The default value is 1.

WDT During STOP Mode (D3). This bit determines whether or not the WDT is active during STOP mode. A1 indicates active during STOP Mode. A 0 disables the WDT during STOP mode. Since the on-board OSC is stopped during STOP mode, the WDT clock source has to select the on-board RC OSC for the WDT to recover from STOP mode. The default is 1.

Clock Source For WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of the bit is 0, which selects the RC oscillator.

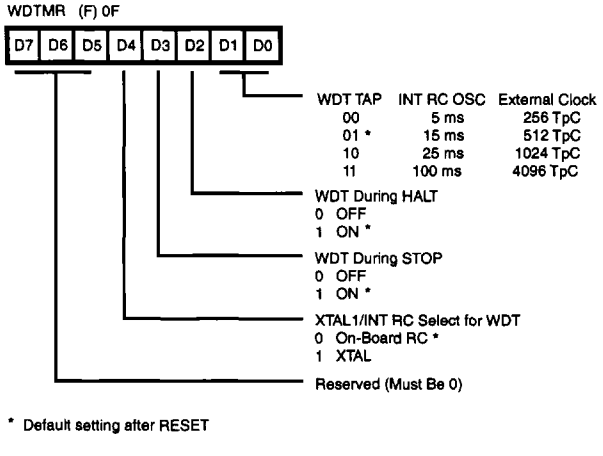


Figure 18. Watch-Dog Timer Mode Register (Write Only)

FUNCTIONAL DESCRIPTION (Continued)

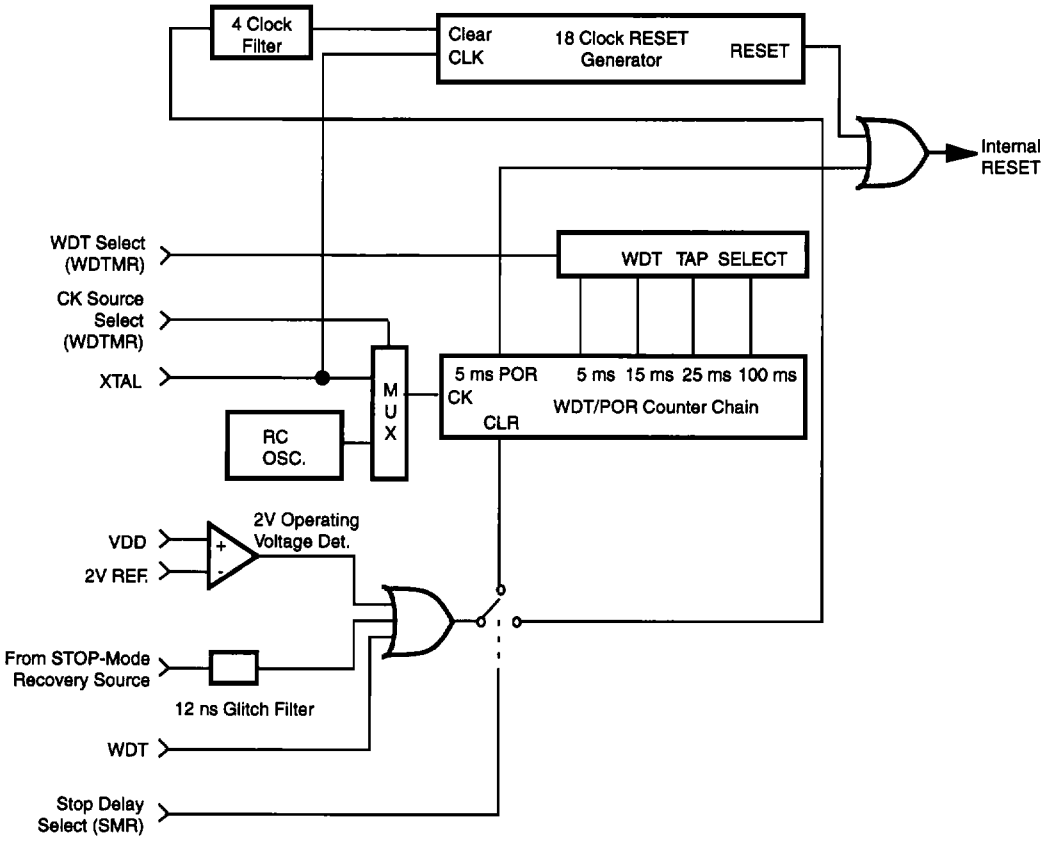


Figure 19. Resets and WDT

Auto Reset Voltage. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below V_{RST} (Figure 20).

If the V_{CC} drops below 4.5V while the device is in operation, the device must be powered down and then re-powered up again. **Note:** V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum Power-On Reset time-out (T_{POR}).

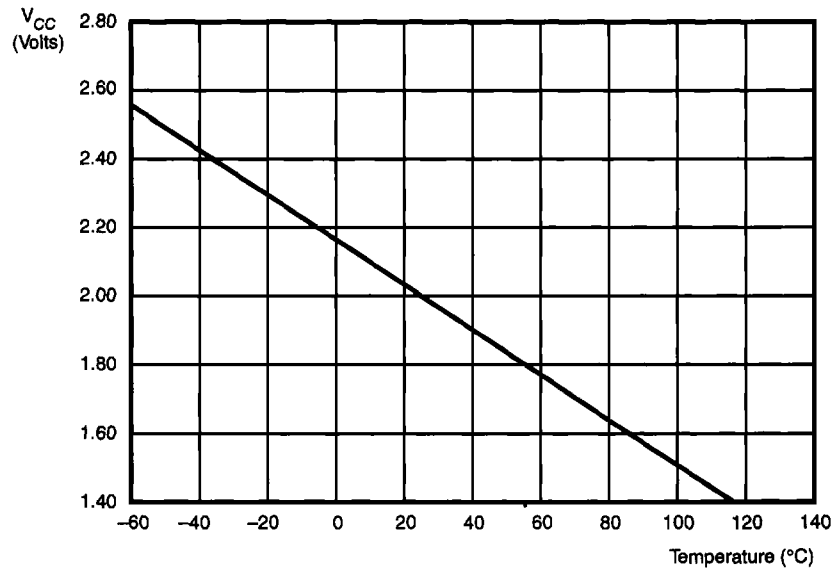


Figure 20. Typical Z86E30/E31 V_{RST} Voltage vs Temperature

FUNCTIONAL DESCRIPTION (Continued)

EPROM Programming Mode

Table 8 shows the programming voltages of each programming mode. Table 9, Figures 21, 22, and 23 show the programming timing of each programming mode. Figure 24 shows the flow-chart of an Intelligent Programming Algorithm, which is compatible with a 2764A EPROM (Z86E30/E31 is 4K/2K EPROM, 2764A is 8K EPROM).

Figure 25 shows the circuit diagram of the Z86E30/E31 programming adaptor which adapts from 2764A to Z86E30/E31. Since the EPROM size of Z86E30/E31 differs from 2764A, the programming address range should be set from 0000H to 0FFFH.

Table 8. EPROM Programming Table

Programming Modes	V_{PP}	EPM	/CE	/OE	/PGM	ADDR	DATA	V_{CC}*
EPROM READ1	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	4.5V†
EPROM READ2	X	V_H	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	5.5V†
PROGRAM	V_H	X	V_{IL}	V_{IH}	V_{IL}	ADDR	In	6.0V
PROGRAM VERIFY	V_H	X	V_{IL}	V_{IL}	V_{IH}	ADDR	Out	6.0V
EPROM PROTECT	V_H	V_H	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RC OSCILLATOR SELECT	V_H	V_{IL}	V_H	V_{IH}	V_{IL}	NU	NU	6.0V
RAM PROTECT	V_H	V_{IH}	V_H	V_{IL}	V_{IL}	NU	NU	6.0V

Notes:
V_H = .12.5V
V_{IH} = As per specific Z8 DC specification.
V_{IL} = As per specific Z8 DC specification.
X = Not used, but must be set to V_H, V_{iH}, or V_{IL} level.
NU = Not used, but must be set to either V_{IH} or V_{IL} level.
I_{PP} during programming = 40 mA maximum.
I_{CC} during programming, verify, or read = 40 mA maximum.
* V_{CC} has a tolerance of ±0.25V.
† Although most progammers do an EPROM read at V_{CC} = 5.0V, Zilog recommends an EPROM read at V_{CC} = 4.5V and 5.0V to ensure proper device operations during the V_{CC} after programming.

Table 9. EPROM Programming Timing

Parameters	Name	Min	Max	Units
1	Address Setup Time	2		µs
2	Data Setup Time	2		µs
3	V_{PP} Setup	2		µs
4	V_{CC} Setup Time	2		µs
5	Chip Enable Setup Time	2		µs
6	Program Pulse Width	0.95		ms
7	Data Hold Time	2		µs
8	/OE Setup Time	2		µs
9	Data Access Time		200	ns
10	Data Output Float Time		100	ns
11	Overprogram Pulse Width	2.85		ms
12	EPM Setup Time	2		µs
13	/PGM Setup Time	2		µs
14	Address to /OE Setup Time	2		µs
15	Option Program Pulse Width	78		ms

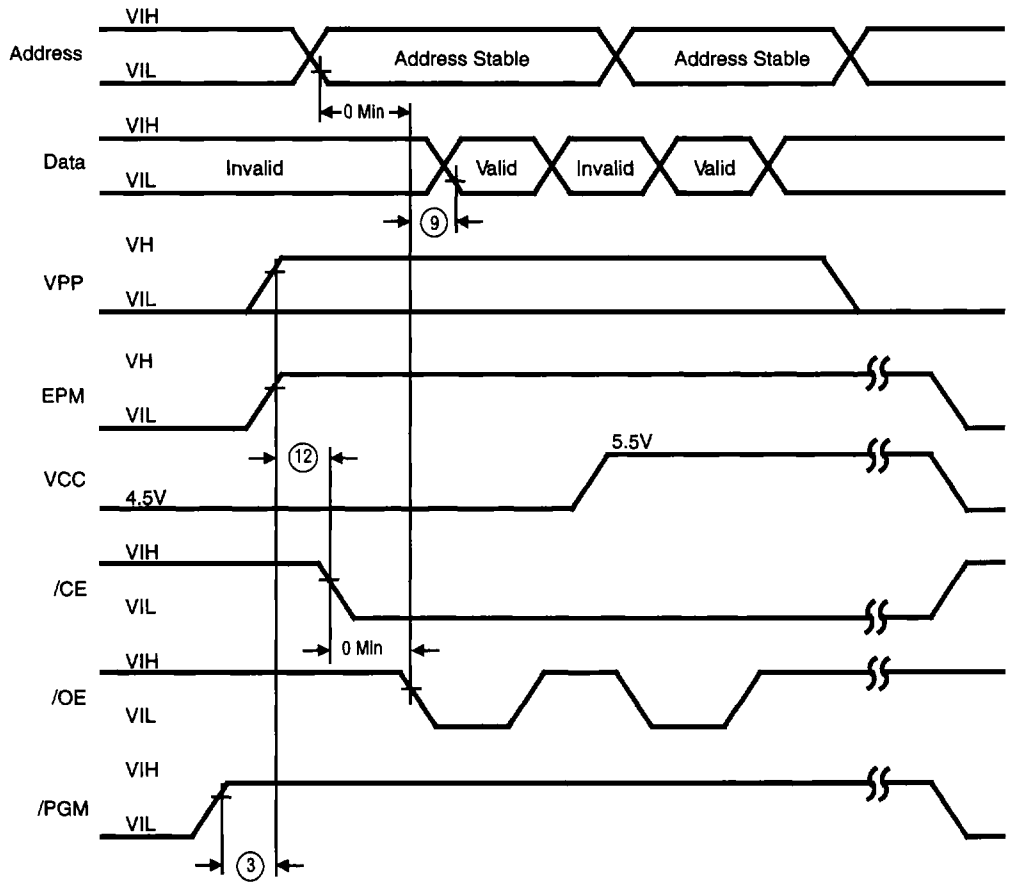


Figure 21. EPROM READ Mode Timing Diagram

FUNCTIONAL DESCRIPTION (Continued)

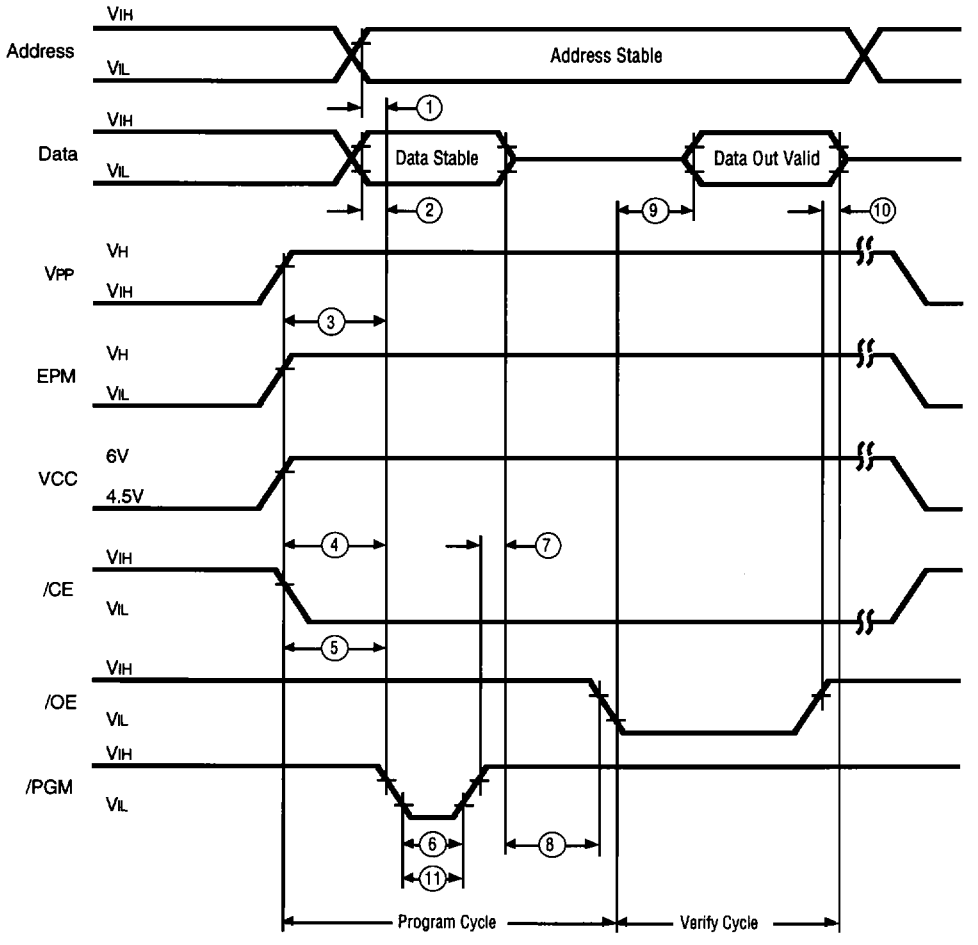


Figure 22. Timing Diagram of EPROM Program and Verify Modes

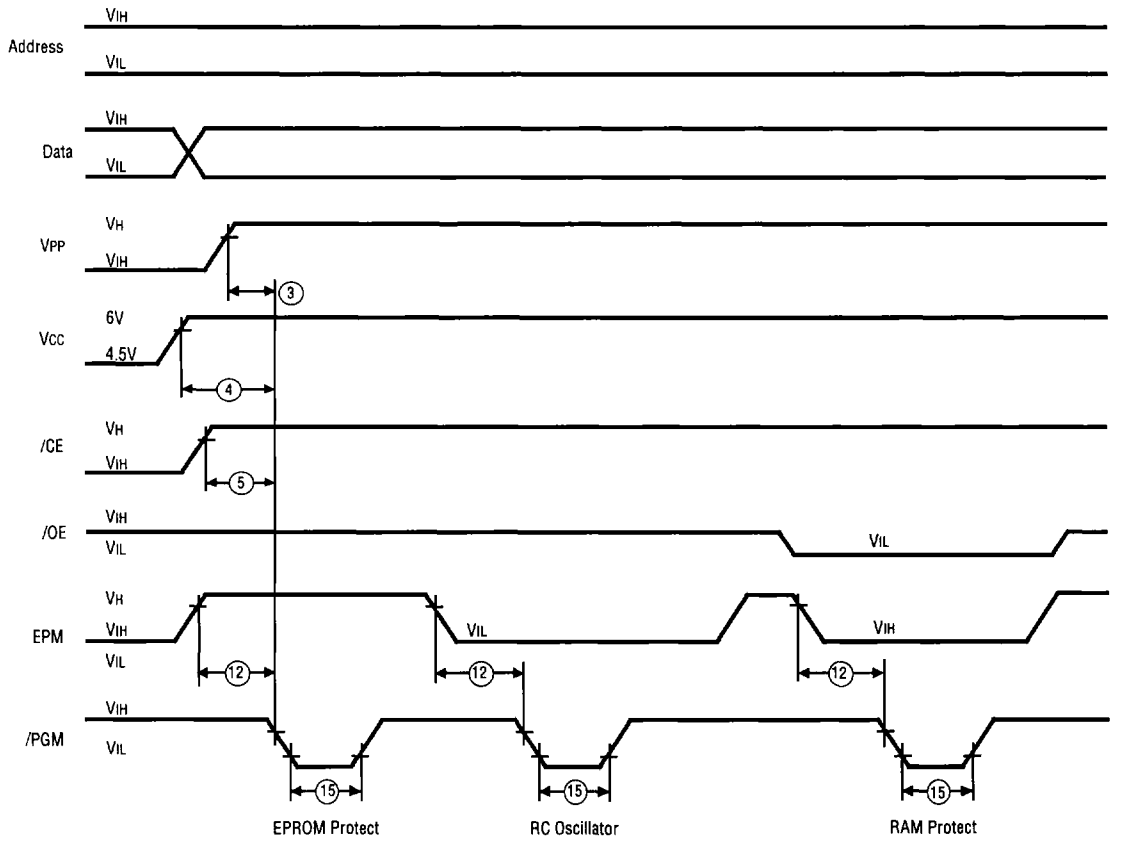


Figure 23. Timing Diagram of EPROM Protect, RAM Protect, and RC OSC Modes

FUNCTIONAL DESCRIPTION (Continued)

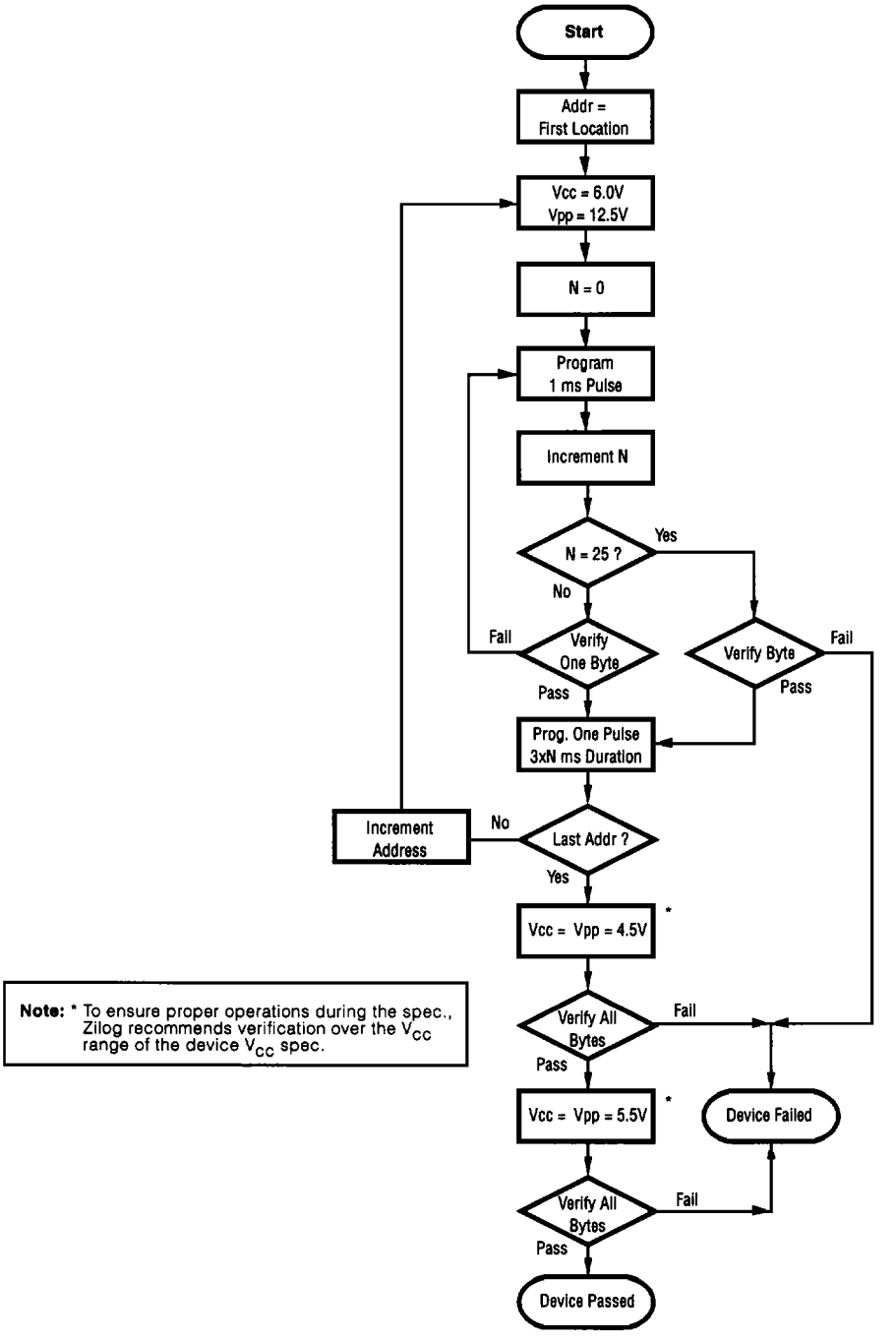


Figure 24. Z86E30/E31 Programming Algorithm

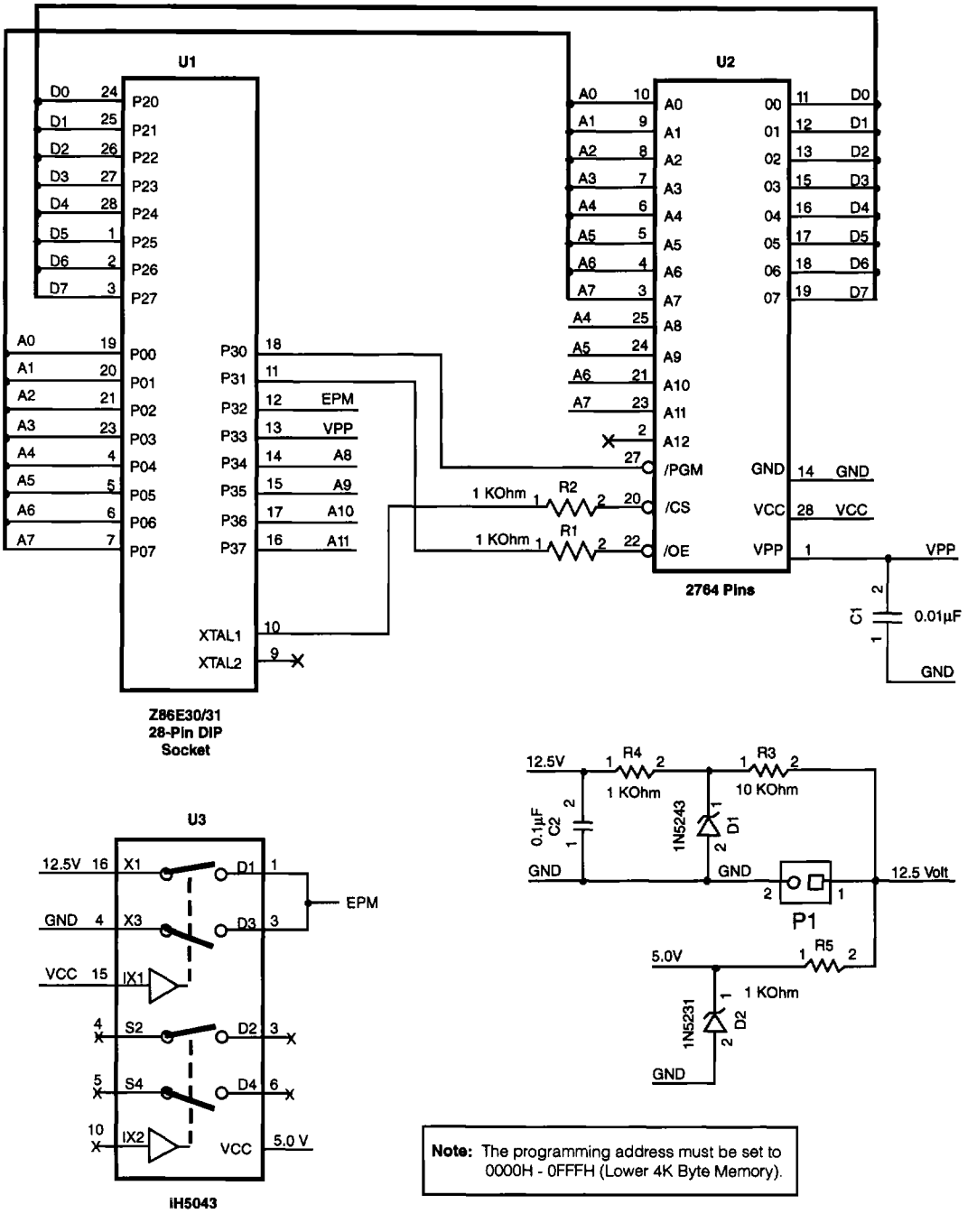


Figure 25. Z86E30/E31 Programming Adaptor Circuitry

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
V_{IHM} **	Max Input Voltage		7	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to Ground.
** Applies to all Port pins, except Port 31, 32, 33 and must limit current going into and out of Port pin to 250 µA maximum.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 26).

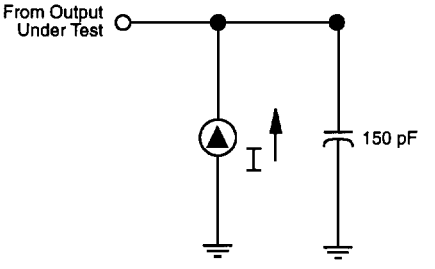


Figure 26. Test Load Configuration

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

V_{CC} SPECIFICATION

V_{CC} = 5.0V ±0.5V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
	Max Input Voltage	5.0V		V_{CC} + 0.5V		V	I_{IN} <250 µA	[7]
V_{CH}	Clock Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} + 0.3V	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	5.0V	0.7 V_{CC}	V_{CC} +0.3	2.5	V		[7]
V_{IL}	Input Low Voltage	5.0V	V_{SS} –0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	5.0V	V_{CC} –0.4		4.8	V	I_{OH} = –2.0 mA	[9]
	(Low EMI Mode)	5.0V	V_{CC} –0.4		4.8	V	I_{OH} = –0.5 mA	[8]
V_{OL1}	Output Low Voltage	5.0V		0.4	0.1	V	I_{OL} = +4.0 mA	[9]
	(Low EMI Mode)	5.0V		0.4	0.1	V	I_{OL} = +1.0 mA	[8]
V_{OL2}	Output Low Voltage	5.0V		1.5	0.3	V	I_{OL} = +12 mA, 3 Pin Max	[9]
V_{OFFSET}	Comparator Input Offset Voltage	5.0V		50	10	mV		
I_{IL}	Input Leakage	5.0V	–10	+10	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	5.0V	–10	+10	< 1	µA	V_{IN} = 0V, V_{CC}	
I_{CC}	Supply Current	5.0V		16	15	mA	@ 8 MHz	[4,5,11]
	(Standard Mode)			20	18	mA	@ 12 MHz	[4,5,11]

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-driven XTAL	0.3 mA	6.0	mA	8 MHz
Crystal or resonator	3.5 mA	6.0	mA	8 MHz

[2] V_{SS}=0V=GND.

[3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} timeout. V_{CC} specified at 4.5V to 5.5V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] CL1 = CL2 = 100 pF.

[6] Same as note [4] except inputs at V_{CC}.

[7] Except clock pins and Port 3 input pins in EPROM mode.

[8] Port Low EMI mode.

[9] Port STD mode.

[10] SMR Reg Bit D1=1.

[11] Z86E30 only.

DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V_{CC} Note[3]	T_A = 0°C to +70°C Min	Max	Typical @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current (Standard Mode)	5.0V		6.0	3.5	mA	HALT mode V_{IN} = 0V, V_{CC} V_{CC} @ 8 MHz	[4,5]
		5.0V		3.0	1.50	mA	Clock Divide-by-16 @ 8 MHz	[4,5]
I_{CC}	Supply Current (SCLK/TCLK = XTAL)	5.0V		7.5	5.0	mA	@ 2 MHz	[4,5,10]
		5.0V		12.0	8.0	mA	@ 4 MHz	[4,5,10]
I_{CC1}	Standby Current (SCLK/TCLK = XTAL)	5.0V		2.0	1.0	mA	@ 2 MHz	[4,5,10]
		5.0V		3.0	1.5	mA	@ 4 MHz	[4,5,10]
I_{CC1}	(Standard Mode)	5.0V		2.0	0.75	mA	Clock Divide-by-16 @ 2 MHz	[4,5]
		5.0V		2.0	1.0	mA	Clock Divide-by-16 @ 4 MHz	[4,5]
I_{CC2}	Standby Current	5.0V		10	2	µA	STOP mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		5.0V		800	450	µA	STOP mode V_{IN} =0V, V_{CC} WDT is Running	[6]
I_{ALL}	Auto Latch Low Current	5.0V		–10	–5	µA	0V < V_{IN} < V_{CC}	
I_{ALH}	Auto Latch High Current	5.0V		20	10	µA	0V < V_{IN} < V_{CC}	
T_{POR}	Power-On Reset	5.0V	2.5		4.5	ms		[3]
V_{RST}	Auto Reset Voltage			3.0	2.6	V		

Notes:

[1] I_{CC1}

	Typ	Max	Unit	Freq
Clock-driven XTAL	0.3 mA	6.0	mA	8 MHz
Crystal or resonator	3.5 mA	6.0	mA	8 MHz

[2] V_{SS}=0V=GND.

[3] V_{CC} must be in the allowed operating range (4.5V to 5.5V) prior to the minimum T_{POR} timeout. V_{CC} specified at 4.5V to 5.5V.

[4] All outputs unloaded, I/O pins floating, inputs at rail.

[5] CL1=CL2=100 pF.

[6] Same as note [4] except inputs at V_{CC}.

[7] Except clock pins and Port 3 input pins in EPROM mode.

[8] Port Low EMI mode.

[9] Port STD mode.

[10] SMR Reg Bit D1=1.

[11] Z86E30 only.

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram (Standard Mode for SCLK/TCLK + XTAL/2)

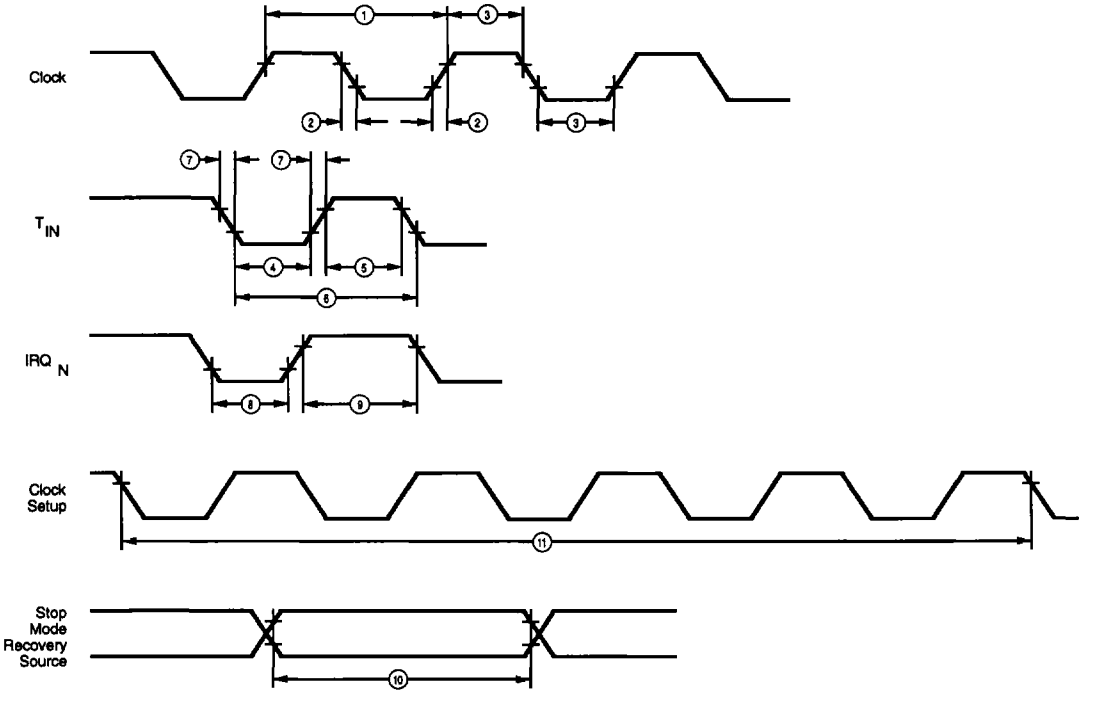


Figure 27. Additional Timing

AC ELECTRICAL CHARACTERISTICS
Additional Timing Table (Standard Mode)

				T_A = 0°C to +70°C					
			V_{CC}	8 MHz [11]		12 MHz [11]			
No	Symbol	Parameter	Note[6]	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	5.0V	125	DC	83.3	DC	ns	[1]
2	TrC,TfC	Clock Input Rise and Fall Times	5.0V		25		15	ns	[1]
3	TwC	Input Clock Width	5.0V	62.5		41.6		ns	[1]
4	TwTinL	Timer Input Low Width	5.0V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	5.0V	5TpC		5TpC			[1]
6	TpTin	Timer Input Period	5.0V	8TpC		8TpC			[1]
7	TpTin TfTin	Timer Input Rise and Fall Timers	5.0V		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	5.0V	70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	5.0V	5TpC		5TpC			[1,3]
9	TwIH	Int. Request Input High Time	5.0V	5TpC		5TpC			[1,2]
10	Twsm	STOP-Mode Recovery Width Spec	5.0V	12		12		ns	
11	Tost	Oscillator Start-up Time	5.0V	5TpC		5TpC			[4]
12	Twdt	Watch-Dog Timer Delay Time	5.0V	5		5		ms	D1 = 0 [5] [7]
			5.0V	15		15		ms	D1 = 0 [5] [8]
			5.0V	25		25		ms	D1 = 1 [5] [9]
			5.0V	100		100		ms	D1 = 1 [5] [10]

Notes:
[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
[2] Interrupt request through Port 3 (P33-P31).
[3] Interrupt request through Port 3 (P30).
[4] SMR – D5 = 0.
[5] Reg. WDTMR.
[6] 5.0V ±0.5V
[7] Reg. WDTMR D1 = 0, D0 = 0.
[8] Reg. WDTMR D1 = 0, D0 = 1.
[9] Reg. WDTMR D1 = 1, D0 = 0.
[10] Reg.WDTMR D1 = 1, D0 = 1.
[11] Z86E30 max frequency = 12 MHz; Z86E31 max frequency = 8 MHz.

AC ELECTRICAL CHARACTERISTICS
Handshake Timing Diagrams

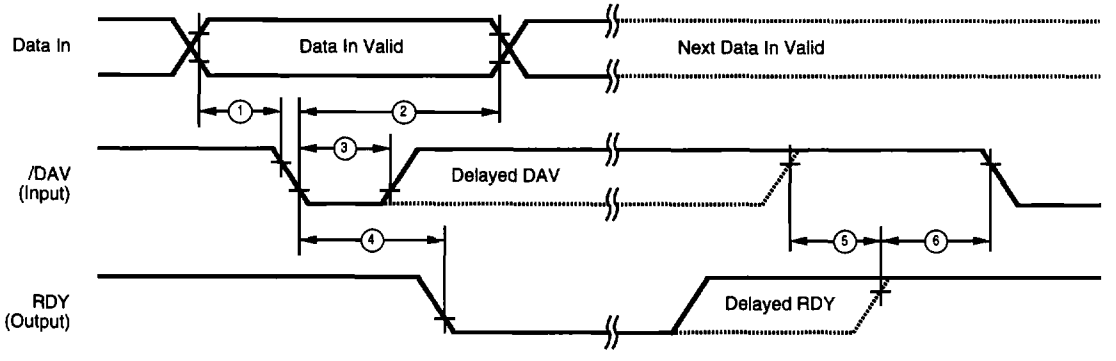


Figure 28. Input Handshake Timing

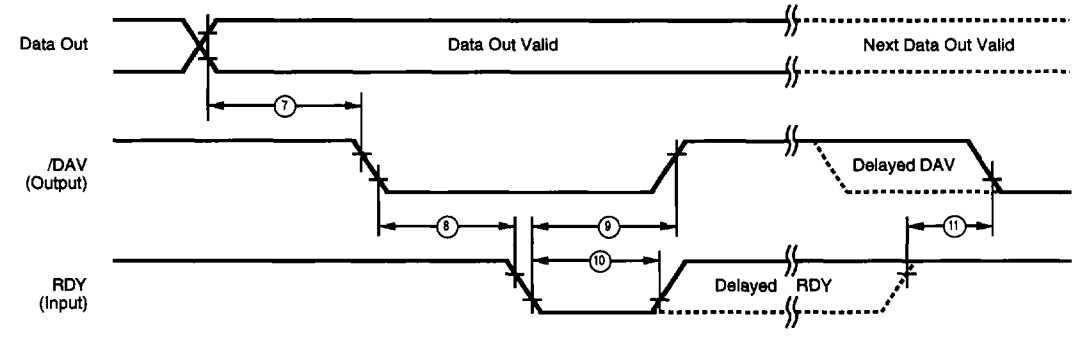


Figure 29. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS

Handshake Timing Table - Standard Mode

No	Symbol	Parameter	V_{CC} Note[1]	T_A = 0°C to +70°C 8 MHz, 12 MHz [2] Min	Max	Data Direction
1	TsDI(DAV)	Data In Setup Time	5.0V	0		IN
2	ThDI(DAV)	Data In Hold Time	5.0V	115		IN
3	TwDAV	Data Available Width	5.0V	110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	5.0V		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	5.0V		80	IN
6	TdRDY0(DAV)	RDY Rise to DAV Fall Delay	5.0V	0		IN
7	TdD0(DAV)	Data Out to DAV Fall Delay	5.0V	63		OUT
8	TdDAV0(RDY)	DAV Fall to RDY Fall Delay	5.0V	0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	5.0V		115	OUT
10	TwRDY	RDY Width	5.0V	80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	5.0V	80	80	OUT

Note:
[1] 5.0V ±0.5V Standard operating temperature range 0°C to +70°C.
[2] Z86E30 max frequency = 12 MHz; Z86E31 max frequency = 8 MHz.

EXPANDED REGISTER FILE CONTROL REGISTERS

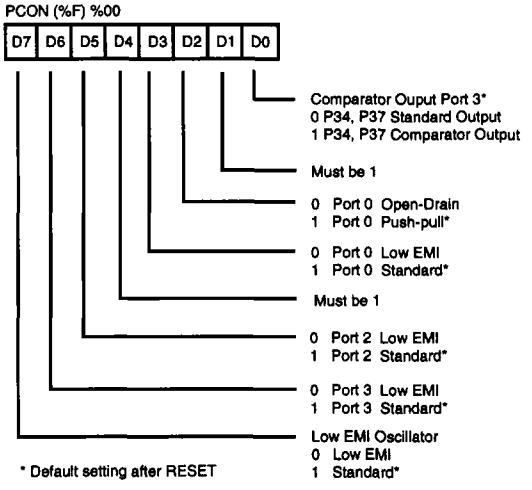


Figure 30. Port Configuration Register (Write Only)

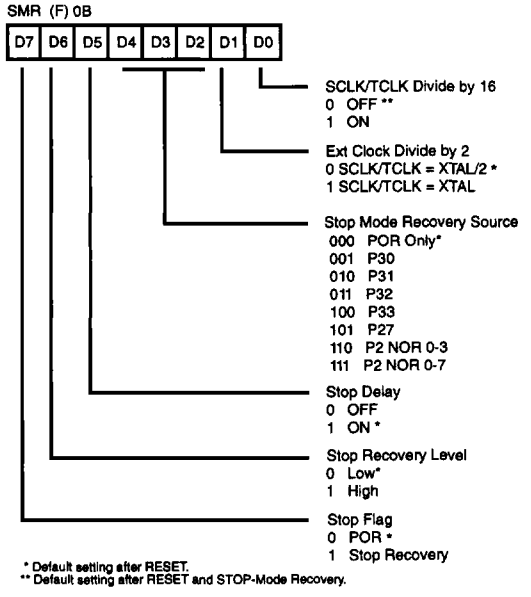


Figure 31. STOP-Mode Recovery Register (Write Only Except Bit D7, Which is Read Only)

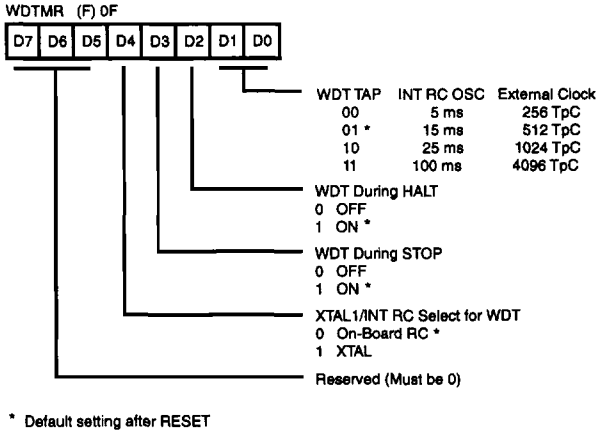


Figure 32. Watch-Dog Timer Mode Register (Write Only)

Z8® CONTROL REGISTER DIAGRAMS

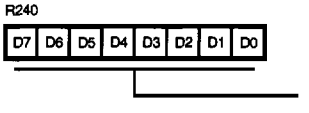


Figure 33. Reserved

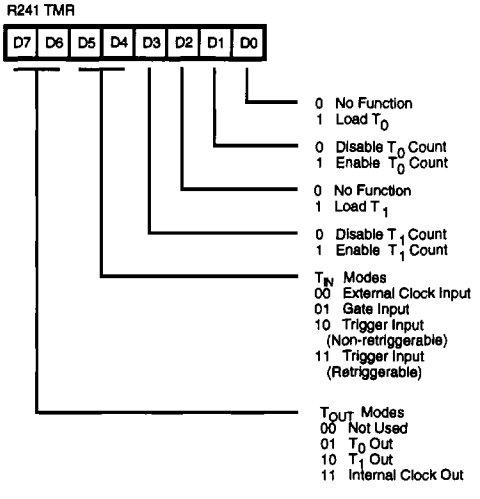


Figure 34. Timer Mode Register ($F1_H$: Read/Write)

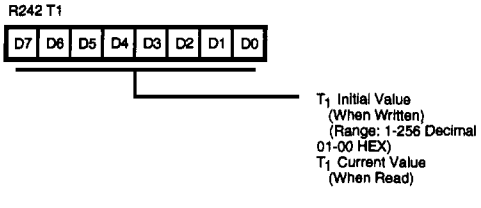


Figure 35. Counter Timer 1 Register ($F2_H$: Read/Write)

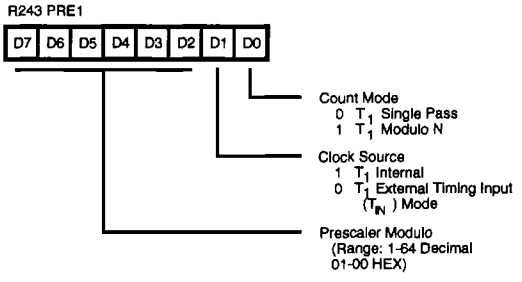


Figure 36. Prescaler 1 Register ($F3_H$: Write Only)

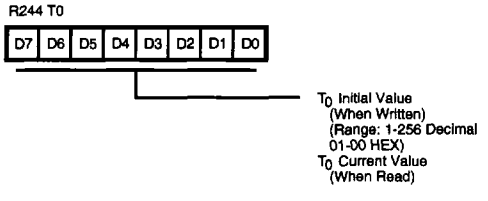


Figure 37. Counter/Timer 0 Register ($F4_H$: Read/Write)

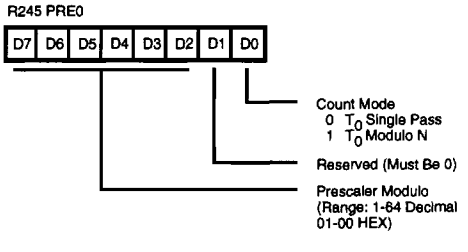


Figure 38. Prescaler 0 Register ($F5_H$: Write Only)

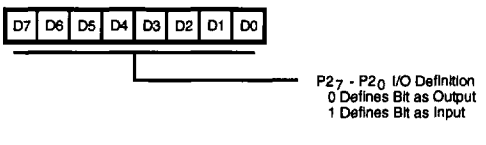


Figure 39. Port 2 Mode Register ($F6_H$: Write Only)

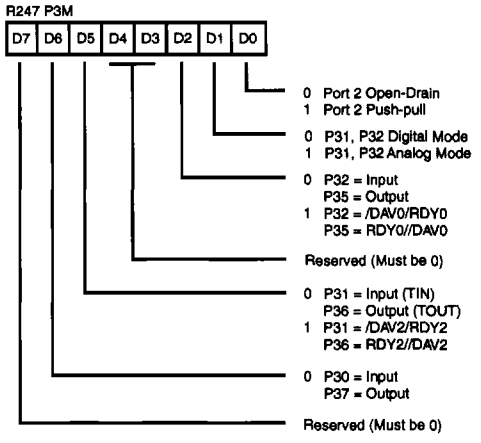


Figure 40. Port 3 Mode Register ($F7_H$: Write Only)

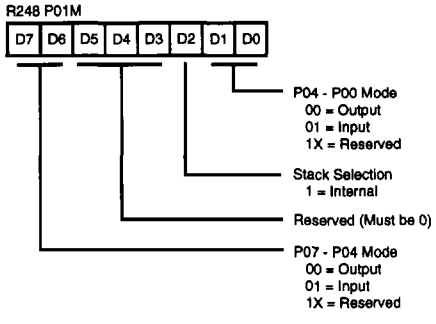


Figure 41. Port 0 and 1 Mode Register ($F8_H$: Write Only)

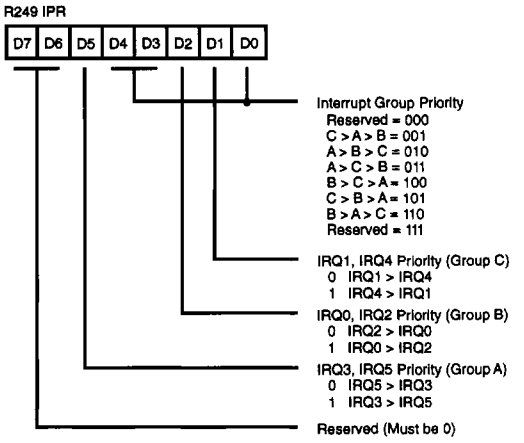


Figure 42. Interrupt Priority Register ($F9_H$: Write Only)

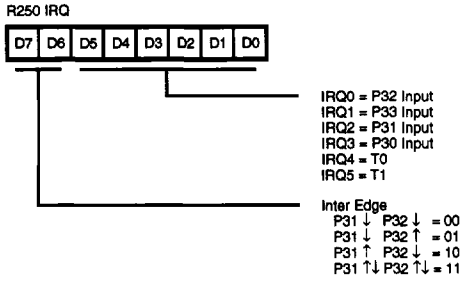


Figure 43. Interrupt Request Register (FA_H: Read/Write)

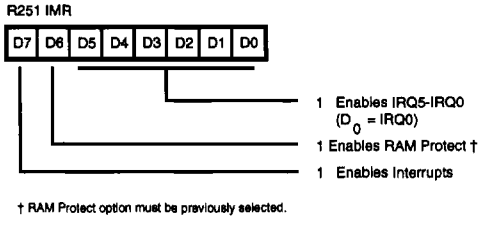


Figure 44. Interrupt Mask Register (FB_H: Read/Write)

Z8® CONTROL REGISTER DIAGRAMS (Continued)

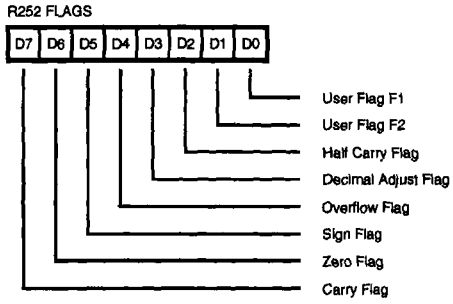


Figure 45. Flag Register (FC_H: Read/Write)

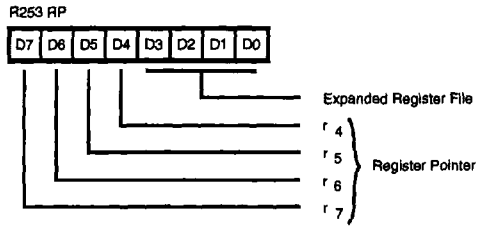


Figure 46. Register Pointer (FD_H: Read/Write)

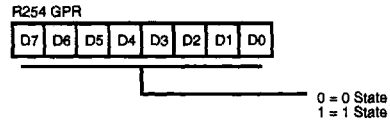


Figure 47. General-Purpose Register

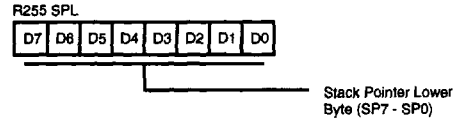


Figure 48. Stack Pointer (FF_H: Read/Write)

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

Affected flags are indicated by:

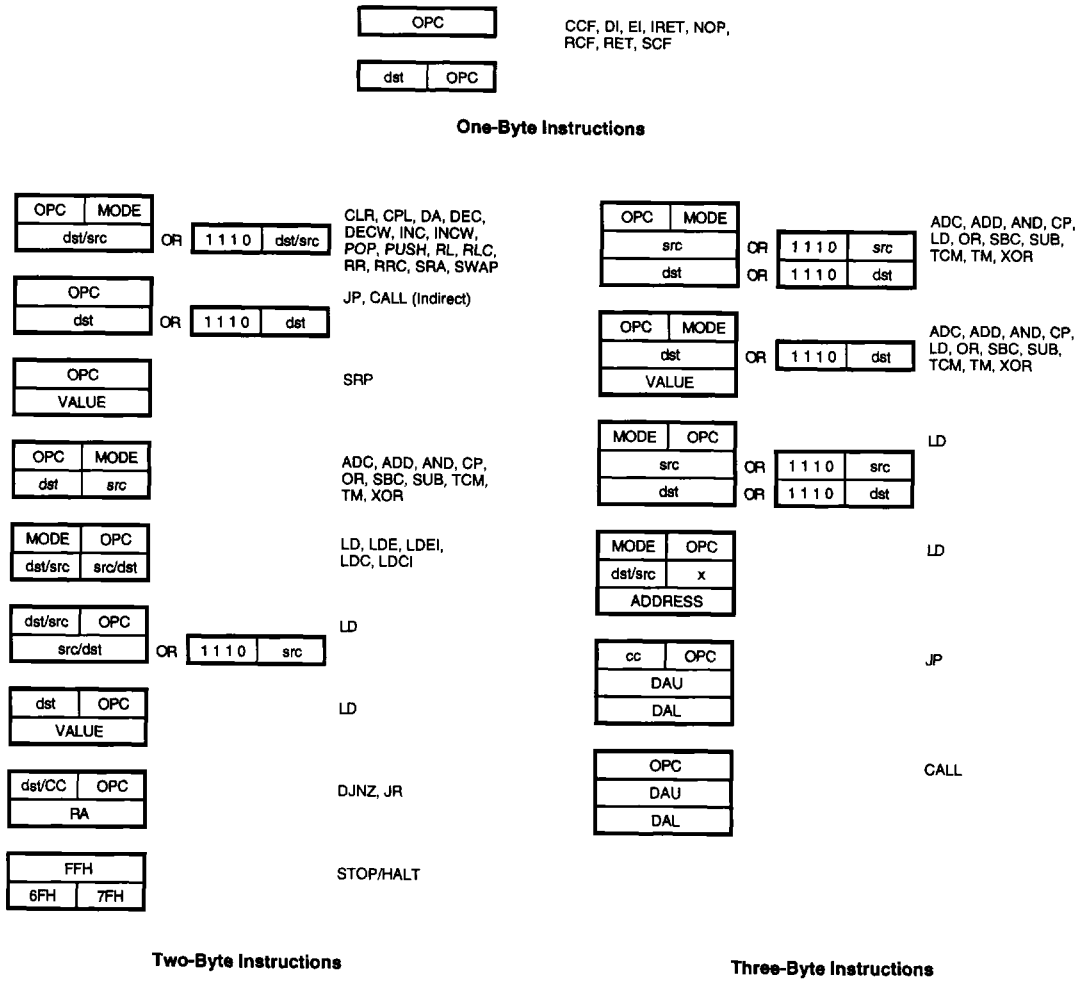
0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

8

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000	F	Never True (Always False)	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location. The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

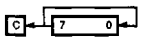
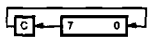
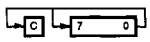
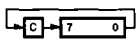
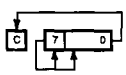
dst (7)

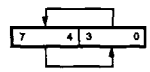
refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src + C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP – 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst – src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst – 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst – 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r – 1 if r ≠ 0 PC←PC + dst Range: +127, –128	RA		rA r = 0 – F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r R IR		rE r = 0 – F 20 21	-	*	*	*	-	-
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 – F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, –128	RA		cB c = 0 – F	-	-	-	-	-	-
LD dst, src dst←src	r r R r X r Ir R R R IR IR	Im R r X r Ir r R IR IM IM R	rC r8 r9 r = 0 – F C7 D7 E3 F3 E4 E5 E6 E7 F5	-	-	-	-	-	-
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP – 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst 	R IR		90 91	*	*	*	*	-	-
RLC dst 	R IR		10 11	*	*	*	*	-	-
RR dst 	R IR		E0 E1	*	*	*	*	-	-
RRC dst 	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst –src – C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst 	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst – src	†		2[ ]	*	*	*	*	1	*
SWAP dst 	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
WDT			5F	-	X	X	X	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

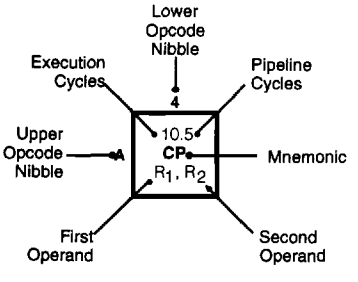
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1	12.0 **LDC** Irr1, r2	18.0 **LDCI** Irr1, Ir2	20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2				3				2					3	1	



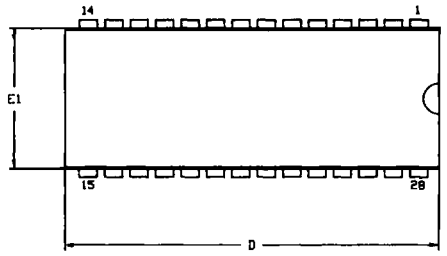
Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_1 = Dst address
R_2 or r_2 = Src address

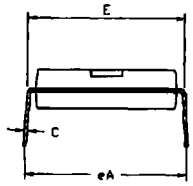
Sequence:
Opcode, First Operand, Second Operand

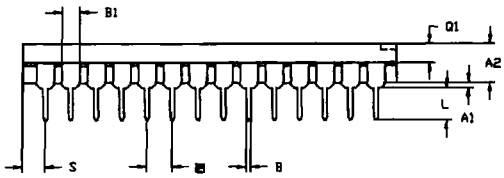
Note: The blanks are reserved.

* 2-byte instruction appears as a 3-byte instruction.

PACKAGE INFORMATION







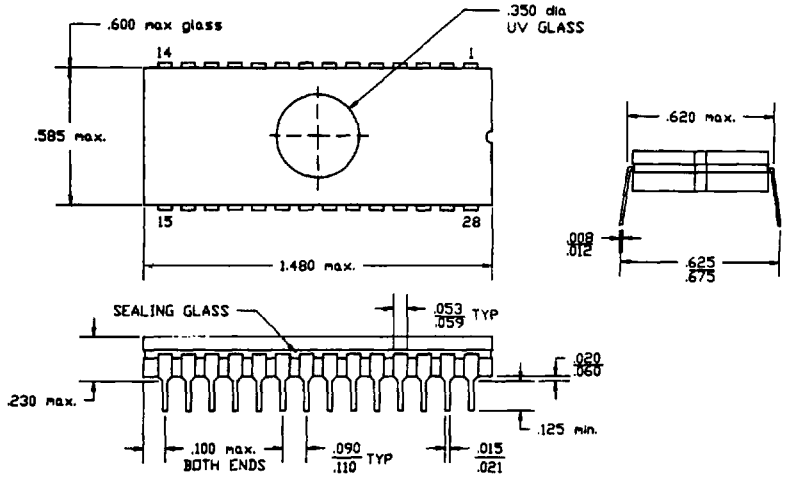
OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	0.81	.020	.032
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.52	1.78	.060	.070
	02	1.27	1.52	.050	.060
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.51	.610	.650
L		3.18	3.81	.125	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

CONTROLLING DIMENSIONS : INCH

28-Pin DIP Package Diagram

PACKAGE INFORMATION (Continued)



28-Pin Window Cerdip Package Diagram

ORDERING INFORMATION

Z86E30 (12 MHz)

28-Pin DIP	28-Pin Cerdip Window Lid
Z86E3012PSC	Z86E3012KSE

Z86E31 (8 MHz)

28-Pin DIP	28-Pin Cerdip Window Lid
Z86E3108PSC	Z86E3108KSE

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

CODES

Preferred Package
P = Plastic DIP

Longer Lead Time
K= Cerdip Window Lid

Temperature
S = 0°C to +70°C

Speeds
08 = 8 MHz
12 = 12 MHz

Environmental
C = Plastic Standard
E = Hermetic Standard

Example:

Z 86E30 12 P S C is a Z86E30, 12 MHz, DIP, 0°C to +70°C, Plastic Standard Flow