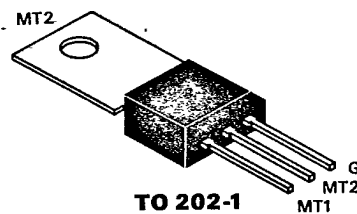


8834750 TAG SEMICONDUCTORS LTD

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TAG SEMICONDUCTORS LTD


**Z0405BE -
Z0405NE TRIACS**
**4.0 A 200-800 V
5/5/5/5 mA**

The Z0405 series of TRIAC's are high performance PNP devices diffused with TAG's proprietary Top Glass™ Process. These parts are intended for general purpose applications where logic compatible gate sensitivity is required.

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions	
Repetitive Peak Off State Voltage	Z0405BE Z0405DE Z0405ME Z0405NE	V_{DRM}	200 400 600 800		V	[$T_j = -40^\circ\text{C}$ to 125°C] [$R_{GK} = 1\text{K}\Omega$]	
On-State Current		$I_T(\text{RMS})$	4.0		A		All Conduction Angles $T_C = 75^\circ\text{C}$
Nonrept. On-State Current		I_{TSM}	25		A		Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	22		A		Half Cycle, 50 Hz
Fusing Current		I^2t	2.4		A^2s	$t = 10\text{ ms}$	
Peak Gate Current		I_{GM}	1.2		A	$10\mu\text{s}$ max.	
Peak Gate Dissipation		P_{GM}	3		W	$10\mu\text{s}$ max.	
Gate Dissipation		$P_{G(\text{AV})}$	0.2		W	20 ms max.	
Operating Temperature		T_j	-40	125	$^\circ\text{C}$		
Storage Temperature		T_{stg}	-40	150	$^\circ\text{C}$		
Soldering Temperature		T_{sld}		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.	

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}		200	μA	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 125^\circ\text{C}$
Off-State Leakage Current	I_{DRM}		5	μA	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 25^\circ\text{C}$
On-State Voltage	V_T		2.10	V	at $I_T = 6.0\text{ A}$, $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(\text{TO})}$		0.95	V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	r_T		180	$\text{m}\Omega$	$T_j = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT\text{ I}+}$ (1)		5	mA	$V_D = 12\text{ V}$
	$I_{GT\text{ I}-}$ (2)		5	mA	$V_D = 12\text{ V}$
	$I_{GT\text{ III}-}$ (3)		5	mA	$V_D = 12\text{ V}$
	$I_{GT\text{ III}+}$ (4)		5	mA	$V_D = 12\text{ V}$
Gate Trigger Voltage	V_{GT}		2	V	$V_D = 12\text{ V}$ All Quadrants
Holding Current	I_H		5	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	dv/dt	30		$\text{V}/\mu\text{s}$	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 125^\circ\text{C}$
Critical Rate of Rise, Off-State	dv/dt_c	1		$\text{V}/\mu\text{s}$	$I_T = 4.0\text{ A}$ $di/dt = 1.78\text{ A/ms}$ $T_C = 75^\circ\text{C}$
Thermal Resistance junc. to case	$R_{\theta jc}$		7.5	K/W	
Thermal Resistance junc. to amb.	$R_{\theta ja}$		60	K/W	

Z04