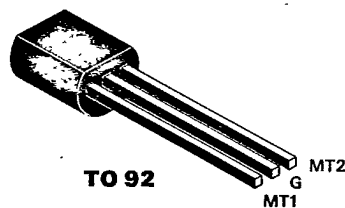


TAG SEMICONDUCTORS LTD


**Z0102BA -  
Z0102NA TRIACS**
**1.0 A 200-800 V  
3/3/3/3 mA**

The Z0102 series of TRIAC's are high performance PNP devices diffused with TAG's proprietary Top Glass™ Process. These parts are intended for general purpose applications where logic compatible gate sensitivity is required.

**Absolute Maximum Ratings**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	<b>Z0102BA</b>	$V_{DRM}$	200		V	[ $T_j = -40^\circ\text{C}$ to $125^\circ\text{C}$ ] [ $R_{GK} = 1\text{K}\Omega$ ]
	<b>Z0102DA</b>		400		V	
	<b>Z0102MA</b>		600		V	
	<b>Z0102NA</b>		800		V	
On-State Current		$I_T(\text{RMS})$	0.8		A	All Conduction Angles $T_C = 50^\circ\text{C}$
Nonrept. On-State Current		$I_{TSM}$	22		A	Half Cycle, 60 Hz
Nonrept. On-State Current		$I_{TSM}$	20		A	Half Cycle, 50 Hz
Fusing Current		$I^2t$	2		$\text{A}^2\text{s}$	$t = 10\text{ ms}$
Peak Reverse Gate Voltage		$V_{GRM}$	8		V	
Peak Gate Current		$I_{GM}$	1.2		A	10 $\mu\text{s}$ max.
Peak Gate Dissipation		$P_{GM}$	3		W	10 $\mu\text{s}$ max.
Gate Dissipation		$P_{G(AV)}$	0.2		W	20 ms max.
Operating Temperature		$T_j$	-40	125	$^\circ\text{C}$	
Storage Temperature		$T_{stg}$	-40	150	$^\circ\text{C}$	
Soldering Temperature		$T_{slid}$		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	$I_{DRM}$		200	$\mu\text{A}$	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 125^\circ\text{C}$
Off-State Leakage Current	$I_{DRM}$		5	$\mu\text{A}$	$V_D = V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 25^\circ\text{C}$
On-State Voltage	$V_T$		1.26	V	at $I_T = 1.2\text{ A}$ , $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(TO)}$		0.95	V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	$r_T$		200	$\text{m}\Omega$	$T_j = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT I+}$ (1)		3	mA	$V_D = 12\text{ V}$
	$I_{GT I-}$ (2)		3	mA	$V_D = 12\text{ V}$
	$I_{GT III-}$ (3)		3	mA	$V_D = 12\text{ V}$
	$I_{GT III+}$ (4)		3	mA	$V_D = 12\text{ V}$
Gate Trigger Voltage	$V_{GT}$		2	V	$V_D = 12\text{ V}$ All Quadrants
Holding Current	$I_H$		3	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	$dv/dt$	30		$\text{V}/\mu\text{s}$	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\text{K}\Omega$ $T_j = 125^\circ\text{C}$
Critical Rate of Rise, Off-State	$dv/dt_c$	1		$\text{V}/\mu\text{s}$	$I_T = 0.8\text{ A}$ $di/dt = 0.35\text{ A/ms}$ $T_C = 50^\circ\text{C}$
Gate Controlled Delay Time	$t_{gd}$		2.5	$\mu\text{s}$	$I_G = 15\text{ mA}$ $di/dt = 0.15\text{ A}/\mu\text{s}$
Thermal Resistance junc. to case	$R_{\theta jc}$		90	K/W	
Thermal Resistance junc. to amb.	$R_{\theta ja}$		180	K/W	

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