Standard 2K x 8 SRAM

Features

- 2048 x 8 bit static CMOS RAM
- 70 and 85 ns Access Times
- Common data inputs and data outputs
- Three-state outputs
- Typ. operating supply current
  70 ns: 30 mA
  85 ns: 28 mA
- Data retention current at 3 V:
  < 10 µA (standard)
- Standby current standard < 30 µA
- Standby current low power (L)
  < 5 µA
- Standby current for L-version at 25 °C and 5 V: typ. 50 nA
- TTL/CMOS-compatible
- Automatical reduction of power-dissipation in long Read or Write cycles
- Power supply voltage 5 V
- Operating temperature ranges
  0 to 70 °C
  -40 to 85 °C
- CECC 90000 Quality Standard
- ESD protection > 2000 V
  (MIL STD 883C M3015.7)
- Latch-up immunity >100 mA
- Packages: PDIP24 (600 mil)
  SOP24 (300 mil)

Description

The U6216A is a static RAM manufactured using a CMOS process technology with the following operating modes:

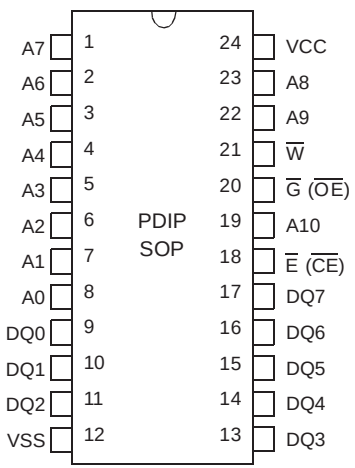
- Read - Standby
- Write - Data Retention

The memory array is based on a 6-transistor cell.

The circuit is activated by the falling edge of $\overline{E}$. The address and control inputs open simultaneously. According to the information of $\overline{W}$ and $\overline{G}$, the data inputs, or outputs, are active. During the active state $\overline{E}$ = L each address change leads to a new Read or Write cycle. In a Read cycle, the data outputs are activated by the falling edge of $\overline{G}$, afterwards the data word read will be available at the outputs DQ0 - DQ7. After the address change, the data outputs go High-Z until the new information read is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals $\overline{W}$ or $\overline{G}$, the operating current (I_O = 0 mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of $\overline{W}$, or by the rising edge of $\overline{E}$, respectively.

Data retention is guaranteed down to 2 V. With the exception of $\overline{E}$, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required.

Pin Configuration

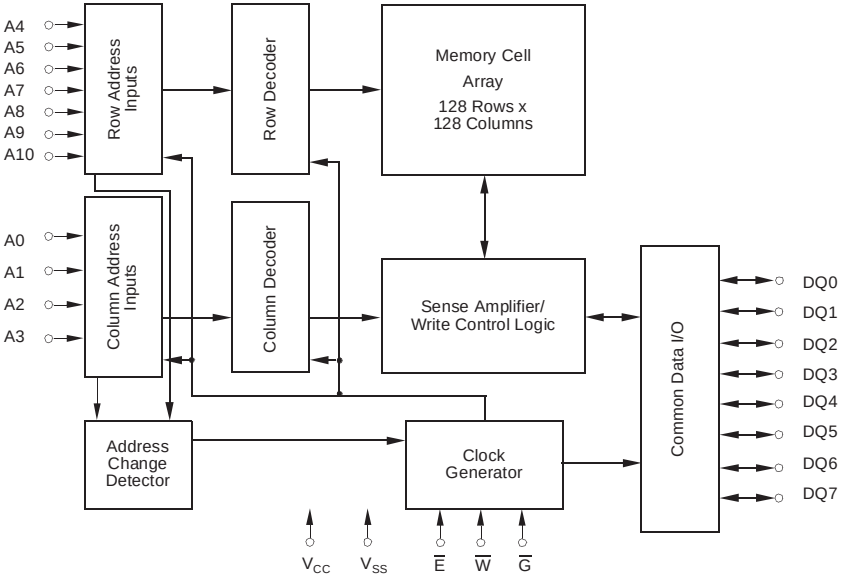


Top View

Pin Description

Signal Name	Signal Description
A0 - A10	Address Inputs
DQ0 - DQ7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

Block Diagram



Truth Table

Operating Mode	$\overline{E}$	$\overline{W}$	$\overline{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

* H or L

Characteristics

All voltages are referenced to V_{SS} = 0 V (ground).
All characteristics are valid in the power supply voltage range and in the operating temperature range specified.
Dynamic measurements are based on a rise and fall time of ≤ 5 ns, measured between 10 % and 90 % of V_I, as well as input levels of V_{IL} = 0 V and V_{IH} = 3 V. The timing reference level of all input and output signals is 1.5 V, with the exception of the t_{dis}-times and $t_{t(QX)}$, in which cases transition is measured ± 200 mV from steady-state voltage.

Maximum Ratings		Symbol	Min.	Max.	Unit
Power Supply Voltage		V_{CC}	-0.5	7	V
Input Voltage		V_I	-0.5	V_{CC} + 0.5	V
Output Voltage		V_O	-0.5	V_{CC} + 0.5	V
Power Dissipation		P_D		1	W
Operating Temperature	C-Type K-Type	T_a	0 -40	70 85	°C °C
Storage Temperature		T_{stg}	-55	125	°C

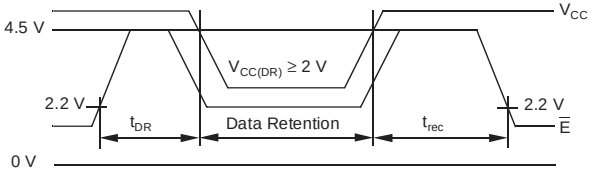
Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		4.5	5.5	V
Data Retention Voltage	$V_{CC(DR)}$		2.0		V
Input Low Voltage*	V_{IL}		-0.3	0.8	V
Input High Voltage	V_{IH}		2.2	V_{CC} + 0.3	V

* -1 V at Pulse Width 50 ns

Electrical Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply Current - Operating Mode	$I_{CC(OP)}$	V_{CC} = 5.5 V V_{IL} = 0.8 V V_{IH} = 2.2 V t_{cW} = 70 ns = 85 ns		50 45	mA mA
Supply Current - Standby Mode (CMOS level) Standard Low Power (L)	$I_{CC(SB)}$	V_{CC} = 5.5 V $V_{(\overline{E})}$ = V_{CC} - 0.2 V		 30 5	 µA µA
Supply Current - Standby Mode (TTL level)	$I_{CC(SB)1}$	V_{CC} = 5.5 V $V_{(\overline{E})}$ = 2.2 V		3	mA
Supply Current - Data Retention Mode (Standard)	$I_{CC(DR)}$	$V_{CC(DR)}$ = 3 V = 2 V $V_{(\overline{E})}$ = $V_{CC(DR)}$ - 0.2 V		10 5	µA µA
Output High Voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -1.0 mA	2.4		V
Output Low Voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 4.0 mA		0.4	V
Input High Leakage Current	I_{IH}	V_{CC} = 5.5 V V_{IH} = 5.5 V		2	µA
Input Low Leakage Current	I_{IL}	V_{CC} = 5.5 V V_{IL} = 0 V	-2		µA
Output High Current	I_{OH}	V_{CC} = 4.5 V V_{OH} = 2.4 V		-1	mA
Output Low Current	I_{OL}	V_{CC} = 4.5 V V_{OL} = 0.4 V	4		mA
Output Leakage Current High at Three-State Outputs	I_{OHZ}	V_{CC} = 5.5 V V_{OH} = 5.5 V		2	µA
Low at Three-State Outputs	I_{OLZ}	V_{CC} = 5.5 V V_{OL} = 0 V	-2		µA

Switching Characteristics	Symbol		Min.		Max.		Unit
	Alt.	IEC	07	08	07	08	
Time to Output in Low-Z	t_{LZ}	$t_{t(QX)}$	5	5	10	10	ns
Cycle Time							
Write Cycle Time	t_{WC}	t_{cW}	70	85			ns
Read Cycle Time	t_{RC}	t_{cR}	70	85			ns
Access Time							
$\overline{E}$ LOW to Data Valid	t_{ACE}	$t_{a(E)}$			70	85	ns
$\overline{G}$ LOW to Data Valid	t_{OE}	$t_{a(G)}$			35	45	ns
Address to Data Valid	t_{AA}	$t_{a(A)}$			70	85	ns
Pulse Widths							
Write Pulse Width	t_{WP}	$t_{w(W)}$	40	50			ns
Chip Enable to End of Write	t_{CW}	$t_{w(E)}$	45	55			ns
Setup Times							
Address Setup Time	t_{AS}	$t_{su(A)}$	0	0			ns
Chip Enable to End of Write	t_{CW}	$t_{su(E)}$	45	55			ns
Write Pulse Width	t_{WP}	$t_{su(W)}$	40	50			ns
Data Setup Time	t_{DS}	$t_{su(D)}$	30	30			ns
Data Hold Time	t_{DH}	$t_{h(D)}$	0	0			ns
Address Hold from End of Write	t_{AH}	$t_{h(A)}$	0	0			ns
Output Hold Time from Address Change	t_{OH}	$t_{v(A)}$	5	5			ns
$\overline{E}$ HIGH to Output in High-Z	t_{HZCE}	$t_{dis(E)}$	0	0	30	30	ns
$\overline{W}$ LOW to Output in High-Z	t_{HZWE}	$t_{dis(W)}$	0	0	25	30	ns
$\overline{G}$ HIGH to Output in High-Z	t_{HZOE}	$t_{dis(G)}$	0	0	30	30	ns

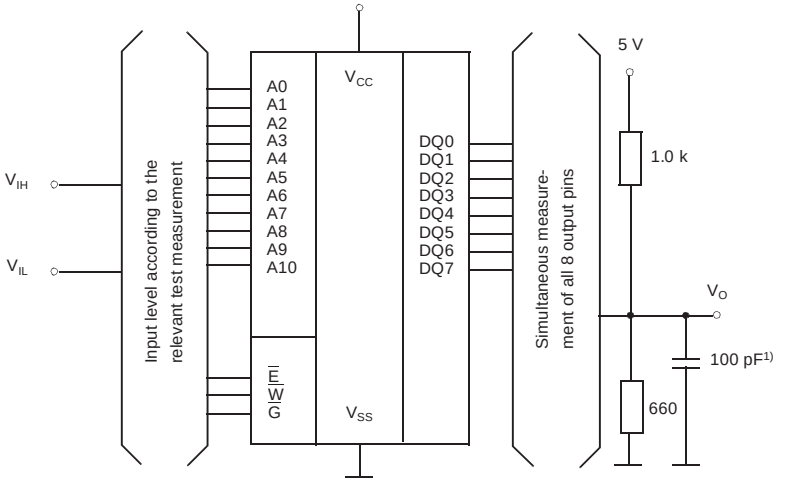
Data Retention Mode



$V_{CC(DR)} - 0.2\ V \leq V_{\overline{E}(DR)} \leq V_{CC(DR)} + 0.3\ V$

Chip Deselect to Data Retention Time	t_{DR}:	min 0 ns
Operating Recovery Time	t_{rec}:	min t_{cR}

Test Configuration for Functional Check



[1)] In measurement of $t_{dis(E)}$, $t_{dis(W)}$, $t_{dis(G)}$, $t_{t(QX)}$ the capacitance is 5 pF.

Capacitance	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	V_{CC} = 5.0 V V_I = V_{SS}	C_I		7	pF
Output Capacitance	f = 1 MHz T_a = 25 °C	C_O		7	pF

All pins not under test must be connected with ground by capacitors.

IC Code Numbers

Example

U6216A D K 07 L

Typ

Package
D = PDIP
S = SOP

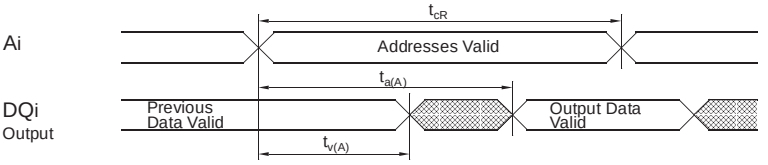
Operating Temperature Range
C = 0 to 70 °C
K = -40 to 85 °C

Access Time
07 = 70 ns
08 = 85 ns

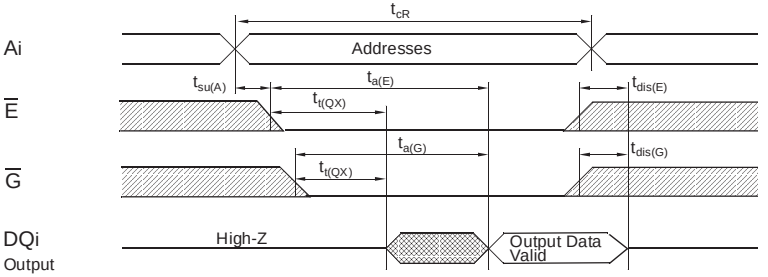
Power Consumption
= Standard
L = Low Power

The date of manufacture is given by the 4 last digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

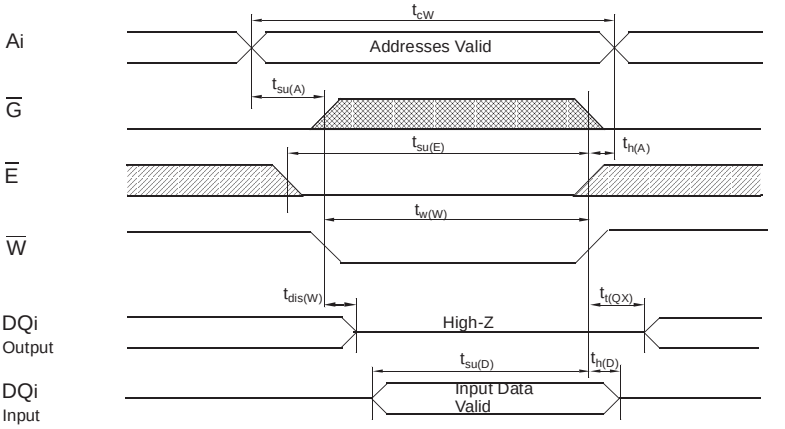
Read Cycle 1 (during Read cycle : $\overline{E} = \overline{G} = V_{IL}$, $\overline{W} = V_{IH}$)



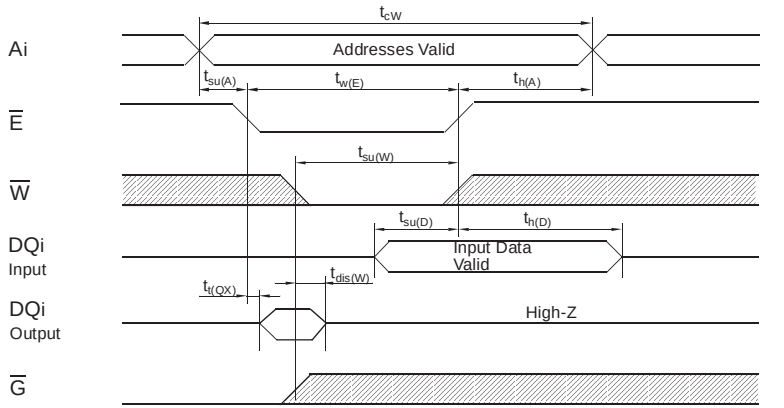
Read Cycle 2 (during Read cycle: $\overline{W} = V_{IH}$)



Write Cycle1 ($\overline{W}$-controlled)



Write Cycle 2 ($\overline{E}$-controlled)



undefined L- or H-level

Zentrum Mikroelektronik Dresden

Memory Products 1998
Standard 2K x 8 SRAM U6216A

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