24 W BTL OR 2 × 12 W STEREO CAR RADIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA1510/TDA1510A is a class-B integrated output amplifier encapsulated in a 13-lead single in-line (SIL) plastic power package. Developed primarily for car radio application, the device can also be used to drive low impedance loads (down to 1,6 Ω). With a supply voltage (V_P) of 14,4 V, an output power of 24 W can be delivered into a 4 Ω Bridge Tied Load (BTL), or when used as a stereo amplifier, 2 x 12 W into 2 Ω or 2 x 7 W into 4 Ω.

Features

- Flexibility – stereo as well as mono BTL
- Low offset voltage at the output (important for BTL)
- Load dump protection
- A.C. short-circuit-safe to ground
- Low number, small sized external components
- Internal limiting of bandwidth for high frequencies
- High output power
- Large useable gain variation
- Good ripple rejection
- Thermal protection
- Low stand-by current possibility
- High reliability

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range:						
operating		V_P	6,0	14,4	18,0	V
non-operating		V_P	–	–	28,0	V
non-operating, load dump protection		V_P	–	–	45,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current		I_{so}	0,15	0,35	0,80	mA
Input impedance	pins 1, 2, 12 and 13	$\lvert Z_I \rvert$	1	–	–	MΩ
Storage temperature range		T_{stg}	–65	–	+ 150	°C
Crystal temperature		T_c	–	–	150	°C

PACKAGE OUTLINES

TDA1510: 13-lead SIL-bent-to-DIL; plastic power (SOT141B).
TDA1510A: 13-lead SIL-bent-to-DIL; plastic power (SOT141C).

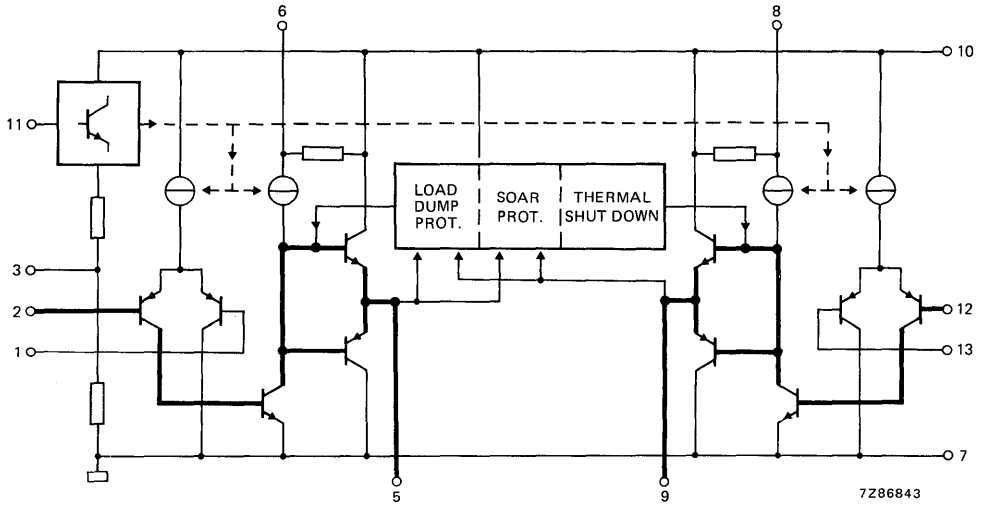
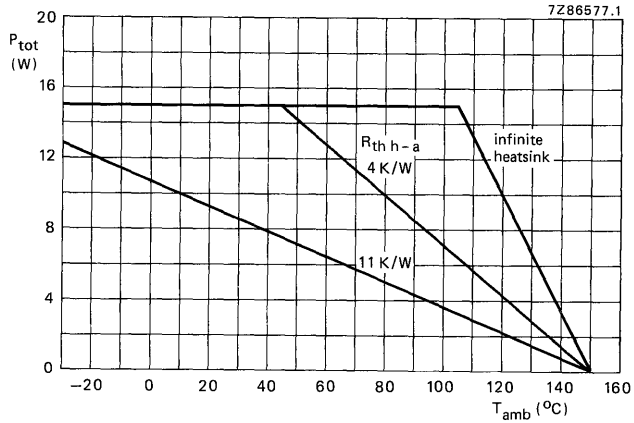


Fig. 1 Functional diagram; heavy lines indicate signal paths.

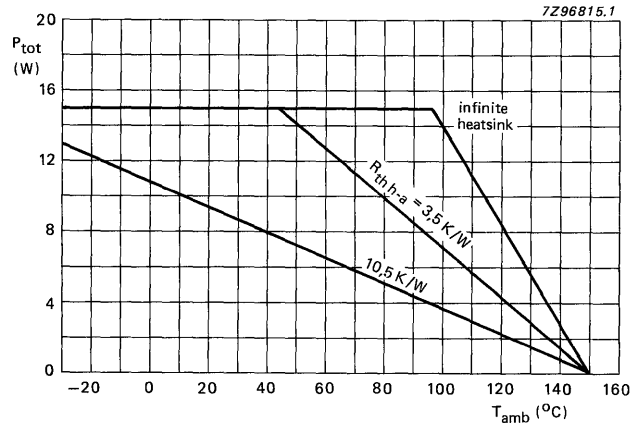
RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage:					
operating	pin 10	V_P	–	18	V
non-operating		V_P	–	28	V
non-operating, load dump protection	during 50 ms	V_P	–	45	V
Peak output current		I_{OM}	–	6	A
Total power dissipation	see Fig. 2	P_{tot}			
Storage temperature range		T_{stg}	–65	+ 150	°C
Crystal temperature		T_c	–	+ 150	°C



(a)



(b)

Fig. 2 Power derating curves; (a) TDA1510, (b) TDA1510A.

HEATSINK DESIGN EXAMPLE

The derating of the encapsulation requires the following external heatsink (for sine-wave drive):

TDA1510 ($R_{th\ j\text{-}mb}$) = 3 K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3 = 4\ K/W$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3 = 11\ K/W$$

TDA1510A ($R_{th\ j\text{-}mb}$) = 3,5 K/W

24 W BTL (4 Ω) or 2 x 12 W stereo (2 Ω); maximum sine-wave dissipation = 12 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{12} - 3{,}5 = 3{,}5\ K/W$$

2 x 7 W stereo (4 Ω); maximum sine-wave dissipation = 6 W;
T_{amb} = 65 °C (maximum):

$$R_{th\ h\text{-}a} = \frac{150 - 65}{6} - 3{,}5 = 10{,}5\ K/W$$

D.C. CHARACTERISTICS

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	6,0	14,4	18,0	V
Repetitive peak output current		I_{ORM}	–	–	4,0	A
Total quiescent current		I_{tot}	–	75	120	mA
Stand-by current		I_{sb}	–	–	2	mA
Switch-on current	$V_{11} \leqslant V_{10}$; note 1	I_{so}	0,15	0,35	0,80	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; f = 1 kHz; unless otherwise specified

parameter	parameter	symbol	min.	typ.	max.	unit
Bridge Tied Load application (BTL)						
Output power with bootstrap	note 6; R_L = 4 Ω					
	V_P = 13,2 V					
	d_{tot} = 0,5%	P_o	–	15,0	–	W
	d_{tot} = 10%	P_o	–	20,0	–	W
	V_P = 14,4 V					
	d_{tot} = 0,5%	P_o	15,5	18,0	–	W
	d_{tot} = 10%	P_o	20,0	24,0	–	W
Open loop voltage gain		G_o	–	75	–	dB
Closed loop voltage gain	note 2	G_c	39,5	40,0	40,5	dB
Frequency response	at –3 dB; note 3	f_r	–	20 to > 20 k	–	Hz
Input impedance	note 4	$\|Z_i\|$	1	–	–	MΩ
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz					
	R_S = 0 Ω	$V_{n\ (rms)}$	–	0,2	–	mV
	R_S = 10 kΩ	$V_{n\ (rms)}$	–	0,35	0,8	mV
	R_S = 10 kΩ; according to IEC 179 curve A	$V_{n\ (rms)}$	–	0,25	–	mV
Supply voltage ripple rejection	f = 100 Hz; note 5	SVRR	42	50	–	dB
D.C. output offset voltage between channels		$\|\Delta V_{5\text{-}9}\|$	–	2	50	mV
Power bandwidth	–1 dB; d_{tot} = 0,5%	B	–	30 to > 40 k	–	Hz

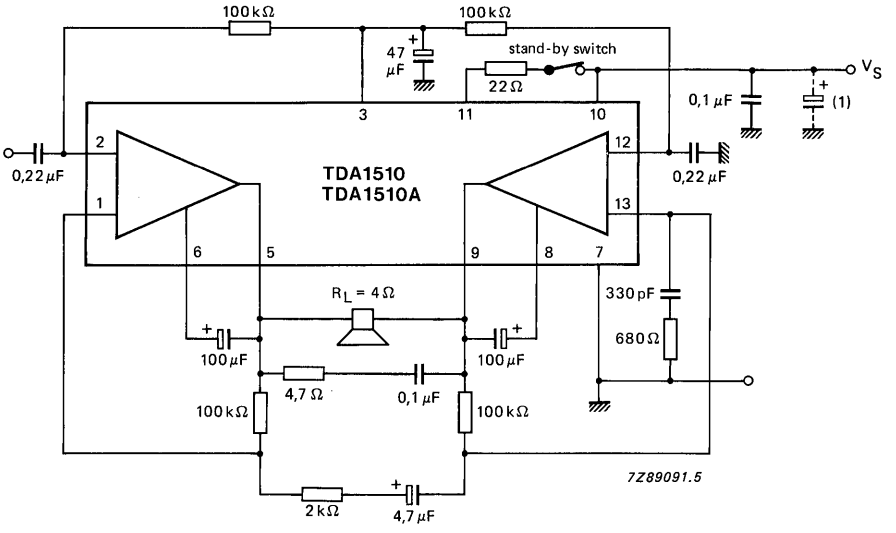
A.C. CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Stereo application						
Output power; with bootstrap	note 6; $R_L = 4\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	4,5	–	W
	$d_{tot} = 10\%$	P_o	–	6,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	4,5	5,5	–	W
	$d_{tot} = 10\%$	P_o	6,0	7,0	–	W
	$R_L = 2\ \Omega$					
	$V_P = 13{,}2$ V					
	$d_{tot} = 0{,}5\%$	P_o	–	7,5	–	W
	$d_{tot} = 10\%$	P_o	–	10,0	–	W
	$V_P = 14{,}4$ V					
	$d_{tot} = 0{,}5\%$	P_o	7,75	9,0	–	W
	$d_{tot} = 10\%$	P_o	10,0	12,0	–	W
Output power; without bootstrap	notes 6, 8 and 9 $R_L = 4\ \Omega$ $V_P = 14{,}4$ V					
	$d_{tot} = 10\%$	P_o	–	6	–	W
Frequency response	notes 3 and 6					
	−3 dB	f_r	–	40 to > 20 k	–	Hz
Supply voltage ripple rejection	note 5					
	f = 1 kHz	SVRR	–	50	–	dB
Channel separation	$R_S = 10\ k\Omega$;					
	f = 1 kHz	α	40	50	–	dB
Closed loop voltage gain	note 7	G_c	39,5	40,0	40,5	dB
Noise output voltage (r.m.s. value)	f = 20 Hz to 20 kHz;					
	$R_S = 0\ \Omega$	$V_{n(rms)}$	–	0,15	–	mV
	$R_S = 10\ k\Omega$	$V_{n(rms)}$	–	0,25	–	mV
	$R_S = 10\ k\Omega$; according to IEC179 curve A	$V_{n(rms)}$	–	0,2	–	mV

Notes to the characteristics

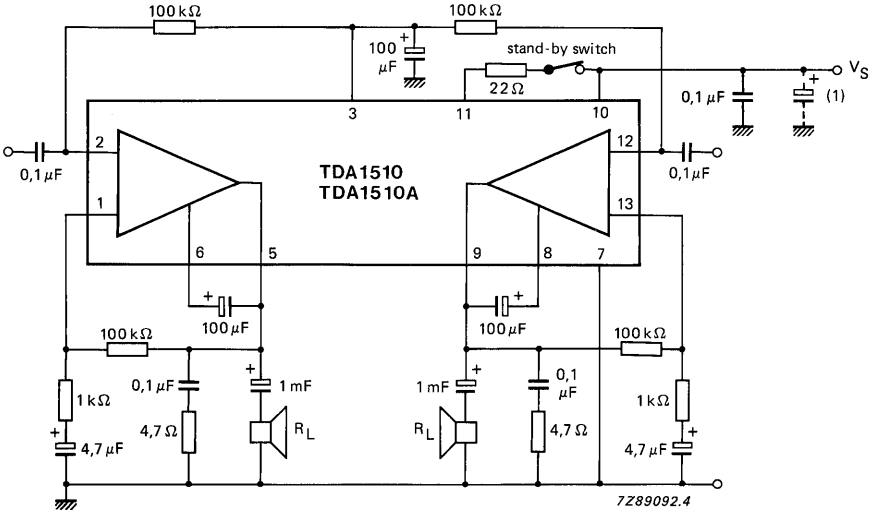
1. If $V_{11} > V_{10}$ then I_{11} must be < 10 mA.
2. Closed loop voltage gain can be chosen between 32 and 56 dB (BTL), and is determined by external components.
3. Frequency response externally fixed.
4. The input impedance in the test circuit (Fig. 3) is typ. 100 kΩ.
5. Supply voltage ripple rejection measured with a source impedance of 0 Ω (maximum ripple amplitude 2 V).
6. Output power is measured directly at the output pins of the IC.
7. Closed loop voltage gain can be chosen between 26 and 50 dB (stereo), and is determined by external components.
8. A resistor of 56 kΩ between pins 3 and 7 is required for symmetrical clipping.
9. Without bootstrap the 100 μF capacitor between pins 5 and 6 and the 100 μF capacitor between pins 8 and 9 can be omitted. Pins 6 and 8 connected to pin 10.

APPLICATION INFORMATION



(1) belongs to power supply

Fig. 3 Test and application circuit; Bridge Tied Load (BTL).



(1) belongs to power supply

Fig. 4 Test and application circuit; stereo mode.