

TC9173P/F, TC9174P/F

9097247 TOSHIBA. ELECTRONIC

02E 18222 D

○ INTERFACE IC FOR I/O PORT EXTENSION

TC9173P/F and TC9174P/F are the ICs for extending the I/O ports of digital tuning system controller LSIs, TC9301AN/02AF/03AN.

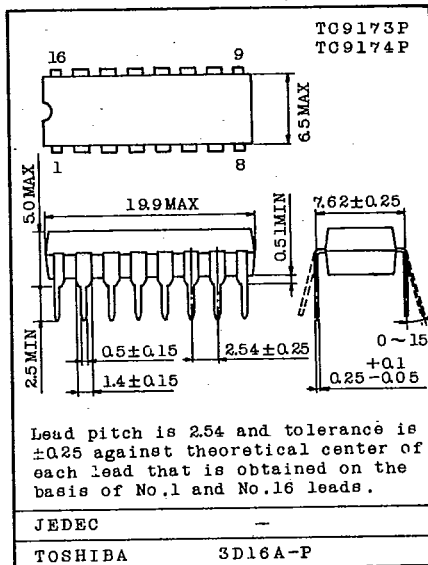
- TC9173P/F is for extension of input/output (I/O).
TC9174P/F is exclusively for extension of output.
- Both types have ten port terminals.
- TC9173P/F can set input/output by one-bit unit.
- Both types have in each port the drivers of Nch open drain structure built in, and the large current drive is possible.
(sink current 10mA Min.)
- TC9174P/F has the output ports of high breakdown voltage structure. (breakdown voltage : 18V Min.)
- TC9174P/F can take the output data into the controller by S0 terminal.
- Each port is controlled with four serial bus lines on the controller.

MAXIMUM RATINGS (Ta=25°C)

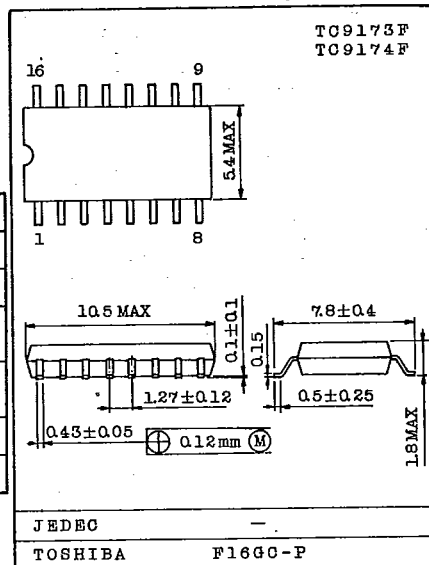
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.3~7.0	V
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Allowable Power Dissipation	P _D	600	mW
Output Voltage Resistance *	V _{OUT}	20	V
Operation Temperature	T _{opr}	-30~75	°C
Storage Temperature	T _{stg}	-55~125	°C

* Only in TC9174P/F.

Unit in mm



Unit in mm



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TC9173P/F

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	*	4.5	5.0	5.5	V
Operating Supply Current	I_{DD}	at no load	-	-	1.0	mA

(I/O PORT)

Input Voltage	"H" Level	V_{IH}		$V_{DD} \times 0.7$	-	V_{DD}	V
	"L" Level	V_{IL}		0	-	$V_{DD} \times 0.3$	
Input Current	"H" Level	I_{IH}	$V_{IH}=5.0\text{V}$	-	-	1.0	μA
	"L" Level	I_{IL}	$V_{IL}=0.0\text{V}$	-	-	-1.0	

(SO)

Output Current	"H" Level	I_{OH1}	$V_{OH}=4.0\text{V}$	-1.0	-2.0	-	mA
Output Off-leak Current		I_{OFF1}	$V_{OUT}=0.0\text{V}$	-	-	-1.0	μA

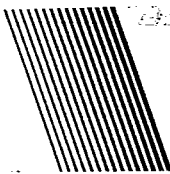
(I/O PORT)

Output Current	"L" Level	I_{OL2}	$V_{OL}=1.0\text{V}$	10	-	-	mA
Output Off-leak Current		I_{OFF2}	$V_{OH}=5.0\text{V}$	-	-	1.0	μA

(SI·CK·STB)

Threshold Value Voltage	"H" Level	V_D		-	3.0	-	V	
	"L" Level	V_N		-	2.0	-		
Hysteresis		V_H		-	1.0	-	V	
Operating Frequency Range		f_{CK}	SI, SO, CK, STB	*	300	500	-	kHz

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TC9174P/F

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage	V_{DD}	*	4.5	5.0	5.5	V
Operating Supply Current	I_{DD}	at no load	-	-	1.0	mA

(S0)

Output Current	"H" Level	I_{OH}	$V_{OH}=4.0\text{V}$	-1.0	-2.0	-	mA
Output Off-leak Current		I_{OFF1}	$V_{OUT}=0.0\text{V}$	-	-	-1.0	μA

(OUT PORT)

Output Current	"L" Level	I_{OL}	$V_{OL}=1.0\text{V}$	10	-	-	mA
Output Off-leak Current		I_{OFF2}	$V_{OH}=18\text{V}$	-	-	1.0	μA

(SI·CK·STB)

Threshold Value Voltage	"H" Level	V_D		-	3.0	-	V	
	"L" Level	V_N		-	2.0	-		
Hysteresis Voltage		V_H		-	1.0	-	V	
Operating Frequency Range		f _{CK}	SI, S0, CK, STB	*	300	500	-	kHz

Note : * The marked, $V_{DD}=4.5\sim 5.5\text{V}$, $T_a=-30\sim 75^\circ\text{C}$ range guaranteed.

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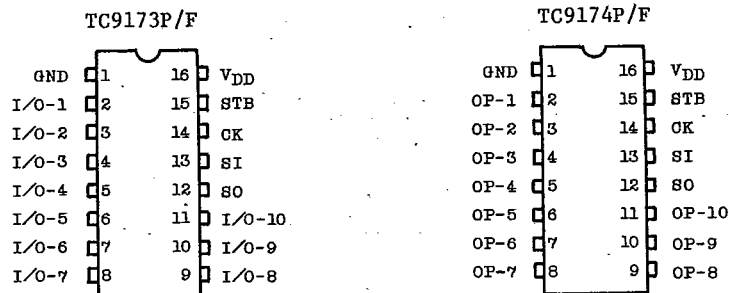
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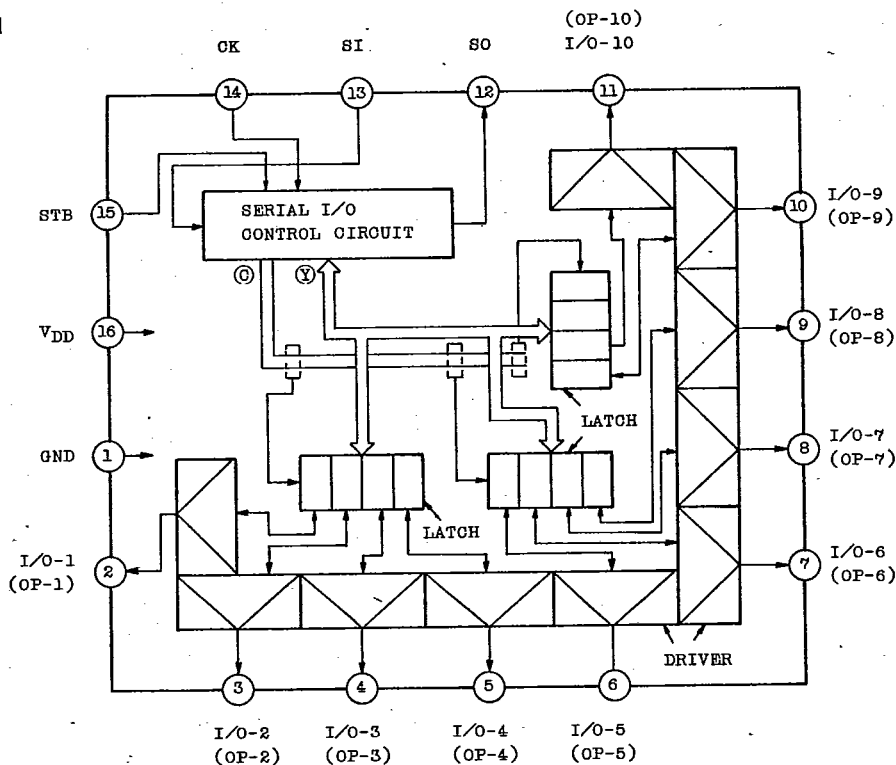
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PIN CONFIGURATION



BLOCK DIAGRAM



Note : The name in () is the terminal name for TC9174P/F.

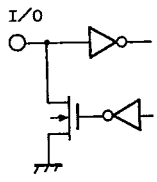
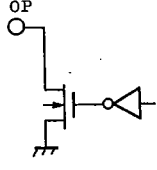
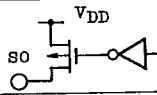
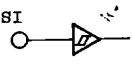
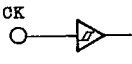
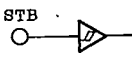
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FUNCTION OF EACH TERMINAL

PIN No.	SYMBOL	NAME OF TERMINAL	FUNCTION-OPERATION	REMARKS			
2	I/O-1	TC9173P/F: General purpose I/O port	TC9173P/F: General purpose I/O port I/O can be set by 1-bit unit with program. . For input, CMOS input. . For output, Nch open drain output. (Large current driving sink current 10mA MIN.)				
	OP-1						
3	I/O-2						
	OP-2						
4	I/O-3						
	OP-3						
5	I/O-4						
	OP-4						
6	I/O-5				TC9174P/F: General purpose	TC9174P/F: General purpose output port High breakdown voltage Nch open drain output for large current driving. Drain output. (Sink current 10mA MIN.) (Breakdown voltage 18V MIN.)	
	OP-5						
7	I/O-6	output port					
	OP-6	OP-1~10					
8	I/O-7						
	OP-7						
9	I/O-8						
	OP-8						
10	I/O-9						
	OP-9						
11	I/O-10						
	OP-10						
12	SO	Serial data output	Data output port of serial I/O port, and Pch open drain output.				
13	SI	Serial data input	Data input port of serial I/O port, and Schmidt input.				
14	CK	Clock signal input	Clock signal input port of serial I/O port and Schmidt input.				
15	STB	Strobe signal input	Strobe signal input port of serial I/O port and Schmidt input.				
16	VDD	Power supply terminal	Applies 5V±10%				
1	GND						

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OPERATION

○ SERIAL BUS I/O

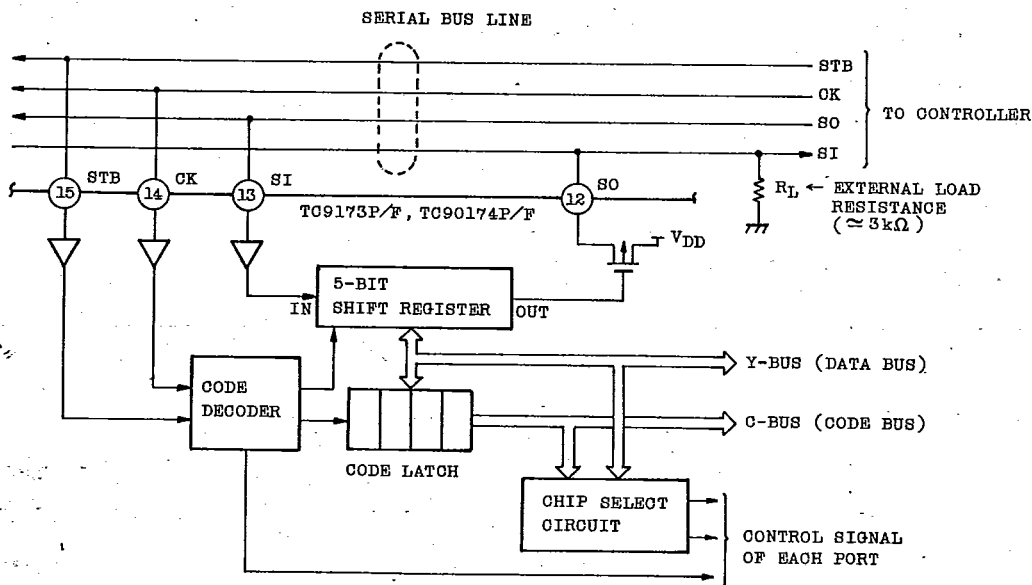
Every port is controlled by the controller through four serial bus lines (SI, SO, CK, STB).

(Note) As controlling the IC connected to the serial bus line by the controller, it is necessary to select the IC to be controlled with the chip-select code. The chip select code is the code for selecting the IC to be controlled among the ICs connected by the serial bus line from the controller.

Chip select code using TC9173P/F: "3"

Chip select code using TC9174P/F: "4"

The terminals of SI, CK and STB involve Schmidt input circuits. Since SO terminal is Pch open drain output, the external load resistance is required.



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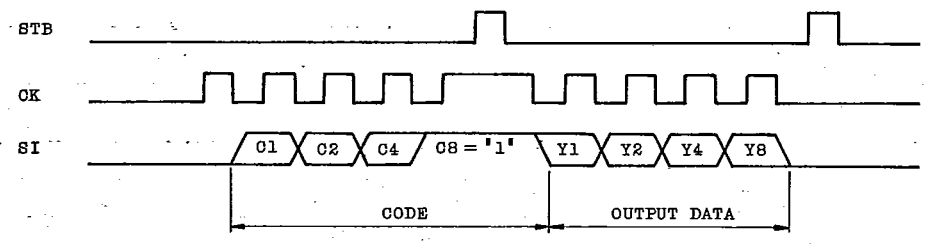
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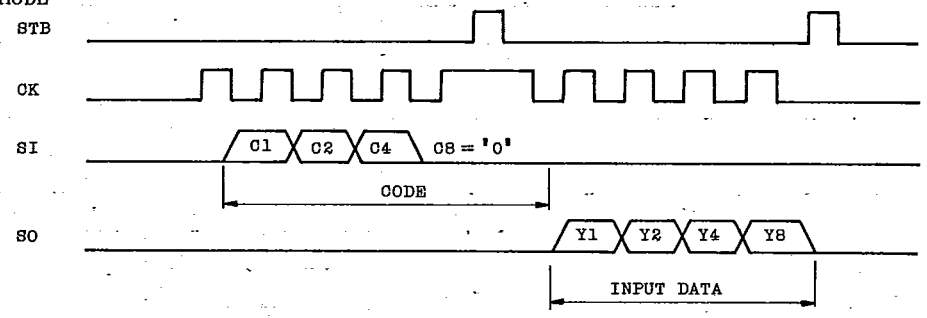
The timing chart of the serial bus line is shown in the figure below.

OUTPUT MODE

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INPUT MODE



○ DESIGNATION OF INPUT/OUTPUT MODE

The designation of input/output mode is performed by SI signal. SI signal is 8-bit structure, and the high-order four bits are for the code designation and the lower-order four bits are for the data.

1. Output Mode

The output mode is designated when the fourth bit (C8) of the code portion (high-order four bits) of the SI signal is "1". Each port is selected by the three bits (C1, C2, C4) of the code portion, and the data Y1, Y2, or Y3 is set to each selected port.

2. Input Mode

The input mode is designated when the fourth bit (C8) of code portion (high-order four bits) of the SI signal is "0". Each port is selected by the three bits (C1, C2, C4) of the code portion, and the selected port data of 4-bit serial is output at SO terminal.

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The code allotment of each port is shown in the table below.

I/O MAP

PRODUCT NAME		TC9173P/F				TC9174P/F			
DATA	Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8	
INPUT MODE	0								
	1	I/O-1	I/O-2	I/O-3	I/O-4	OP-1	OP-2	OP-3	OP-4
	2	I/O-5	I/O-6	I/O-7	I/O-8	OP-5	OP-6	OP-7	OP-8
	3	I/O-9	I/O-10			OP-9	OP-10		
	4								
	5								
	6								
	7								
OUTPUT MODE	8								
	9	I/O-1	I/O-2	I/O-3	I/O-4	OP-1	OP-2	OP-3	OP-4
	A	I/O-5	I/O-6	I/O-7	I/O-8	OP-5	OP-6	OP-7	OP-8
	B	I/O-9	I/O-10			OP-9	OP-10		
	C								
	D								
	E	Test *				Test *			
		1	2			1	2		
F	Designates chip select "3".				Designates chip select "4".				

* Test

1	2	Mode
0		Normal operation
1	0	Outputs are all in OFF state
1	1	Outputs are all in ON state

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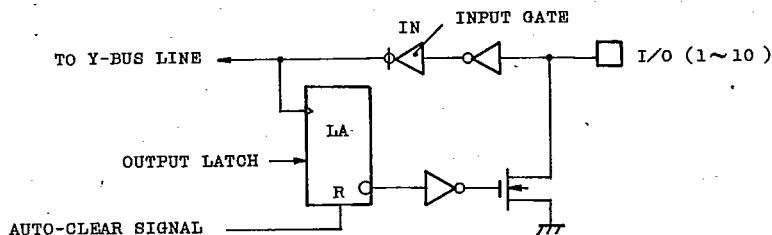
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○ TC9173P/F GENERAL PURPOSE I/O PORT

1. Ten general I/O ports (I/O-1 ~ I/O-10) are available.
2. The control data of I/O port is set by 4-bit unit, however, the input and the output can be set by 1-bit unit.
3. At using each port for output, Nch open drain output is made, and the current driving (sink current 10mA Min.) becomes possible.
4. At using each port for input, C-MOS input is mode. Pull up and Pull down resistor is not involved.
5. At "POWER SUPPLY ON", all the ports are designated for input by the auto-clear operation.
6. The circuit structure of each port (for 1 bit) is as shown in below the figure.



7. Usage as output port

In the output mode (codes "9"~"B"), through setting the data "1", "0" to each port, the output state of the port becomes as shown in the table below.

DATA	OUTPUT STATE
"1"	"0" level (Nch FET is ON state)
"0"	Floating (Nch FET is OFF state)

8. Usage as input port

Set data "0" to the terminal required to be used as the input port in the output mode (code "9"~"B").

In the port set with the data "0", the output driver turns into OFF state, and the input data becomes possible to take in with input mode. (Positive logic input).

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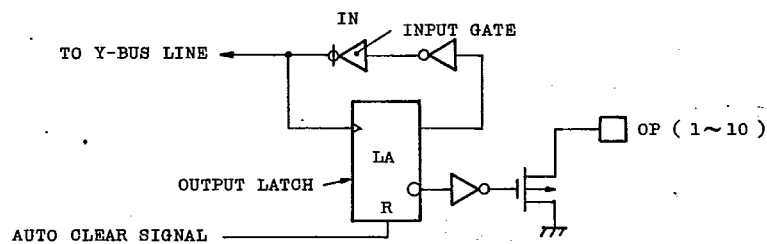
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○ TC9174P/F GENERAL PURPOSE OUTPUT PORT

1. Ten general purpose output ports are available. (OP-1~OP-10)
2. Input mode is available and the data set by (OP-1~OP-10) can be taken again in the controller side.
3. The control data of each port is made by 4-bit unit.
4. Every ports involves the high breakdown voltage driver of Nch open drain structure for the current driver. (breakdown voltage 18V Min. sink current 10mA Min.)
5. At the power supply ON, all the ports are set to the floating state (driver OFF) by the auto-clear operation.
6. The circuit structure (for 1 bit) of each port is as shown in the figure below.



7. By means of setting the data "0" or "1" in the output mode (codes "9"~"B"), the output state becomes as shown in the table below.

DATA	OUTPUT STATE
"1"	"0" level (Nch FET is ON state)
"0"	Floating (Nch FET is OFF state)

○ TEST MODE

The test modes for the function evaluation are available. The test mode is controlled by the "TEST" code.

CODE	Y1	Y2	MODE
E	0	*	Normal operation (test mode clear)
E	1	0	2~11 pin floating (driver OFF state)
E	1	1	2~11 pin "0" level, 12 pin "1" level state

Note 1 : * mark : Don't care

Note 2 : Be sure to clear the "TEST" code with program.

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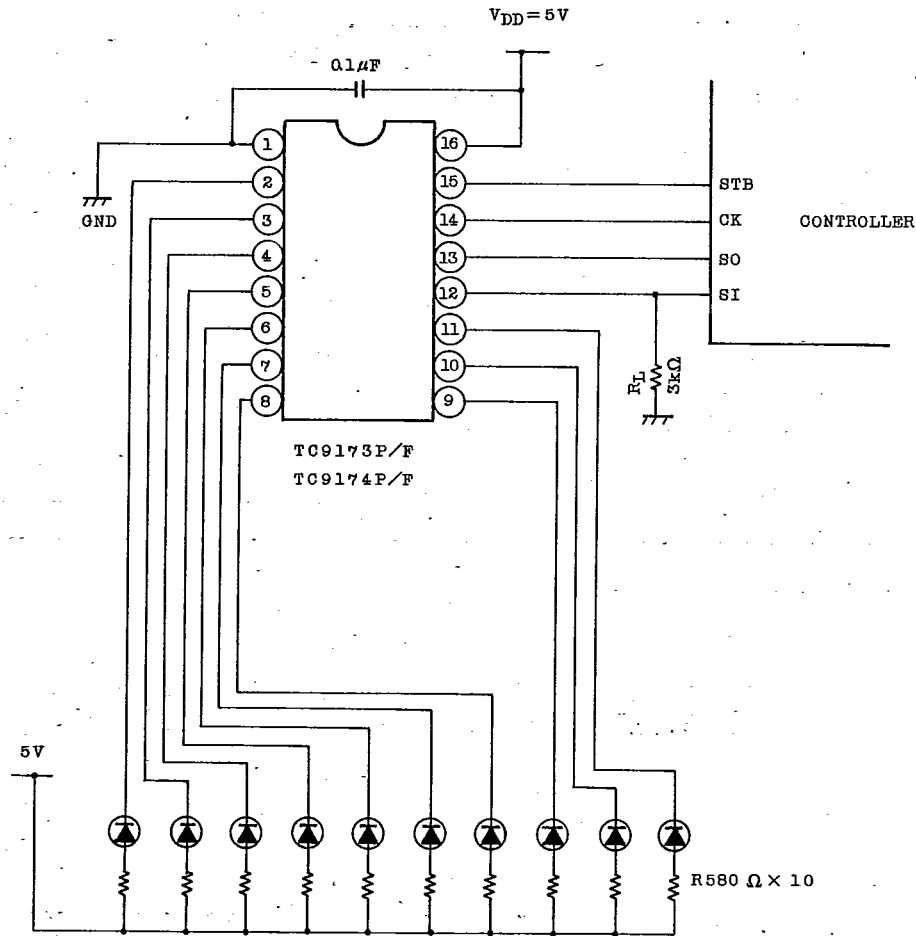
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EXAMPLE OF APPLICATION CIRCUIT



LED INDICATION CIRCUIT

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