SN4932N / SN49832N
DUAL 8-BIT SHIFT REGISTER

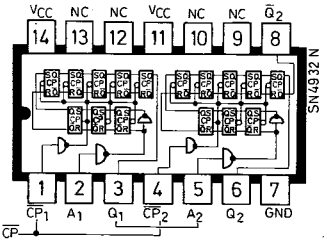
A SERIES 74N TTL SPECIAL SHIFT REGISTER FOR APPLICATION IN

logic

TRUTH TABLE

t_n	$t_n + 16$
A_1	Q_2 $\overline{Q}_2$
0	0 1
1	1 0

NOTES: 1. t_n = bit time before clock pulse
2. $t_n + 16$ = bit time after 16 clock pulses.



description

The SN4932N is a monolithic serial-in, serial-out, dual 8-bit shift register utilizing transistor-transistor logic (TTL) circuits in the familiar high-speed Series 74 configuration. The shift register, composed of 16 R-S master-slave flip-flops, including a clock driver. The register is capable of storing and transferring data at clock rates up to 15 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 360 milliwatts, an full fan-out of 10 is available from the outputs Q_2 and $\overline{Q}_2$.

An internal inverter forms the complementary input to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A_1, A_2 and $\overline{CP}$) appear as only 1 TTL input load.

The clock pulse inverter/driver causes the SN4932N to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift register to be fully compatible with the SN7470N-K flip-flop and the SN7474N dual D-type flip-flop.

The SN4932N ist normally used as a 16-bit shift register by externally connecting output Q_1 to input A_2 and applying a common clock $\overline{CP}$ to inputs $\overline{CP}_1$ and $\overline{CP}_2$. The two 8-bit shift registers may also be used separately with a fan-out of 5 from output Q_1 and a fan-out of 10 from outputs Q_2 and $\overline{Q}_2$.

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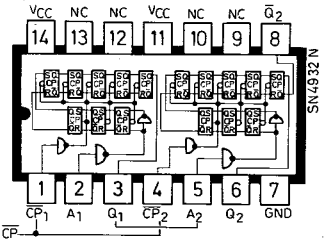

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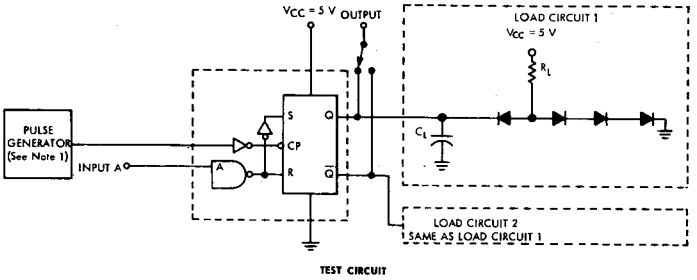
PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT

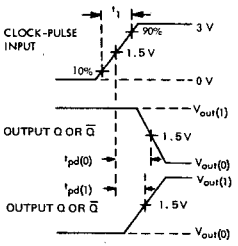


FIGURE 1
PROPAGATION DELAY TIME VOLTAGE WAVEFORM

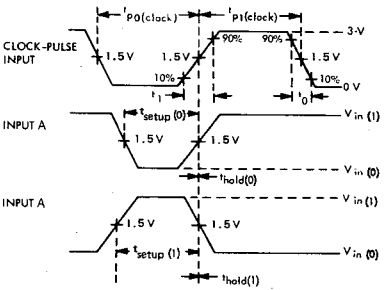


FIGURE 2
SWITCHING TIME VOLTAGE WAVEFORM

NOTES: 1. The generator has the following characteristics: $V_{in(0)} \leq 0{,}3$ V, $V_{in(1)} \geq 2{,}4$ V, $t_{r1} = t_{f0} = 10$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$
2. C_L includes probe and jig capacitance
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. All diodes are 1N3064.

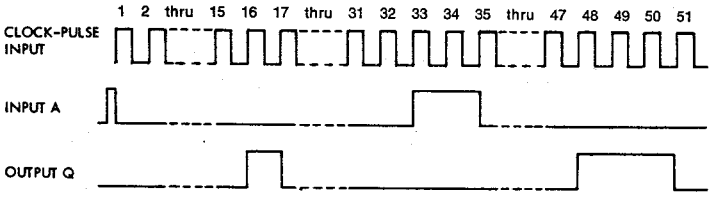
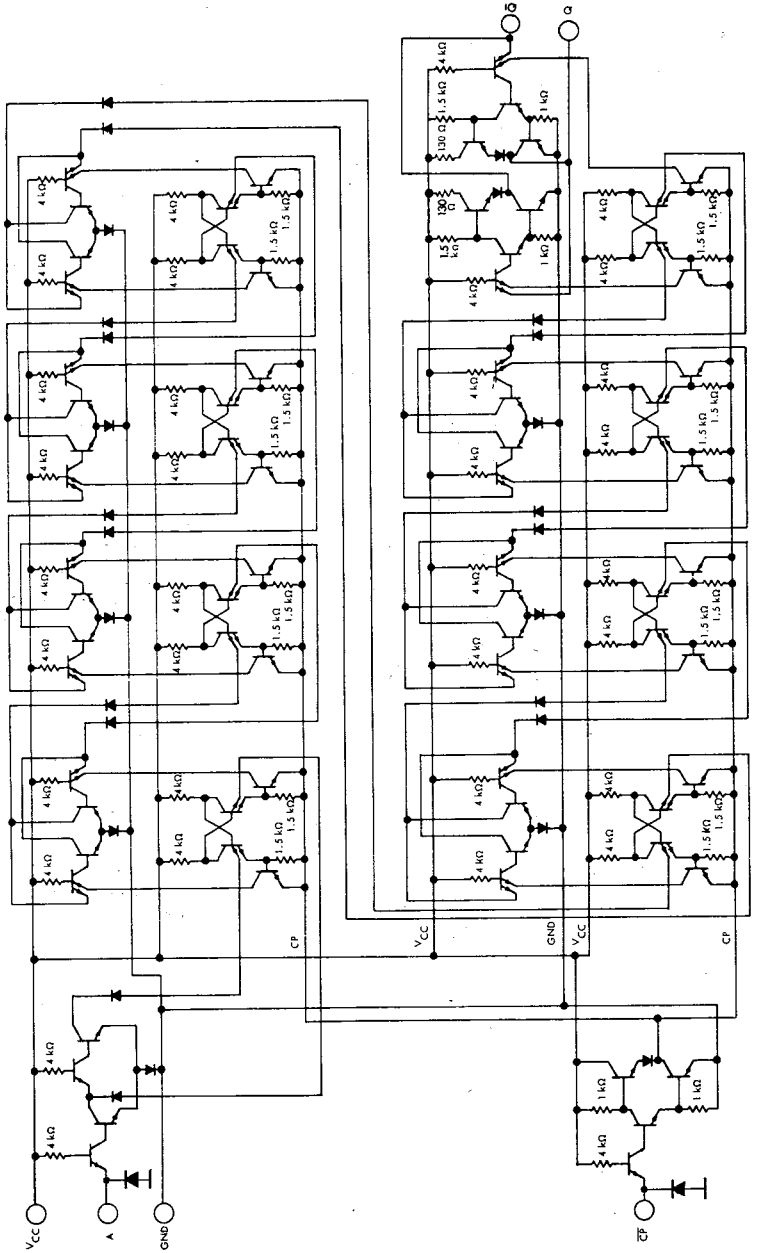


FIGURE 3
TYPICAL INPUT/OUTPUT WAVEFORMS FOR 16-BIT OPERATION

10

schematic (each shift register)



Component values shown are nominal.

* $\overline{Q}$ only available on shift-register Nr. 2