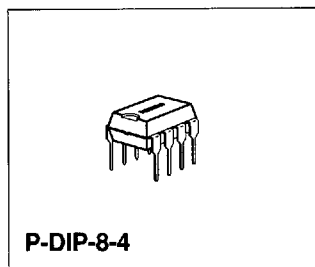


Nonvolatile Memory 8-Kbit E²PROM with I²C Bus Interface

SDA 2586
MOS IC

Features

- Word-organized, reprogrammable nonvolatile memory in n-channel floating-gate technology (E²PROM)
- 1024 × 8-bit organization
- Supply voltage 5 V
- Serial 2-line bus for data input and output (I²C Bus)
- Reprogramming mode, 10 ms erase / write cycle
- Reprogramming by means of on-chip control (without external control)
- The end of the programming cycle can be checked
- Data retention in excess of 10 years
- More than 10⁵ reprogramming cycles per address



Type	Ordering Code	Package	Pin Configuration
SDA 2586-5	Q67100-H5101	P-DIP-8-4	SIEMENS
SDA 25X86-5	Q67100-H3260	P-DIP-8-4	STANDARD

Circuit Description

I²C Bus Interface

The I²C Bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a data line SDA and a clock line SCL. The data line require an external pull-up resistor to V_{CC} (open drain output stages).

The possible operational states of the I²C Bus are shown in **figure 1**. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer, the information on the data bus will only change when the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C Bus system, the device can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, the information is always transmitted in byte-organized form. Between the falling edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the device sets the SDA-line to low as a reception confirmation, if the chip select conditions have been met. During the output of data, the data output of the memory becomes high in impedance during the ninth clock pulse (acknowledge master).

The signal timing required for the operation of the I²C Bus is summarized in **figure 2**.

Control Functions of the I²C Bus

The device is controlled by the controller (master) via the I²C Bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes to the bus after the start condition. Each byte has to be followed by an acknowledge bit. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming instance, the active programming process is only started by the stop condition after data input, **see figure 3**.

The chip select word includes the chip select bit CS. Thus it is possible to parallel two memory devices. Chip select is obtained when the control bits logically correspond to the condition selected at the select input CS. The two most significant bits A8 and A9 are inputs with the chip select words CS/E.

Checking the End of the Programming Cycle and Breaking off the Programming Cycle

Addressing the chip by the input of CS/E during active reprogramming terminates the programming cycle. If the chip is addressed by entering CS/A, this will be ignored. Only when the programming cycle has terminated will the chip react on CS/A. With this procedure the end of the programming cycle can be checked, **see figure 3**.

Memory Read

After the input of the two control words CS/E and WA, the resetting of the start condition and the input of a third control word CS/A, the memory is set ready to read. During acknowledge clock No. 9, the memory information is transferred in parallel to the internal data register. Subsequent to the falling edge of the acknowledge clock the data output is low-impedance and the first data bit can be sampled, **see figure 4**. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 1024, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into "1" state. During the write process, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and the last clock of the control word input, the active programming process is started by the stop condition. The active programming process is executed under on-chip control and can be terminated by addressing the device via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process is max. 20 ms, or typically, 10 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-On and Chip Reset

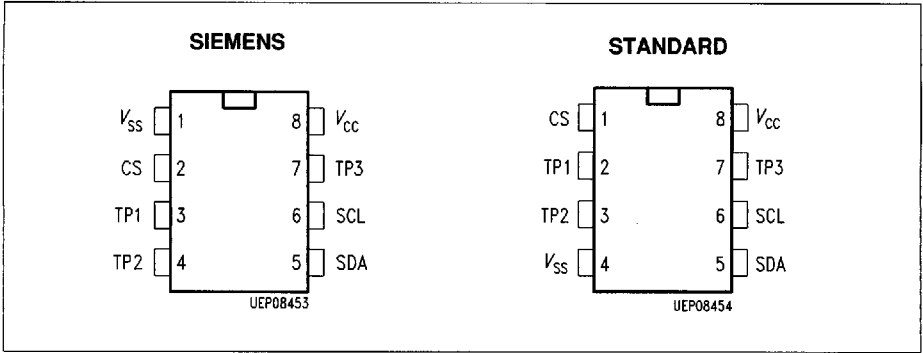
After the supply voltage V_{CC} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to the data output and to the stop condition, the internal control logic is reset. In the case of a subsequent active programming operation, however, the stop condition will not reset the control logic.

Chip Erase

To erase the entire memory the control word CS/E is entered, the address register is loaded with address 0 and the data register with FF (hex), respectively. Immediately prior to generating the stop condition, the input TP2 is connected from 0 to 5 V. The subsequent stop condition initiates the chip erase. As soon as the erase procedure has terminated, TP2 is again connected to 0 V.

■ 8235605 0088990 327 ■

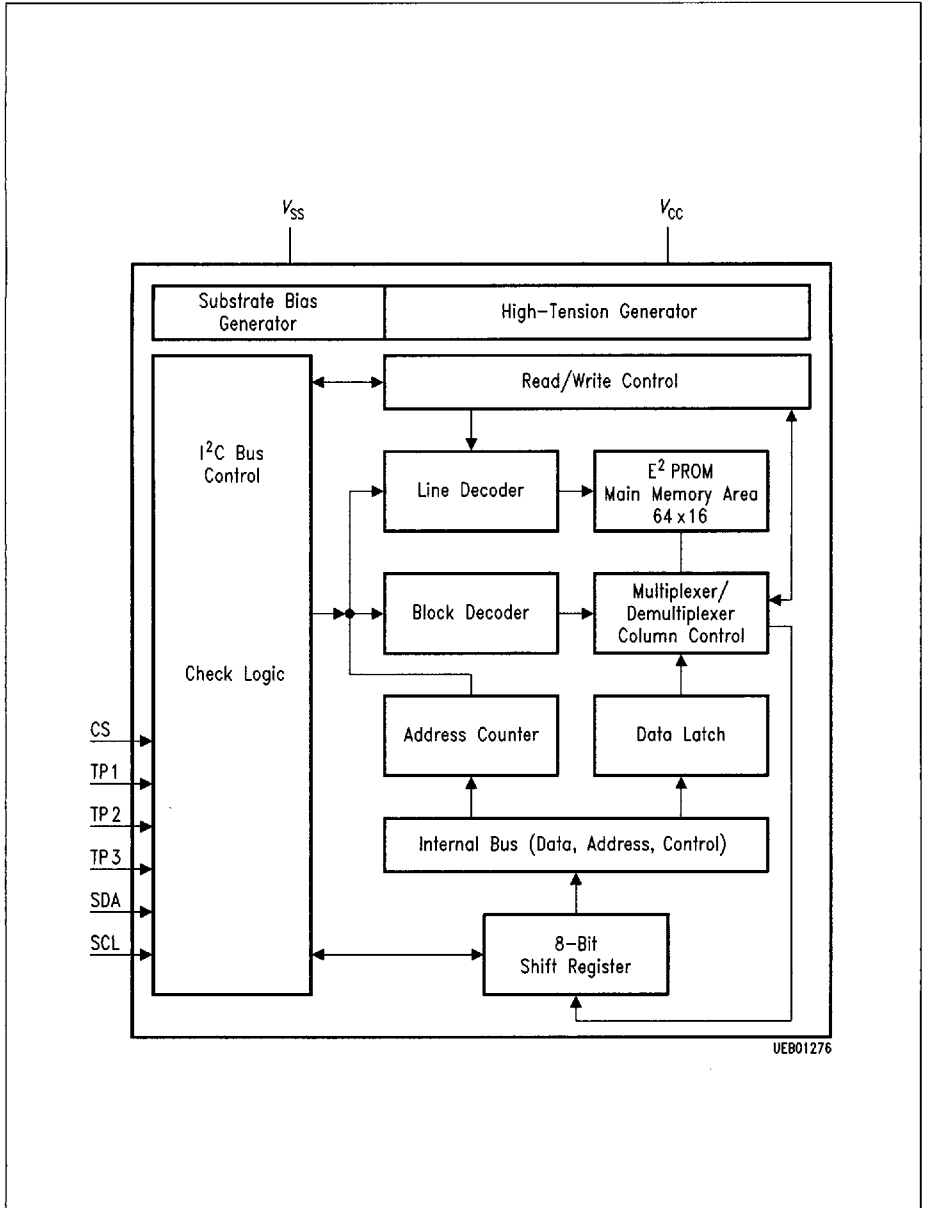
Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.		Symbol	Function
SIEMENS	STANDARD		
1	4	V _{SS}	Ground
2	1	CS	Chip select
3	2	TP1	to V _{SS}
4	3	TP2	0 V normal function, TP2 = 5 V condition to erase of the entire memory
5	5	SDA	Data line
6	6	SCL	Clock line
7	7	TP3	open
8	8	V _{CC}	Supply voltage

■ 8235605 0088991 263 ■



Block Diagram

■ 8235605 0088992 1TT ■

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{CC}	- 0.3	6	V
Input voltage	V_I	- 0.3	6	V
Power dissipation	P_D		130	mW
Storage temperature	T_{stg}	- 40	125	°C
Thermal resistance (system-air)	$R_{th SA}$		100	K/W
Junction temperature	T_j		85	°C

Operating Range

Supply voltage	V_{CC}	4.75	5.25	V
Ambient temperature	T_A	0	70	°C

Characteristics $T_A = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.75	5.0	5.25	V	
Supply current	I_{CC}			20	mA	$V_{CC} = 5.25\text{ V}$

Inputs

Input voltage SDA/SCL	V_{IL}			1.5	V	
Input voltage SDA/SCL	V_{IH}	3.0		V_{CC}	V	
Input current SDA/SCL	I_{IH}			10	μA	$V_{IH} = V_{CC}$

Outputs

Output current SDA	I_{QL}			3.0	mA	$V_{QL} = 0.4\text{ V}$
Leakage current SDA	I_{QH}			10	μA	$V_{QH} = V_{CC\text{ max}}$

Inputs

Input voltages CS/TP1/TP2	V_{IL}			0.2	V	
Input voltages CS/TP1/TP2	V_{IH}	4.5		V_{CC}	V	
Input currents CS/TP1/TP2	I_{IH}			100	μA	$V_{CC} = 5.25\text{ V}$
Clock frequency	f_{SCL}			100	kHz	
Reprogramming duration	t_{PROG}		10	20	ms	erase and write
Input capacity	C_1			10	pF	
Total erase	t_{GL}			20	ms	TP2 = 5 V

Diagrams

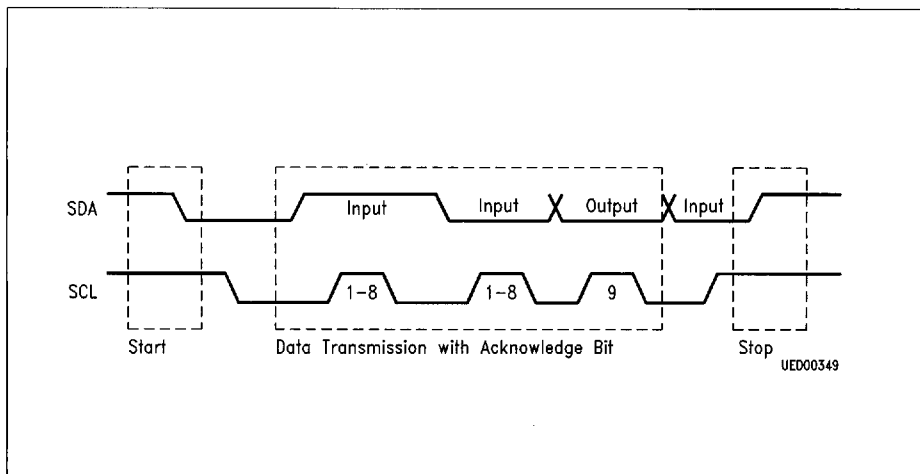


Figure 1
Operational States of the I²C Bus

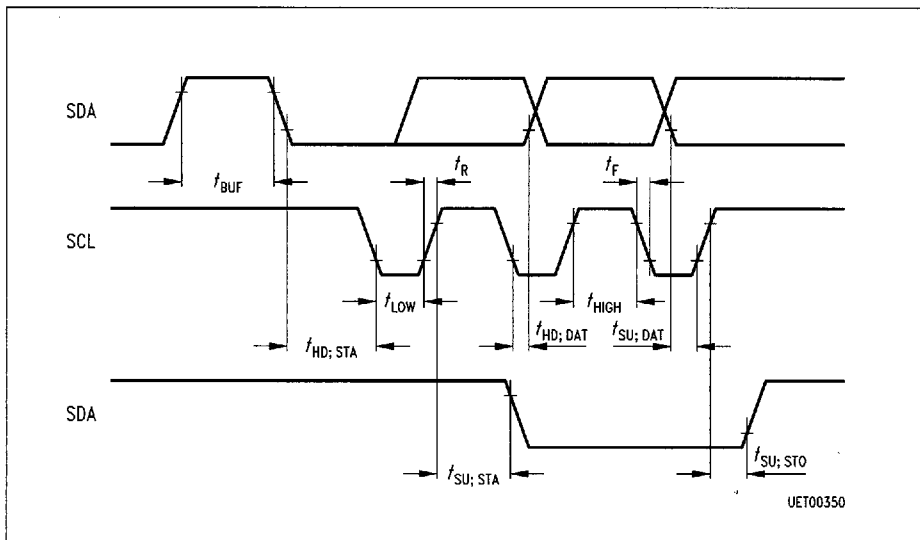


Figure 2
Time Conditions for the I²C Bus (high-speed mode)

Timing Conditions

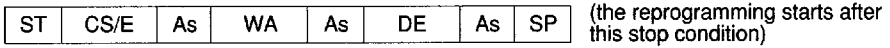
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Minimum time the bus must be free before a new transmission can start	t_{BUF}	4.7		μs
Start condition hold time	$t_{\text{HD;STA}}$	4.0		μs
Clock low period	t_{LOW}	4.7		μs
Clock high period	t_{HIGH}	4.0		μs
Start condition set-up time, only valid for repeated start code	$t_{\text{SU;STA}}$	4.7		μs
Data set-up time	$t_{\text{SU;DAT}}$	250		ns
Rise time of both the SDA and SCL line	t_{R}		1	μs
Fall time of both the SDA and SCL line	t_{F}		300	μs
Stop condition set-up time	$t_{\text{SU;SPO}}$	4.7		μs

Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL. All values refer to V_{IH} and V_{IL} level.

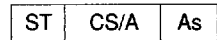
Figure 3

Programming

Control word input



Check for program end by



1. when As = 1 programming is not finished
2. when As = 0 programming is finished

Programm interruption by

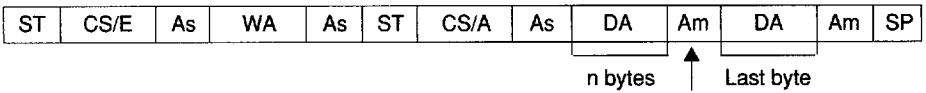


Figure 4

Read

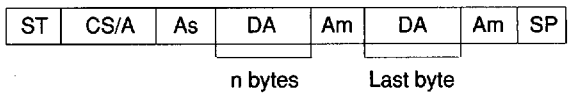
Control word input read

a) complete (with word address input)



Automatic incrementation
of the word address

b) shortened:
Bit 0 ... 9 the last adapted word
address keep unchanged



Autoincrement
before stop condition

Am = 0
Am = 1

Control Word Table

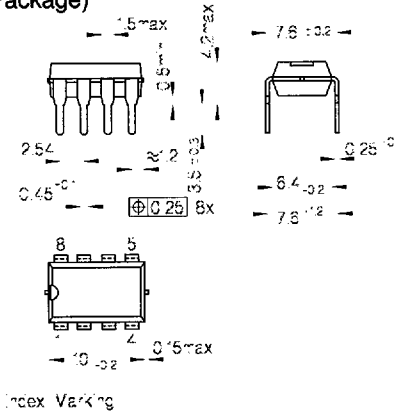
Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	A9	A8	CS	0	0	through memory
CS/A	1	0	1	0	–	–	CS	1	0	through memory
WA	A7	A6	A5	A4	A3	A2	A1	A0	0	through memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	through memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0/1	through master

Control Word Input Key

CS/E	Chip select for data input into memory (with word-address bit A8 and A9)
CS/A	Chip select for data output out of memory
WA	Memory word address
DE	Data word for memory
DA	Data word read out for memory
D0 to D7	Data bits
ST	Start condition
SP	Stop condition
As	Acknowledge bit from memory
Am	Acknowledge bit from master
CS	Chip select bits
A0 to A9	Memory word address bits

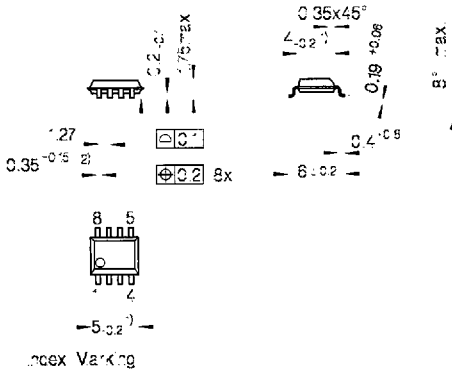
3 Package Outlines

P-DIP-8-4
(Plastic Dual In-line Package)



GPD05025

P-DSO-8-1
(Plastic Dual Small Outline Package)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion of 0.05 max. per side

GPS05121

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

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Siemens AG Österreich
Erdberger Lände 26
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☎ (01) 71711-56 11
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AUS

Siemens Ltd., Head Office
544 Church Street
Richmond (Melbourne), Vic. 3121
☎ (03) 420 71 11
☎ 30 425
Fax (03) 4 20 72 75

B

Siemens Electronic Components
Benelux
Charleroisesteenweg 116/
Chaussée de Charleroi 116
B-1060 Brussel/Bruxelles
☎ (+32) 2-536 23 48
Fax (+32) 2-536 28 57

BR

ICOTRON S.A.
Indústria de Componentes
Eletrônicos
Avenida Mutinga, 3650-6º andar
05150 São Paulo-SP
☎ (011) 8 33-22 11
☎ 11-81 001
Fax (011) 8 31-40 06

CDN

Siemens Electric Ltd.
Electronic Components Division
1180 Courtney Park Drive
Mississauga, Ontario L5T 1P2
☎ (416) 5 64 19 95
☎ (069) 68 841
Fax (416) 6 70-65 63

CH

Siemens-Albis AG
Freilagerstraße 28
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☎ 823 781-23
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D

Siemens AG
Salzufer 6-8
10587 Berlin
☎ (030) 39 93-26 26
Fax (030) 39 93-24 90

Siemens AG
Lahnweg 10
40219 Düsseldorf
☎ (0211) 3 99-29 30
Fax (0211) 3 99-14 81

Siemens AG
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Fax (040) 28 89-30 96

Siemens AG
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Siemens S.A.
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Fax (01) 8 03 39 26

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☎ 234 077
Fax (1) 49 22 39 70

GB

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Fax (0344) 39 66 32

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☎ 216 292
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HK

Siemens Components Ltd
23/F., Tai Yau Building
181 Johnston Road, Wanchai
Hong Kong
☎ (852) 28 32 05 00
Fax (852) 28 27 84 21

I

Siemens S.p.A.
Semiconductor Sales
Via dei Valtorta, 48
20127 Milano
☎ (02) 6676-1
Fax (02) 6676-4395

IND

Siemens Ltd.
Head Office
134-A, Dr. Annie Besant Road,
Worli
P.O.B. 6597
Bombay 400018
☎ (022) 4938786
☎ 1175142
Fax (022) 4940240

IRL

Siemens Ltd.
Electronic Components Division
8 Raglan Road
Dublin 4
☎ (01) 6684727
☎ 93744
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J

Fuji Electronic Components Ltd
Shinjuku Koyama Bldg. 2F
30-3, 4-Chome
Yoyogi, Shibuya-ku
Tokyo 151
☎ (81) 3-53888525
Fax (81) 3-33769792

N

Siemens A/S
Østre Aker vei 90
Postboks 10, Veitvet
0518 Oslo 5
☎ (02) 633000
☎ 78477
Fax (02) 633805

NL

Siemens Electronic Components
Benelux
Postbus 16068
NL-2500 BB Den Haag
☎ (+31) 70-3332429
Fax (+31) 70-3332815

P

Siemens S.A.
Estrada Nacional 117, Km 2,6
Aifragide
2700 Amadora
☎ (01) 4170011
☎ 62955
Fax (01) 4172870

PL

Siemens Sp. z.o.o.
ul. Stawki 2
POB 276
00-950 Warszawa
☎ 6351619
☎ 825554
Fax 6355238

RC

Tai Engineering Co., Ltd.
6th Fl., Central Building
108, Chung Shan North Road, Sec. 2
P.O. Box 68-1882
Taipei 10449
☎ (02) 5234700
☎ 27860 taiengco
Fax (02) 5367070

ROK

Siemens Ltd.
Asia Tower Bldg, 10th floor
726 Yeoksam-dong, Kangnam-ku
CPO Box 3001, Seoul 135-080
Korea
☎ (822) 527-7740
Fax (822) 527-7779

RUS

Siemens AG
1. Donskoj pr., 2
Moskva 117419
☎ (095) 237-6476, -6911
☎ 414385
Fax (095) 237-6614

S

Siemens Components
Österögatan 1
Box 46
S-164 93 Kista
☎ (08) 7033500
☎ 11672
Fax (08) 7033501

SF

Siemens Oy
P.O.B. 60
02601 Espoo
☎ (0) 51051, ☎ 124465
Fax (0) 51052398

SGP

Siemens Components Pte. Ltd.
166 Kallang Way
Singapore 1334
☎ (65) 8400600
Fax (65) 7421080

TR

SIMKO Ticaret ve Sanayi A.S.
Meclisi Mebusan Cad. No. 125
P.K. 1001, 80007 Karaköy
80040 Findikli
☎ (01) 2510900
☎ 24233 sies tr
Fax (01) 2524134

USA

Siemens Components, Inc.
Integrated Circuit Division
10950 North Tantau Avenue
Cupertino, CA 95014
☎ (408) 777-4500
Fax (408) 777-4977

ZA

Siemens Ltd.
Siemens House,
P.O.B. 4583
Johannesburg 2000
☎ (011) 3151950
☎ 450091
Fax (011) 3151968