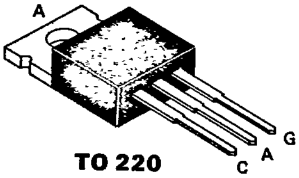
S1210BH – S1210NH SCR'S

12 A 200–800 V 10–25 mA

The S1210 series silicon controlled rectifiers are high performance glass passivated PNPN devices. These parts are intended for general purpose high current applications where moderate gate insensitivity is required.



TO 220

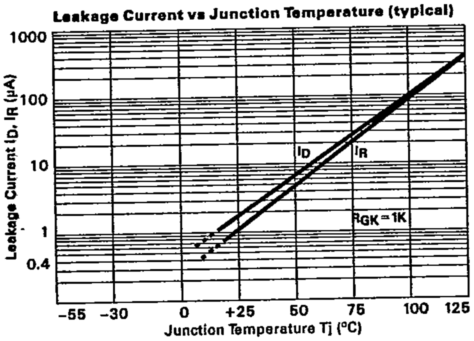
Absolute Maximum Ratings $T_A = 25\,°C$ unless otherwise noted

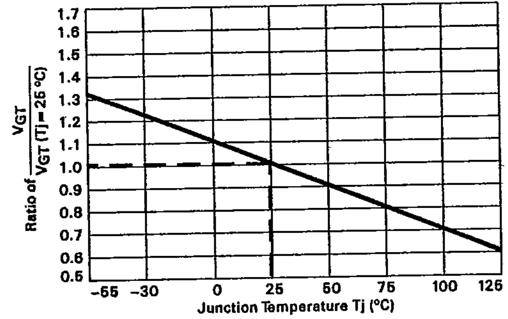
Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	**S1210BH**		200		V	
	S1210DH	$\begin{bmatrix} V_{DRM} \\ V_{RRM} \end{bmatrix}$	400		V	$\begin{bmatrix} T_j = -40\,°C \text{ to } 125\,°C \\ R_{GK} = 1\,K\Omega \end{bmatrix}$
	S1210MH		600		V	
	S1210NH		800		V	
On-State Current		$I_{T(RMS)}$	12		A	All Conduction Angles $T_C = 85\,°C$
Average On-State Current		$I_{T(AV)}$	7.6		A	Half Cycle, $\Theta = 180°$, $T_C = 85\,°C$
Nonrept. On-State Current		I_{TSM}	132		A	Half Cycle, 60 Hz
Nonrept. On-State Current		I_{TSM}	120		A	Half Cycle, 50 Hz
Fusing Current		I^2t	72		A^2s	t = 10 ms, Half Cycle
Peak Gate Current		I_{GM}	4		A	10µs max.
Peak Gate Dissipation		P_{GM}	10		W	10µs max.
Gate Dissipation		$P_{G(AV)}$	1		W	20 ms max.
Operating Temperature		Tj	−40	125	°C	
Storage Temperature		T_{stg}	−40	125	°C	
Soldering Temperature		T_{sld}		250	°C	1.6 mm from case, 10 s max.

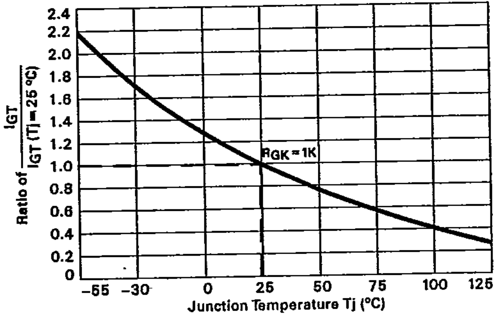
Electrical Characteristics $T_A = 25\,°C$ unless otherwise noted

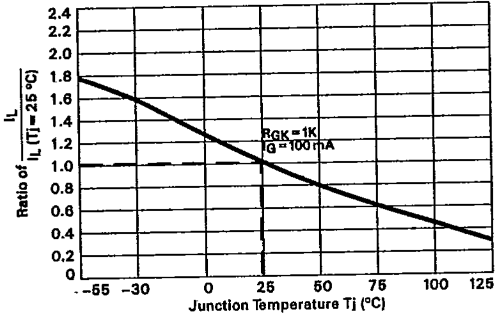
Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	I_{DRM}/I_{RRM}		1.5	mA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 125\,°C$
Off-State Leakage Current	I_{DRM}/I_{RRM}		5	µA	@$V_{DRM} + V_{RRM}$, $R_{GK} = 1\,K\Omega$, $T_j = 25\,°C$
On-State Voltage	V_T		1.80	V	at $I_T = 24\,A$, $T_j = 25\,°C$
On-State Threshold Voltage	$V_{T(TO)}$		1.0	V	$T_j = 125\,°C$
On-State Slope Resistance	r_T		36	mΩ	$T_j = 125\,°C$
Gate Trigger Current	I_{GT}	10	25	mA	$V_D = 7\,V$
Gate Trigger Voltage	V_{GT}		2.0	V	$V_D = 7\,V$
Holding Current	I_H		38	mA	$R_{GK} = 1\,K\Omega$
Latching Current	I_L		75	mA	$R_{GK} = 1\,K\Omega$
Critical Rate of Voltage Rise	dv/dt	200		V/µs	$V_D = .67 x V_{DRM}$ $R_{GK} = 1\,K\Omega$ $T_j = 125\,°C$
Critical Rate of Current Rise	di/dt	100		A/µs	$I_G = 125\,mA$ $di_G/dt = 1.25\,A/µs$ $T_j = 125\,°C$
Gate Controlled Delay Time	t_{gd}		500	ns	$I_G = 125\,mA$ $di_G/dt = 1.25\,A/µs$
Commutated Turn-Off Time	t_q		50	µs	$T_C = 85\,°C$ $V_D = .67 x V_{DRM}$ $V_R = 35\,V$ $I_T = I_{T(AV)}$
Thermal Resistance junc. to case	$R_{\Theta jc}$		3	K/W	
Thermal Resistance junc. to amb.	$R_{\Theta ja}$		60	K/W	

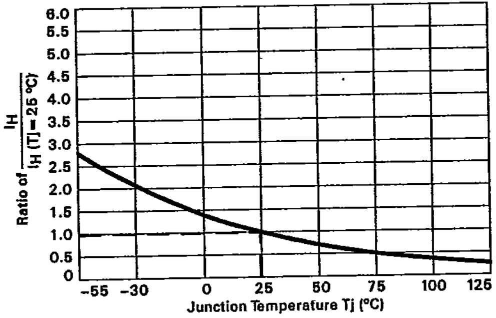
Typical Characteristics
S12 – Chips


Leakage Current vs Junction Temperature (typical)


Normalized DC Gate Trigger Voltage vs Junction Temperature (typical)

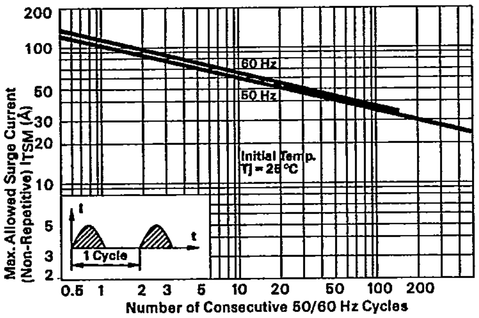

Normalized DC Gate Trigger Current vs Junction Temperature (typical)


Normalized DC Latching Current vs Junction Temperature (typical)

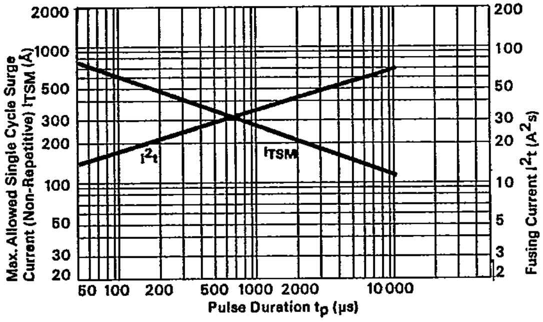

Normalized DC Holding Current vs Junction Temperature (typical)

Typical Characteristics
S12 – Packaged Parts

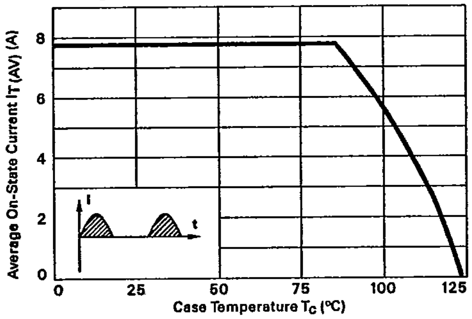
Max. Allowed Multi Cycle Surge (On-State) Current vs Number of Consecutive Cycles



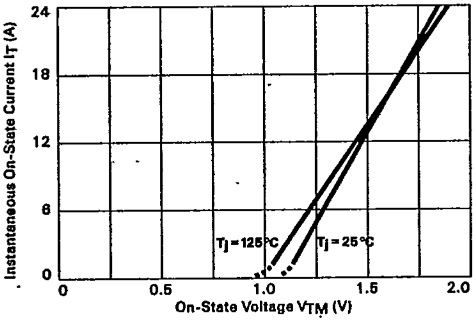
Max. Allowed Single Cycle Surge (On-State) Current vs Surge Current Duration



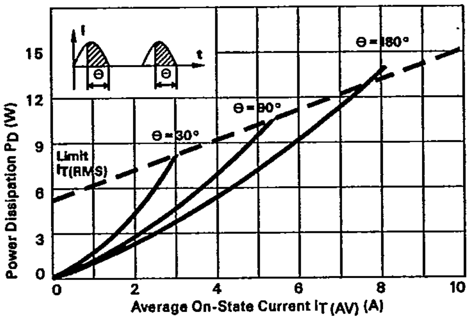
Average On-State Current vs Case Temperature



Instantaneous On-State Current vs On-State Voltage with Junction Temperature as Parameter



Power Dissipation vs Average On-State Current with Phase Conducting Angles as Parameter



Max. All. Power Dissip. vs Ambient Temp. with given Heatsink Thermal Resistances as Parameter