ECG® Semiconductors

ECG973, ECG973D

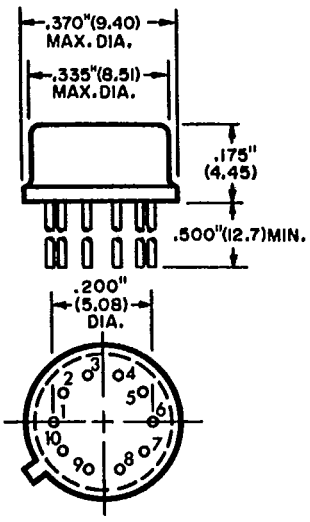
Modulator/Demodulator

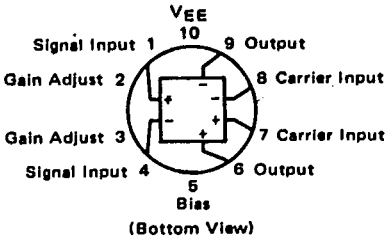
Features

- **Excellent carrier suppression**
  65 dB typ at 0.5 MHz
  50 dB typ at 10 MHz
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common mode rejection**
  86 dB typ

ECG973 is a metal package and ECG973D is a 14 pin DIP. They are silicon monolithic integrated circuits designed for use as a balanced modulator-demodulator where the output voltage is a product of an input voltage and a switching function. Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection and chopper applications.

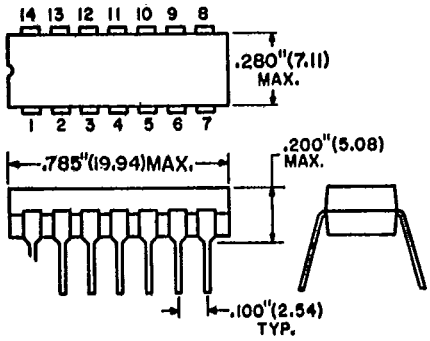
ECG973

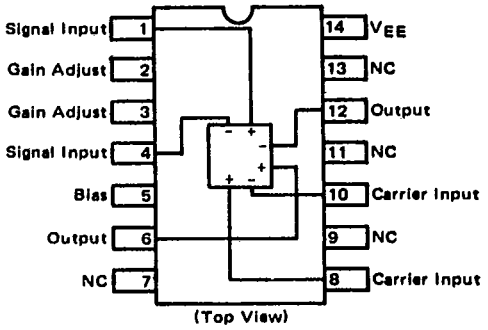




(Bottom View)

ECG973D





(Top View)

Maximum Ratings (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Rating	Unit
Applied Voltage (V_6-V_7, V_3-V_1, V_9-V_7, V_9-V_8, V_7-V_4, V_7-V_1, V_8-V_4, V_6-V_8, V_2-V_5, V_3-V_5)	ΔV	30	Vdc
Differential Input Signal	V_7, V_8 V_4, V_1	+5.0 +(5+I_5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Power Dissipation (Package Limitation) Dual In-Line Package Derate above T_A = +25°C Metal Package Derate above T_A = +25°C	P_D	 575 3.85 680 4.6	 mW mW/°C mW mW/°C
Operating Temperature	T_{opg}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Electrical Characteristics* (V_{CC} = +12 Vdc, V_{EE} = 8.0 Vdc, I_5 = =1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C unless otherwise noted.) (All input and output characteristics are single-ended unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Carrier Feedthrough V_C = 60 mV_{RMS} sine wave and offset adjusted to zero f_C = 1.0 kHz f_C = 10 MHz	5	1	V_{CFT}	 -- --	 40 140	 -- --	μV_{RMS}
V_C = 300 mVp-p square wave: offset adjusted to zero f_C = 1.0 kHz offset not adjusted f_C = 1.0 kHz				 -- --	 0.04 20	 0.4 200	mV_{RMS}
Carrier Suppression f_S = 10 kHz, 300 mV_{RMS} f_C = 500 kHz, 60 mV_{RMS} sine wave f_C = 10 MHz, 60 mV_{RMS} sine wave	5	2	V_{CS}	 40 --	 65 50	 -- --	dB k
Transadmittance Bandwidth (Magnitude) (R_L = 50 Ω) Carrier Input Port, V_C = 60 mV_{RMS} sine wave f_S = 1.0 kHz, 300 mV_{RMS} sine wave	8	8	BW_{3dB}	 --	 300	 --	MHz
Signal Input Port, V_S = 300 mV_{RMS} sine wave $\|V_C\|$ = 0.5 Vdc				--	80	--	MHz
Signal Gain V_S = 100 mV_{RMS}, f = 1.0 kHz; $\|V_C\|$ = 0.5 Vdc	10	3	A_{VS}	2.5	3.5	--	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz Parallel Input Resistance Parallel Input Capacitance	6	--	 r_{ip} c_{ip}	 -- --	 200 2.0	 -- --	 kΩ pF

Electrical Characteristics* (cont.)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Single-Ended Output Impedance, f = 10 MHz Parallel Output Resistance Parallel Output Capacitance	6	--	 r_{op} c_{op}	 -- --	 40 5.0	 -- --	 kΩ pF
Input Bias Current $I_{bS} = \frac{I_1+I_4}{2}$; $I_{bC} = \frac{I_7+I_8}{2}$	7	--	 I_{bS} I_{bC}	 -- --	 12 12	 30 30	μA
Input Offset Current $I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$	7	--	 $\lvert I_{ioS}\rvert$ $\lvert I_{ioC}\rvert$	 -- --	 0.7 0.7	 7.0 7.0	μA
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	7	--	$\lvert TC_{Iio}\rvert$	--	2.0	--	nA/°C
Output Offset Current ($I_6 - I_9$)	7	--	$\lvert I_{oo}\rvert$	--	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	7	--	$\lvert TC_{Ioo}\rvert$	--	90	--	nA/°C
Common-Mode Input Swing, Signal Port, f_s = 1.0 kHz	9	--	CMV	--	5.0	--	V_{p-p}
Common-Mode Gain, Signal Port, f_s = 1.0 kHz, $\lvert V_C\rvert$ = 0.5 Vdc	9	--	ACM	--	−85	--	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	--	V_o	--	8.0	--	Vdc
Differential Output Voltage Swing Capability	10	--	V_{out}	--	8.0	--	V_{p-p}
Power Supply Current $I_6 + I_9$ I_{1Q}	7	6	 I_{CC} I_{EE}	 -- --	 2.0 3.0	 4.0 5.0	mAdc
DC Power Dissipation	7	5	P_D	--	33	--	mW

* Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic packaged devices refer to the first page of this specification.

Notes

1. **Carrier Feedthrough**
   Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).
   Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

2. **Carrier Suppression**
   Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.
   Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The ECG973 has been characterized with a 60 $mV_{(RMS)}$ sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair—or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Note 3 and Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

3. **Signal Gain and Maximum Input Level**

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" ($V_C = 0.5$ Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5

$$V_S < I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

4. **Common-Mode Swing**

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen (see Note 6).

5. **Power Dissipation**

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e., assuming $V_9 = V_6$, $I_5 = I_6 = I_9$ and ignoring base current, $P_D = 2\ I_5\ (V_6 - V_{10}) + I_5\ (V_6 - V_{10})$ where subscripts refer to pin numbers.

6. **Design Equations**

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions. See Note 3 for R_e equation.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_9$$

$$I_B << I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V^- - \Phi}{I_5} - 500\ \Omega$$

where:

R_5 is the resistor between pin 5 and ground

$\Phi = 0.75$ V at $T_A = +25°C$

The ECG973 has been characterized for the condition $I_5 = 1.0$ mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_9 = V^+ - I_5 R_L$$

7. **Biasing**

The ECG973 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table:

$$30 \text{ Vdc} \geq [(V_6, V_9) - (V_7, V_8)] \geq 2 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_7, V_8) - (V_1, V_4)] \geq 2.7 \text{ Vdc}$$

$$30 \text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_9,\ V_7 = V_8,\ V_1 = V_4$$

Bias currents flowing into pins 1, 4, 7, and 8 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

8. **Transadmittance Bandwidth**

Carrier transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21C = \frac{I_O \text{ (each sideband)}}{V_S \text{ (signal)}} \Bigg|_{V_O = 0}$$

Signal transadmittance bandwidth is the 3-dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21S = \frac{I_O \text{ (signal)}}{V_S \text{ (signal)}} \Bigg|_{V_C = 0.5 \text{ Vdc}, V_O = 0}$$

*Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic packaged devices refer to the first page of this specification sheet.

9. **Coupling and Bypass Capacitors C_1 and C_2**

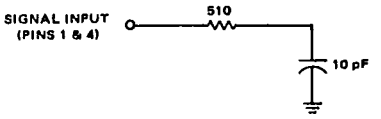
Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 ohms at the carrier frequency.

10. **Output Signal, V_O**

The output signal is taken from pin 6 and 9, either balanced or single-ended. Figure 12 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

11. **Signal Port Stability**

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1 k-ohm resistor in series with the inputs, pins 1 and 4. In this case input current drift may cause serious degradation of carrier suppression.

Performance Characteristics

Figure 1 —
Suppressed Carrier Output Waveform

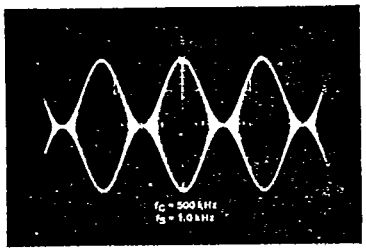


Figure 2 —
Suppressed Carrier Spectrum

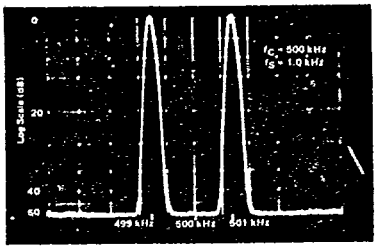


Figure 3 —
Amplitude Modulation Output Waveform

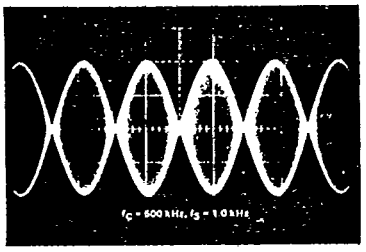
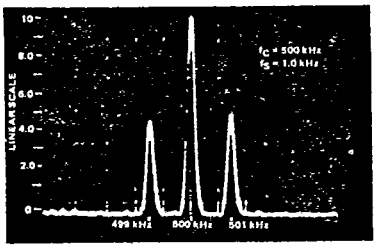


Figure 4 —
Amplitude Modulation Spectrum



Pin number references pertain to this device when packed in a metal can. To ascertain the corresponding pin numbers for plastic packaged devices refer to the first page of this specification.

Test Circuits

Figure 5 — Carrier Rejection and Suppression

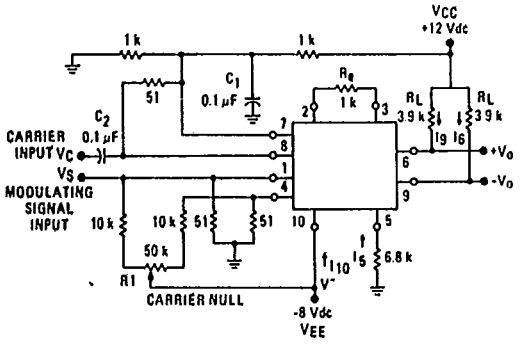


Figure 6 — Input-Output Impedance

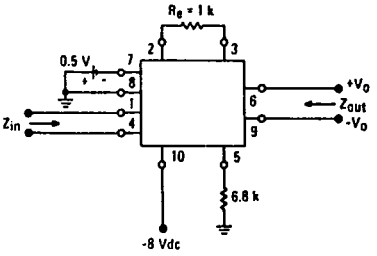


Figure 7 — Bias and Offset Currents

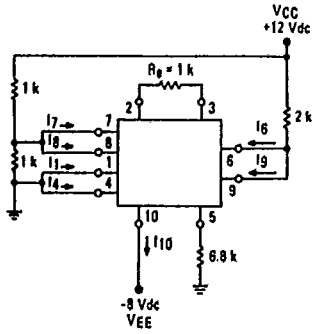


Figure 8 — Transconductance Bandwidth

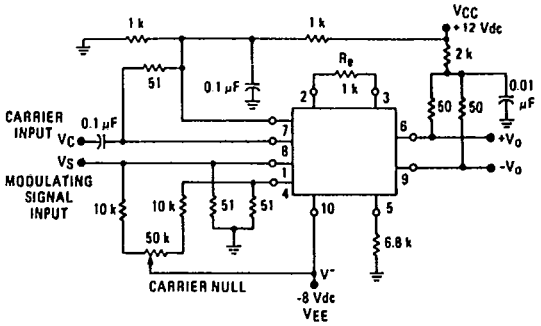


Figure 9 — Common-Mode Gain

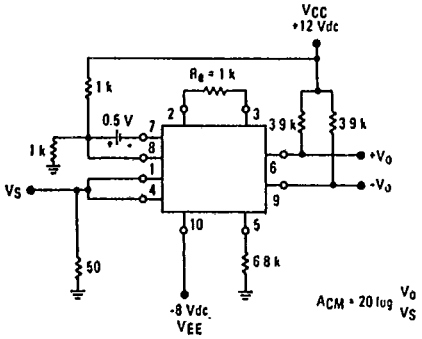
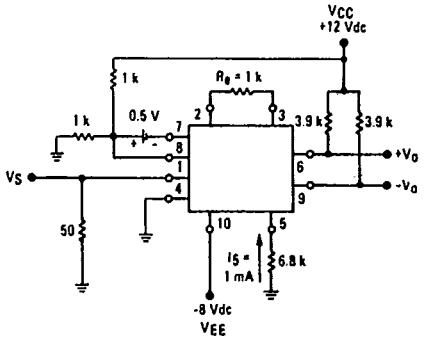


Figure 10 — Signal Gain and Output Swing



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic packaged devices refer to the first page of this specification.

Typical Characteristics

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 $mV_{(RMS)}$, f_S = 1 kHz, V_S = 300 $mV_{(RMS)}$, T_A = +25°C unless otherwise noted.

Figure 11 —
Sideband Output vs Carrier Levels

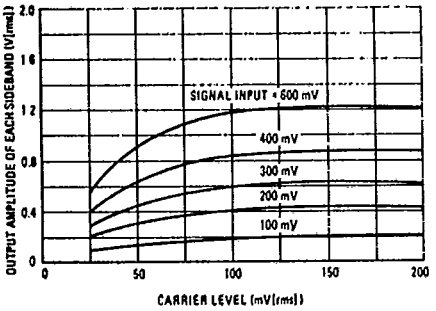


Figure 12 —
Signal Port Parallel Equivalent Input
Resistance vs Frequency

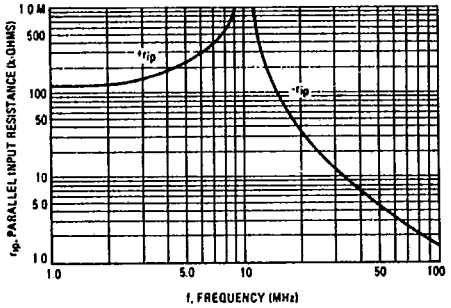


Figure 13 —
Signal Port Parallel Equivalent Input
Capacitance vs Frequency

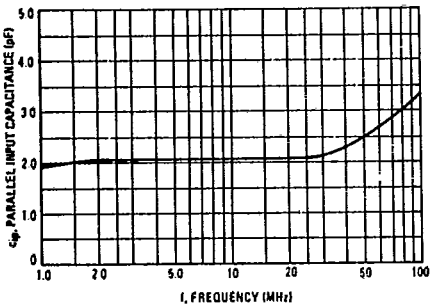


Figure 14 —
Single-Ended Output Impedance
vs Frequency

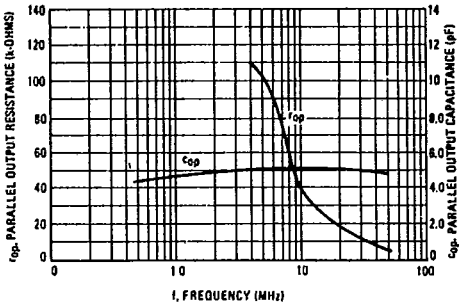


Figure 15 —
Sideband and Signal Port Transadmittances
vs Frequency

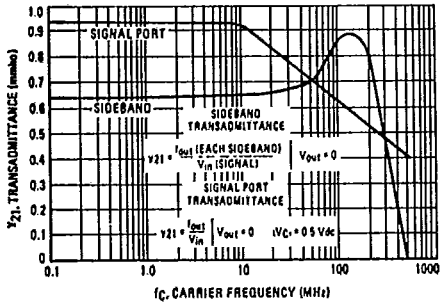
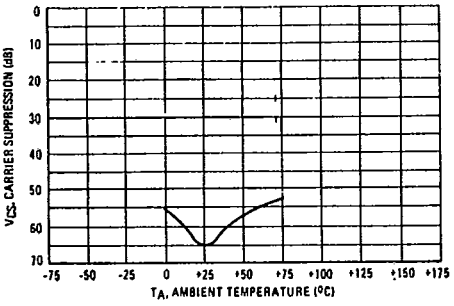


Figure 16 —
Carrier Suppression vs Temperature



Typical Characteristics (cont.)

Figure 17 —
Signal Port Frequency Response

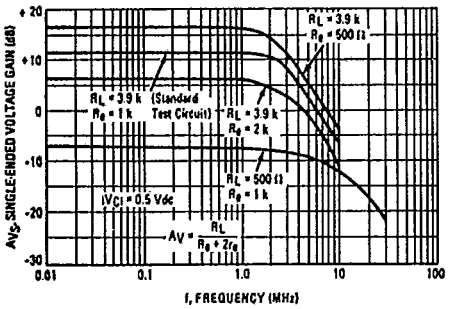


Figure 18 —
Carrier Suppression vs Frequency

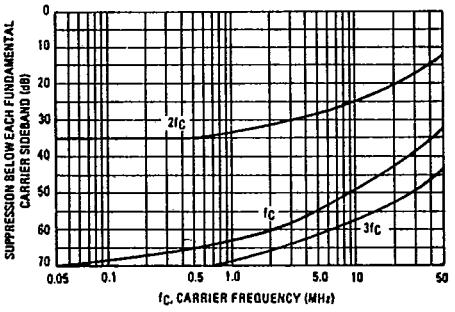


Figure 19 —
Carrier Feedthrough vs Frequency

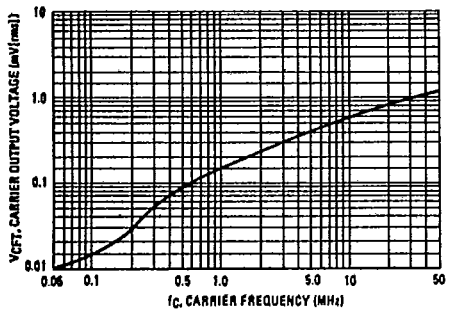


Figure 20 —
Sideband Harmonic Suppression
vs Input Signal Level

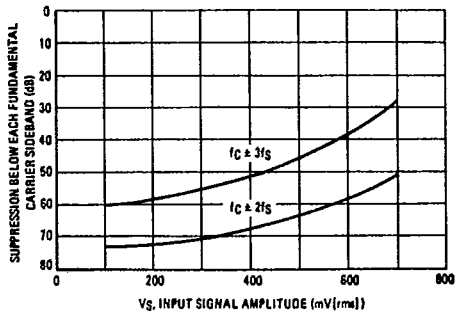


Figure 21 —
Suppression of Carrier Harmonic Sidebands
vs Carrier Frequency

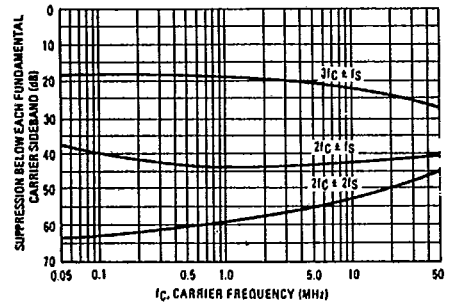
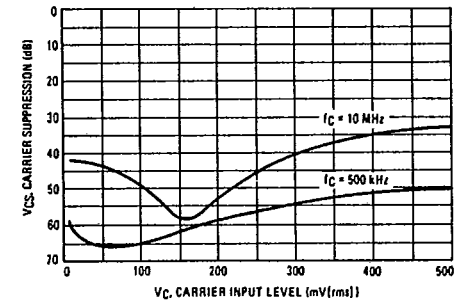


Figure 22 —
Carrier Suppression vs Carrier Input Level



Typical Operation Information

Figure 23 — Circuit Schematic

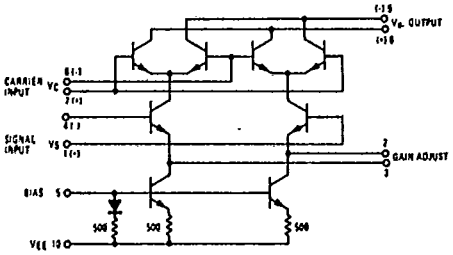


Figure 24 — Modulator Circuit

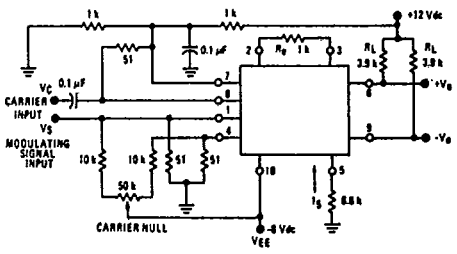


Figure 25 — AC and DC Voltage Gain and Output Frequencies

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E+2r_e)\frac{KT}{q}}$	f_M
High-level dc	$\frac{R_L}{R_E+2r_e}$	f_M

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\frac{KT}{q}(R_E+2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637\ R_L}{R_E+2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR (+12 Vdc SINGLE SUPPLY)

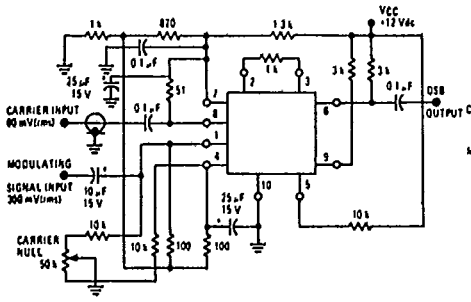


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

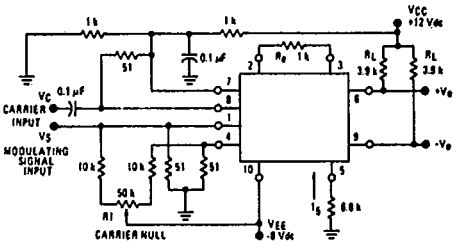


FIGURE 28 – AM MODULATOR CIRCUIT

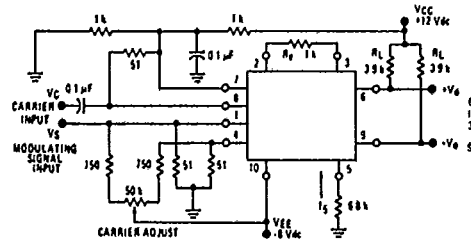
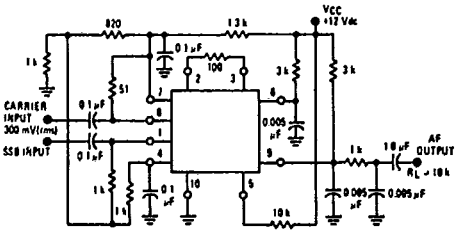


FIGURE 29 – PRODUCT DETECTOR (+12 Vdc SINGLE SUPPLY)



Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic packaged devices refer to the first page of this specification.

TYPICAL APPLICATIONS (continued)

FIGURE 30 – DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)

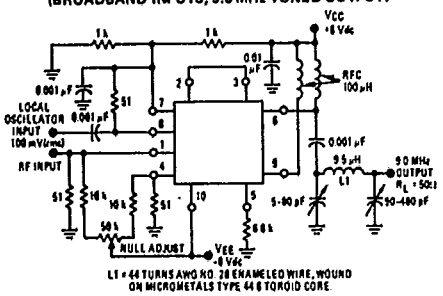


FIGURE 31 – LOW-FREQUENCY DOUBLER

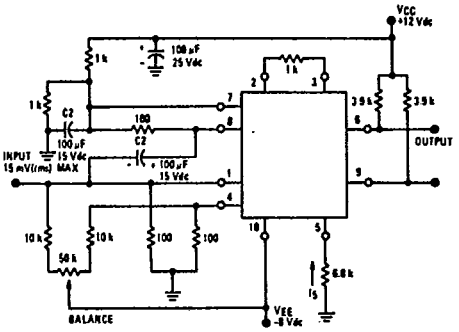
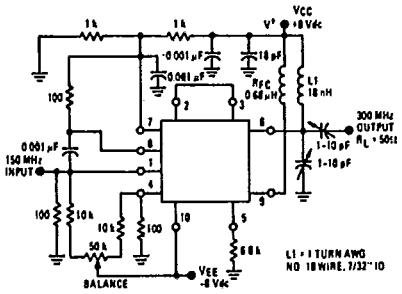
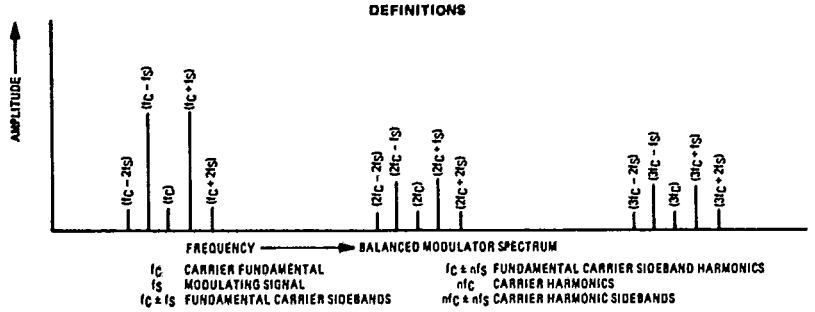


FIGURE 32 – 150 to 300 MHz DOUBLER



DEFINITIONS



f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

Pin number references pertain to this device when packaged in a metal can. To ascertain the corresponding pin numbers for plastic packaged devices refer to the first page of this specification.