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NTE2164
Integrated Circuit
65,536 X 1 Bit Dynamic Random Access Memory

Description:

The NTE2164 is 65, 536 words by 1 bit Dynamic N–Channel MOS RAM designed to operate from a single +5V power supply. The negative–voltage substrate bias is internally generated–its operation is both automatic and transparent.

The NTE2164 utilizes a three–poly N–channel silicon gate process which provides high storage cell density, high performance and high reliability.

The NTE2164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assures that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between Dynamic RAM generations.

The NTE2164 three–state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read–modify–write cycle, data is held on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The NTE2164 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$ only refresh cycles.

Refreshing is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, or normal read or write cycles on lthe 128 address combinations of A_O through A_6 during a 2 ms period.

Multiplexed address inputs permit the NTE2164 to be packaged in the standard 16 pin dual–in–line package. The 16 pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

Features:

- High Memory Density
- Multiplexed address inputs
- Single +5V supply
- On chip substrate bias generator
- Access Time: 150ns
- Read, Write Cycle Time: 270ns
- Low Power Dissipation: 250mW (Active), 28mW (Standby)
- Non–Latched Output is Three–State, TTL Compatible
- Read, Write, Read–Write, Read–Modify–Write, RAS Only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and low input capacitance

- 128 Refresh Cycles (A_O–A_6 Pins for Refresh Address)
- CAS Controlled Output Allows Hidden Refresh

Pin Names

A_O–A_7	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*:

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . –55°C to +150°C
Supply Voltages On Any Pin Except V_{CC} . . . . . –1 to +7 Volts (1)
Supply Voltage, V_{CC} . . . . . –0.5 to +7 Volts (1)
Short Circuit Output Current 50mA
Power Dissipation . . . . . 1 Watt

Note (1) Relative to V_{SS}

T_A = 25°C

***Comment**: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for ex tended periods may affect device reliability.

DC Characteristics: (T_A = 0°C to 70°C (1); V_{CC} = +5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{SS}	–	4.5 0	5.0 0	5.5 0	V
High Level Input Voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	V_{IHC}	All Voltages Referenced to V_{SS}	2.4	–	5.5	V
High Level Input Voltage, All Inputs Except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}	All Voltages Referenced to V_{SS}	2.4	–	5.5	V
Low Level Input Voltage, All Inputs	V_{IL}	All Voltages Referenced to V_{SS}	–2.0	–	0.8	V
Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} (Min)	I_{CC1}	(2)	–	–	50	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Standby Current Power Supply Standby Current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = Hi Impedance)	$I_{CC}2$		–	–	5.0	mA
Refresh Current Average Power Supply Current Refresh Mode RAS Cycling, CAS	I_{CC3}	(2)	–	–	40	mA
Page Mode Current Average Power Supply Current Page Mode Operation RAS = V_{IL}, CAS Cycling t_{PC} = t_{PC} (Min)	I_{CC4}		–	–	40	mA
Input Leakage Current Any Input V_{IN} = 0 to +5.5Volts All Other Pins Not Under Test = 0V	$I_{I(L)}$		–10	–	10	µA
Output Leakage Current is D_{OUT} is Disabled V_{OUT} = 0 to +5.5 Volts	$I_{O(L)}$		–10	–	10	µA
Output Levels High Level Output Voltage (I_{OUT} = 5mA)	V_{OH}		2.4	–	V_{CC}	V
Low Level Output Voltage (I_{OUT} = 4.2mA)	V_{OL}		0	–	0.4	V

Notes:

(1) T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycles rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.

(2) I_{CC1}, I_{CC3} & I_{CC4} depend on output loading and cycle rates. Specified rates are obtained with the output open.

AC Characteristics: (T_A = 0° to +70°C (1); V_{CC} = +5V ±10%; V_{SS} = 0V (3) (4)

Parameter	Symbol	Limits		Test Conditions	Unit
		Min	Max		
Random Read or Write Cycle Time	t_{RC}	270	–	(5)	ns
Read Write Cycle Time	t_{RWC}	270	–	(5)	ns
Page Mode Cycle Time	t_{PC}	170	–	–	ns
Access Time from $\overline{RAS}$	t_{RAC}	–	150	ns	(6) (8)
Access Time from $\overline{CAS}$	t_{CAC}	–	75	ns	(7) (8)
Output Buffer Turn–Off Delay	t_{OFF}	0	40	ns	(9)

Transition Time (Rise & Fall)	t_T	3	50	(4)	ns
$\overline{RAS}$ Precharge Time	t_{RP}	100	–		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	150	10,000		ns
$\overline{RAS}$ Hold Time	t_{RSH}	75	–		ns
$\overline{CAS}$ Pulse Width	t_{CAS}	75	10,000		ns
$\overline{CAS}$ Hold Time	t_{CSH}	150	–		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	75	(10)	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0	–		ns
$\overline{CAS}$ Precharge Time	t_{CPN}	25	–		ns
CAS Precharge Time (For Page Mode Cycle Only)	t_{CP}	60	–		ns
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0	–		ns
Row Address Set−Up Time	t_{ASR}	0	–		ns
Row Address Hold Time	t_{RAH}	15	–		ns
Column Address Set−Up Time	t_{ASC}	0	–		ns
Column Address Hold Time Referenced to $\overline{RAS}$	t_{CAH}	45	–		ns
Read Command Set−Up Time	t_{RCS}	0	–		ns
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	20	–	(13)	ns
Read Command Hold Time	t_{RCH}	0	–	(13)	ns
Write Command Hold Time	t_{WCH}	45	–		ns
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95	–		ns
Write Command Pulse Width	t_{WP}	45	–		ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	45	–		ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	45	–		ns
Data−In Set−Up Time	t_{DS}	0	–	(11)	ns
Data−In Hold Time	t_{DS}	45	–	(11)	ns
Data−In Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95	–		ns
Refresh Period	T_{REF}	–	2		ms
WRITE Command Set−Up Time	t_{WCS}	−10	–	(12)	ns
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	60	–	(12)	ns
$\overline{RAS}$ to WRITE Delay	t_{RWD}	110	–	(12)	ns

Note 1 T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible , however, provided AC operating parameters are met.

Note 2 An initial pause of 100µs is required after power−up followed by any 8 RAS cycles before proper device operation is achieved.

Note 3 AC measurements assume t_T = 5ns.

Note 4 V_{IHC} (min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.

Note 5 The specifications for T_{RC}(min) and t_{RWC}(min) are used only to indicate cycle times at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

Note 6 Assumes that $t_{RCS} \leq t_{RCD}$ (max). If t_{RCS} is greater than the maximum recommended values shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

Note 7 Assumes that $t_{RCD} \geq t_{RCD}$ (max).

Note 8 Measured with a load equivalent to 2TTL loads and 100pF.

Note 9 t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Note 10 Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

Note 11 These parameters are referenced to CAS leading edge in early write cycles and to $\overline{\text{WRITE}}$ leading edge in delayed write or read−modify−write cycles.

Note 12 t_{WCS},t_{CWD} and t_{RWD} are restrictive operating parameters in read−write and read−modify−write cycles only. If $t_{WCS} \geq t_{WCS}$ (min0, the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read−write and the data output will contain data read from the selected cell. if neither of the above conditions are met the conditions of the data out (at access time and until $\overline{\text{CAS}}$ goes back to V_{IH}) is indeterminate.

Note 13 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.