

**NOT RECOMMENDED FOR NEW DESIGNS
POSSIBLE SUBSTITUTE PRODUCT
IRFP150N**

January 2002

40A, 100V, 0.055 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17431.

Ordering Information

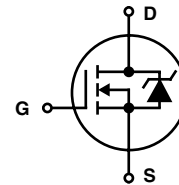
PART NUMBER	PACKAGE	BRAND
IRFP150	TO-247	IRFP150

NOTE: When ordering, include the entire part number.

Features

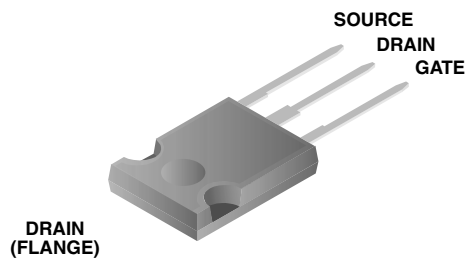
- 40A, 100V
- $r_{DS(ON)} = 0.055\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-247
TOP VIEW



IRFP150

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

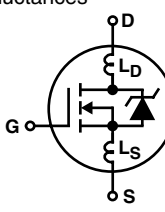
	IRFP150	UNITS
Drain to Source Voltage (Note 1)	100	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	100	V
Continuous Drain Current	40	A
$T_C = 100^\circ\text{C}$	26	A
Pulsed Drain Current (Note 3)	160	A
Gate to Source Voltage	± 20	V
Maximum Power Dissipation	180	W
Linear Derating Factor	1.44	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	150	mJ
Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS		
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$ (Figure 10)	100	-	-	V		
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	2.0	-	4.0	V		
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$	-	-	25	μA		
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$	-	-	250	μA		
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10\text{V}$	40	-	-	A		
Gate to Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA		
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = 22\text{A}$ (Figures 8, 9)	-	0.045	0.055	Ω		
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 20\text{V}$, $I_D = 20\text{A}$ (Figure 12)	13	20	-	S		
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 50\text{V}$, $I_D = 40\text{A}$, $R_{GS} = 6.8\Omega$, $R_L = 1.2\Omega$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	15	24	ns		
Rise Time	t_r		-	140	210	ns		
Turn-Off Delay Time	$t_{D(OFF)}$		-	60	89	ns		
Fall Time	t_f		-	90	140	ns		
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = 10\text{V}$, $I_D = 40\text{A}$, $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$. $I_{g(REF)} = 1.5\text{mA}$ (Figure 14)	-	70	110	nC		
Gate to Source Charge	Q_{gs}	Gate Charge is Essentially Independent of Operating Temperature	-	20	-	nC		
Gate to Drain "Miller" Charge	Q_{gd}		-	30	-	nC		
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$ (Figure 11)	-	2000	-	pF		
Output Capacitance	C_{OSS}		-	1000	-	pF		
Reverse-Transfer Capacitance	C_{RSS}		-	350	-	pF		
Internal Drain Inductance	L_D	Measured from the Drain Lead, 6mm (0.25in) from the Package to the Center of the Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 		-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) from the Header to the Source Bonding Pad			-	12.5	-	nH
Junction to Case	$R_{\theta JC}$		-	-	0.70	$^\circ\text{C/W}$		
Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^\circ\text{C/W}$		

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	40	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	170	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}C, I_{SD} = 40A, V_{GS} = 0V$ (Figure 13)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_{SD} = 40A, dI_{SD}/dt = 100A/\mu s$	98	-	530	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^{\circ}C, I_{SD} = 40A, dI_{SD}/dt = 100A/\mu s$	0.41	-	2.5	μC

NOTES:

2. Pulse Test: Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Repetitive Rating: Pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 10V$, starting $T_J = 25^{\circ}C$, $L = 170\mu H$, $R_G = 50\Omega$, Peak $I_{AS} = 40A$.

Typical Performance Curves Unless Otherwise Specified

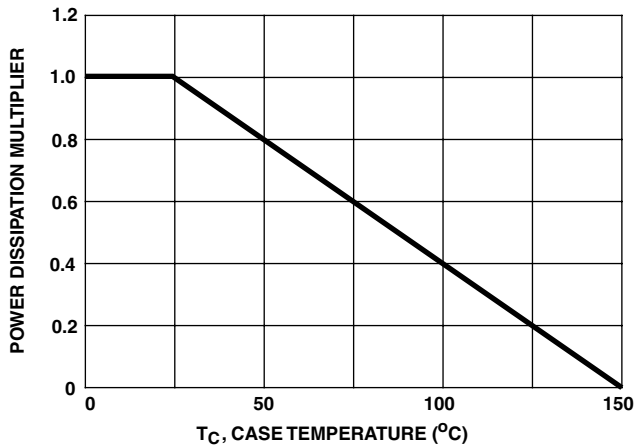


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

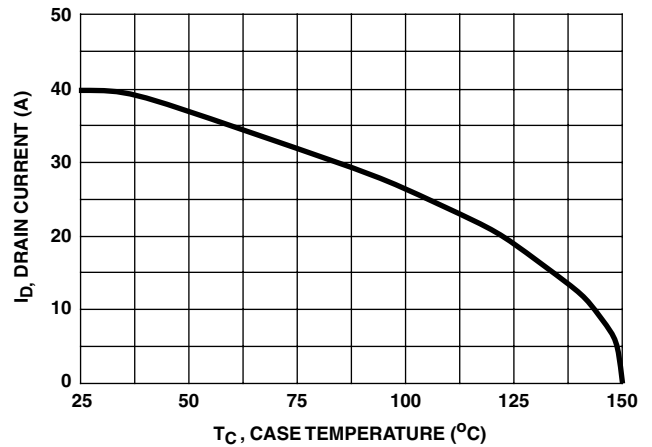


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

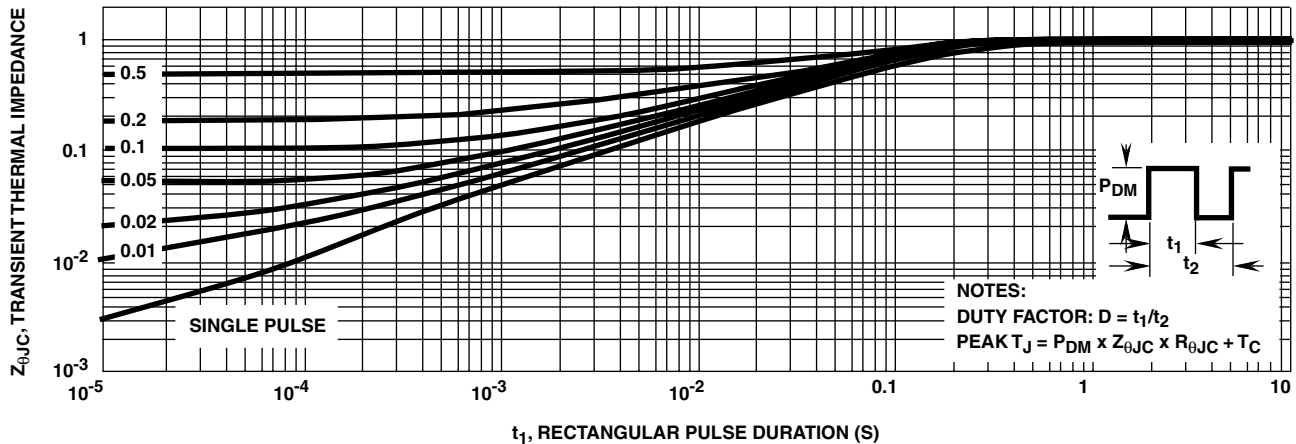


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

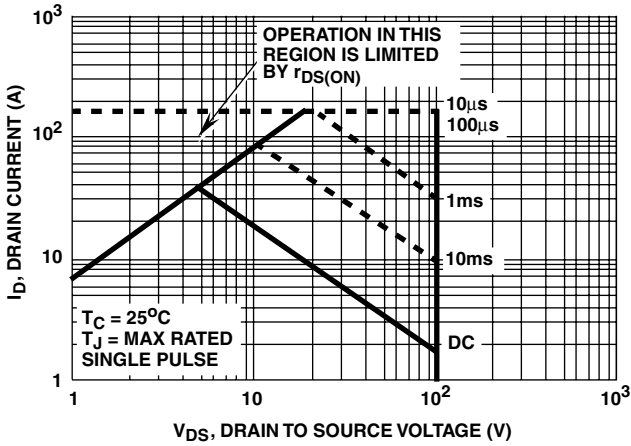


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

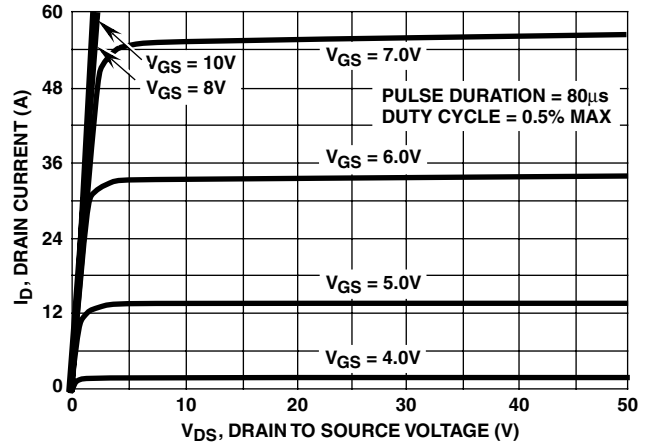


FIGURE 5. OUTPUT CHARACTERISTICS

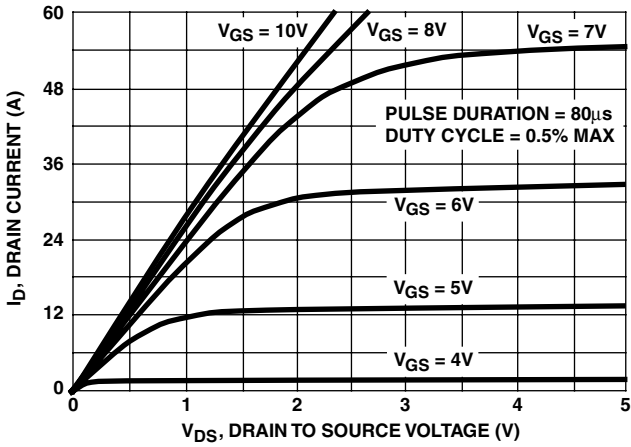


FIGURE 6. SATURATION CHARACTERISTICS

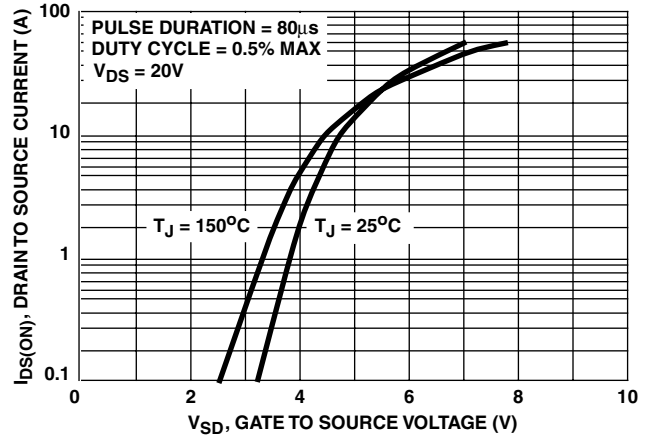


FIGURE 7. TRANSFER CHARACTERISTICS

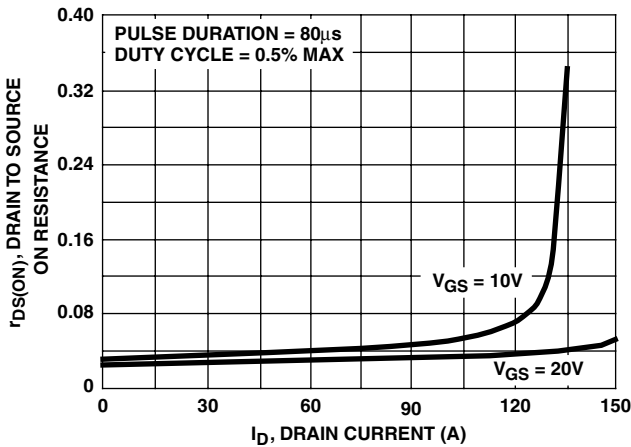


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

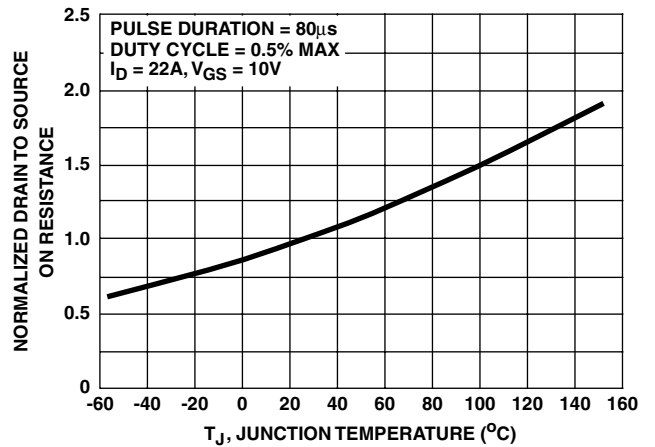


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

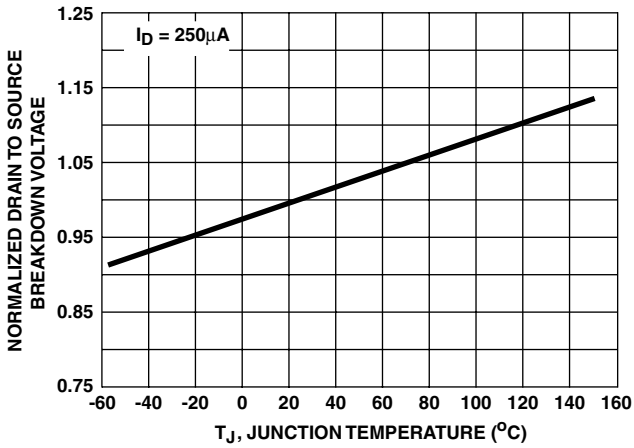


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

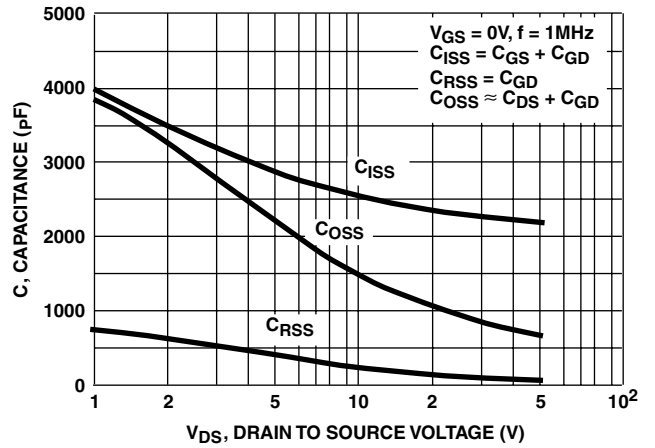


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

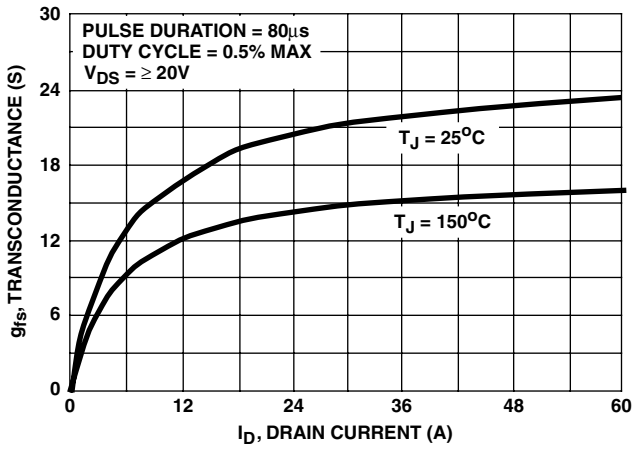


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

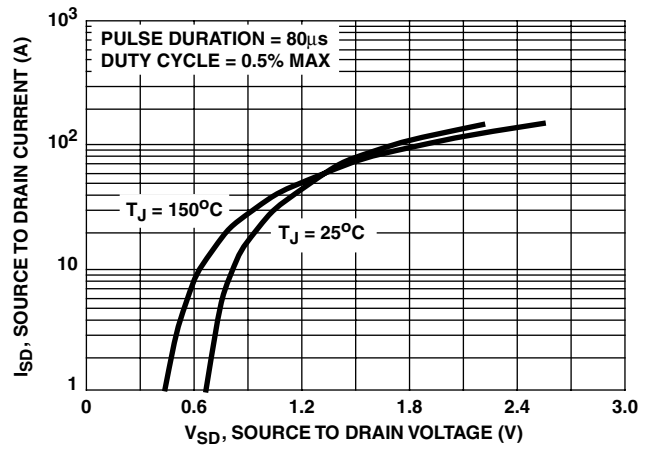


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

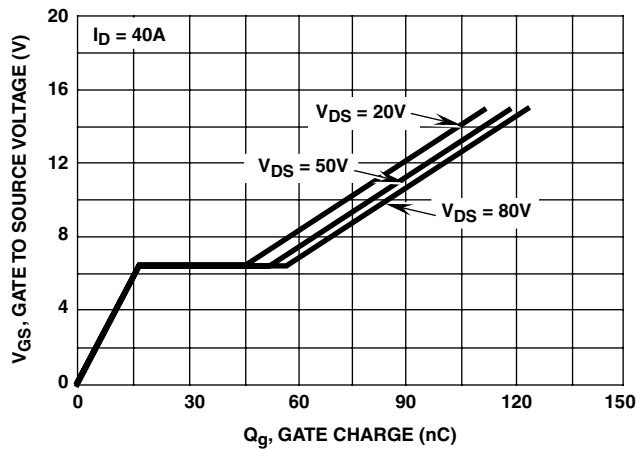


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

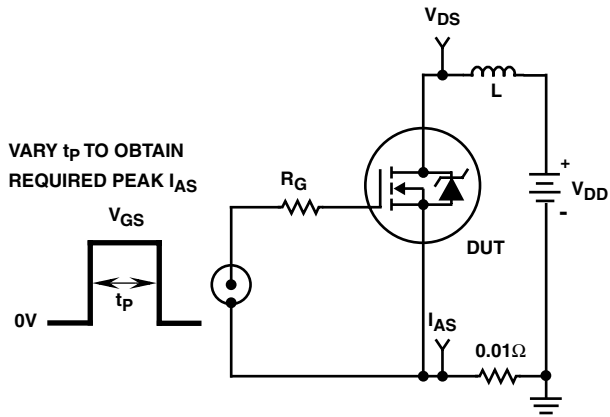


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

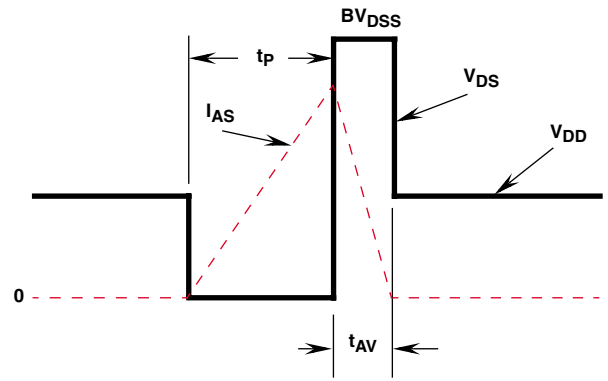


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

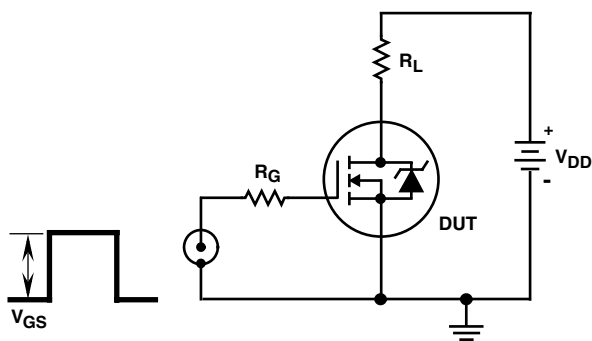


FIGURE 17. SWITCHING TIME TEST CIRCUIT

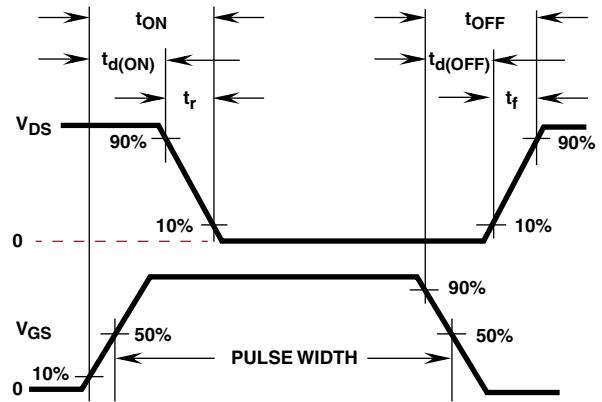


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

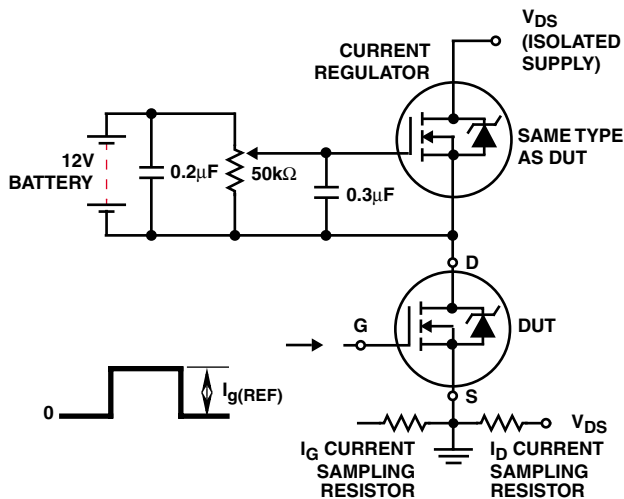


FIGURE 19. GATE CHARGE TEST CIRCUIT

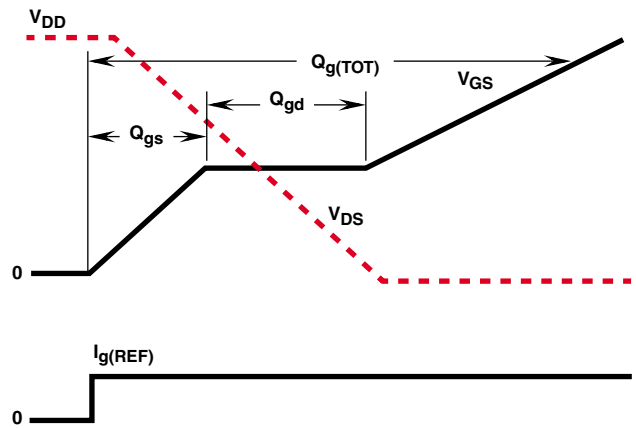


FIGURE 20. GATE CHARGE WAVEFORMS

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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