ICL7116, ICL7117

$3^1/_2$ Digit, LCD/LED Display, A/D Converter with Display Hold

January 1998

Features

- **HOLD Reading Input Allows Indefinite Display Hold**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **Direct Display Drive**
  - **LCD ICL7116**
  - **LED lCL7117**
- **Low Noise - Less Than 15μV_{P-P} (Typ)**
- **On Chip Clock and Reference**
- **Low Power Dissipation - Typically Less Than 10mW**
- **No Additional Active Circuits Required**
- **Surface Mount Package Available**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ICL7116CPL	0 to 70	40 Ld PDIP	E40.6
ICL7116CM44	0 to 70	44 Ld MQFP	Q44.10x10
ICL7117CPL	0 to 70	40 Ld PDIP	E40.6

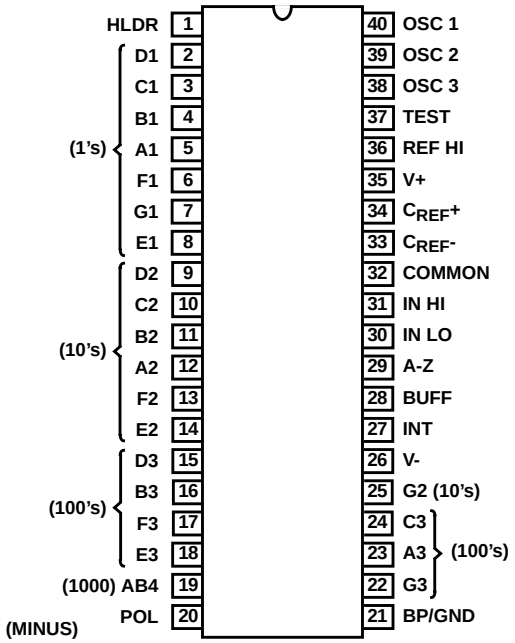
Description

The Intersil ICL7116 and ICL7117 are high performance, low power, $3^1/_2$ digit, A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7116 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive. The ICL7117 will directly drive an instrument size, light emitting diode (LED) display.

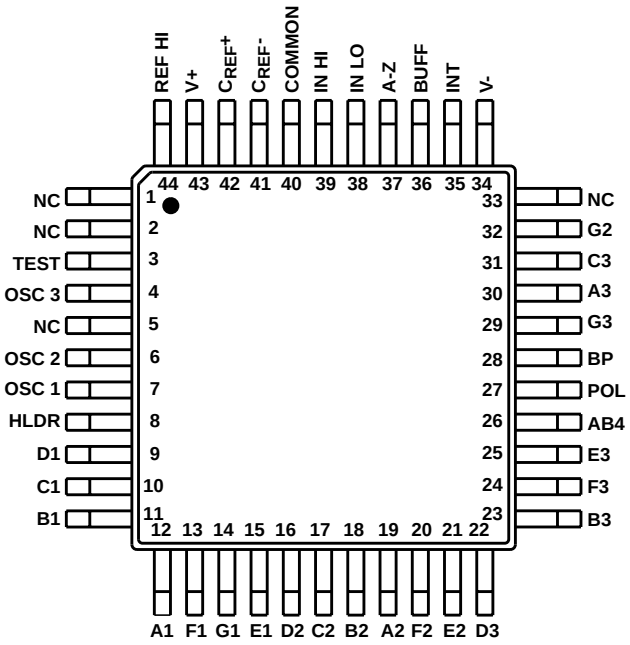
The ICL7116 and ICL7117 have all of the features of the ICL7106 and ICL7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and retain the value on the display indefinitely. To make room for this feature the reference low input has been connected to Common internally rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the ICL7106 and ICL7107. They feature auto-zero to less than 10μV, zero drift of less than 1$\mu V/^oC$, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (ICL7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

Pinouts

ICL7116, ICL7117 (PDIP)
TOP VIEW



ICL7116 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Absolute Maximum Ratings

Supply Voltage
- ICL7116, V+ to V- 15V
- ICL7117, V+ to GND 6V
- ICL7117, V- to GND . . . . . -9V

Analog Input Voltage (Either Input) (Note 1) . . . . . V+ to V-
Reference Input Voltage (Either Input) . . . . . V+ to V-
Clock Input
- ICL7116 . . . . . TEST to V+
- ICL7117 . . . . . GND to V+

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (^{o}C/W)
PDIP Package	50
MQFP Package	80

Maximum Junction Temperature . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(MQFP - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . 0^{o}C to 70^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

(Note 3) T_A = 25^{o}C, f_{CLOCK} = 48kHz, V_{REF} = 100mV

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Zero Input Reading	V_{IN} = 0V, Full Scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error	-V_{IN} = +V_{IN} ≅ 195mV Difference in Reading for Equal Positive and Negative Inputs Near Full Scale	-	±0.2	±1	Counts
Linearity	Full Scale = 200mV or Full Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 5)	-	±0.2	±1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200mV (Note 5)	-	50	-	µV/V
Noise	V_{IN} = 0V, Full Scale = 200mV (Peak-To-Peak Value Not Exceeded 95% of Time) (Note 5)	-	15	-	µV
Leakage Current Input	V_{IN} = 0 (Note 5)	-	1	10	pA
Zero Reading Drift	V_{IN} = 0, 0^{o}C To 70^{o}C (Note 5)	-	0.2	1	µV/^{o}C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0^{o}C To 70^{o}C (Note 5)	-	1	5	ppm/^{o}C
V+ Supply Current	V_{IN} = 0 (Does Not Include LED Current for ICL7117)	-	1.0	1.8	mA
V- Supply Current	ICL7117 Only	-	0.6	1.8	mA
COMMON Pin Analog Common Voltage	25kΩ Between Common and Positive Supply (With Respect to + Supply)	2.4	3.0	3.2	V
Temperature Coefficient of Analog Common	25kΩ Between Common and Positive Supply (With Respect to + Supply) (Note 5)	-	80	-	ppm/^{o}C
DISPLAY DRIVER (ICL7116 ONLY)					
Peak-To-Peak Segment Drive Voltage Peak-To-Peak Backplane Drive Voltage	V+ = to V- = 9V, (Note 4)	4	5.5	6	V
DISPLAY DRIVER (ICL7117 ONLY)					
Segment Sinking Current	V+ = 5V, Segment Voltage = 3V				
(Except Pins 19 and 20)		5	8	-	mA
Pin 19 Only		10	16	-	mA
Pin 20 Only		4	7	-	mA

NOTES:

3. Unless otherwise noted, specifications apply to both the ICL7116 and ICL7117. ICL7116 is tested in the circuit of Figure 1. ICL7117 is tested in the circuit of Figure 2.
4. Back plane drive is in phase with segment drive for 'off' segment, 180 degrees out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5. Not tested, guaranteed by design.

Typical Applications and Test Circuits

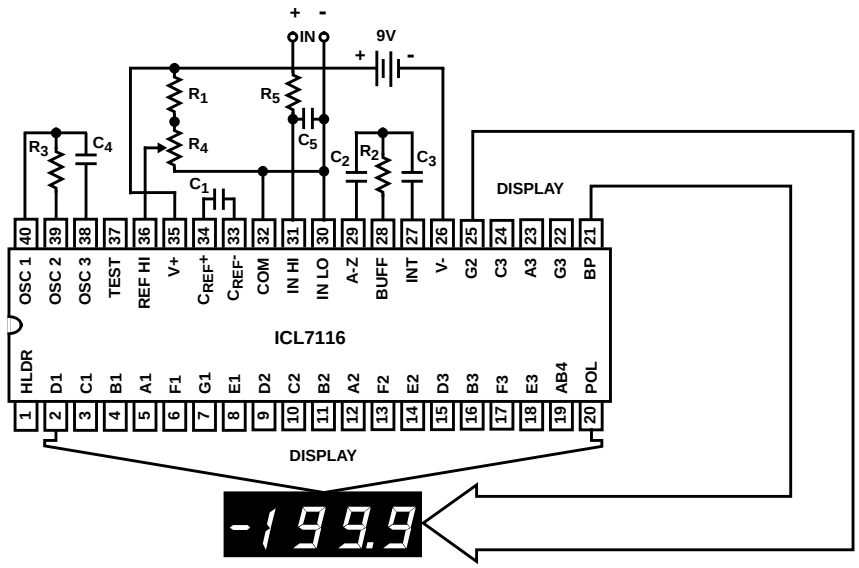


FIGURE 1. ICL7116 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

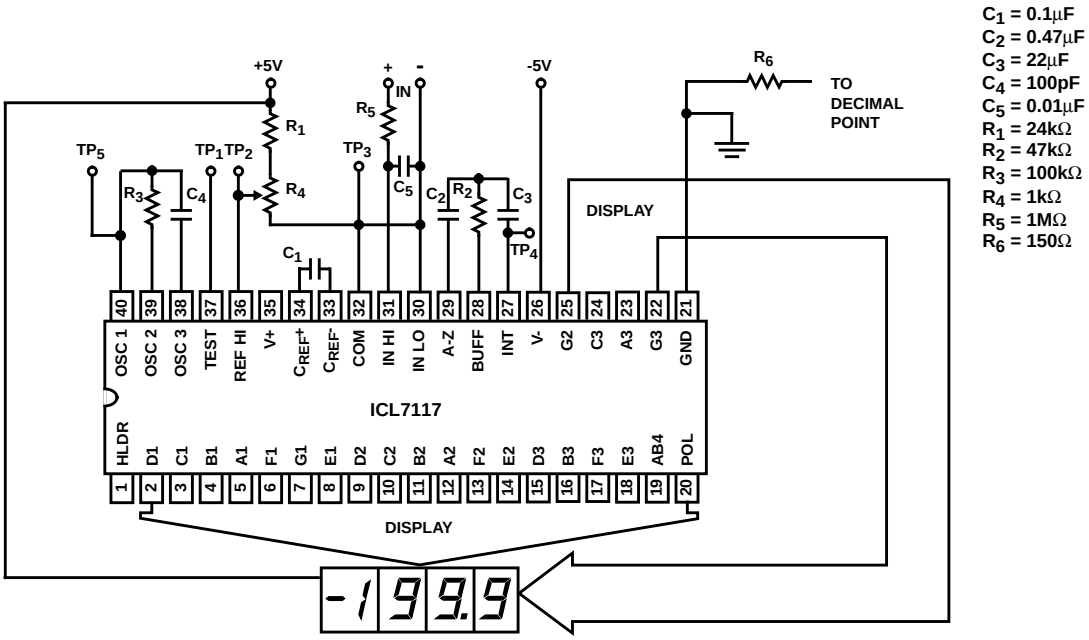


FIGURE 2. ICL7117 TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50k\Omega$
  f_{OSC} (Typ) = 48kHz

- **OSCILLATOR PERIOD**

  $t_{OSC} = RC/0.45$

- **INTEGRATION CLOCK FREQUENCY**

  $f_{CLOCK} = f_{OSC}/4$

- **INTEGRATION PERIOD**

  $t_{INT} = 1000 \times (4/f_{OSC})$

- **60/50Hz REJECTION CRITERION**

  t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

- **OPTIMUM INTEGRATION CURRENT**

  $I_{INT} = 4\mu A$

- **FULL SCALE ANALOG INPUT VOLTAGE**

  V_{INFS} (Typ) = 200mV or 2V

- **INTEGRATE RESISTOR**

  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

  $$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

  $$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

- **V_{INT} MAXIMUM SWING:**

  $(V- + 1.0V) < V_{INT} < (V+ - 0.5V)$, V_{INT} (Typ) = 2V

- **DISPLAY COUNT**

  $$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**

  $t_{CYC} = t_{CL0CK} \times 4000$
  $t_{CYC} = t_{OSC} \times 16{,}000$
  when f_{OSC} = 48KHz; t_{CYC} = 333ms

- **COMMON MODE INPUT VOLTAGE**

  $(V- + 1V) < V_{IN} < (V+ - 0.5V)$

- **AUTO-ZERO CAPACITOR**

  $0.01\mu F < C_{AZ} < 1\mu F$

- **REFERENCE CAPACITOR**

  $0.1\mu F < C_{REF} < 1\mu F$

- **V_{COM}**

  Biased between V+ and V-.

- **$V_{COM} \cong$ V+ - 2.8V**

  Regulation lost when V+ to V- < ≅6.8V.
  If V_{COM} is externally pulled down to (V + to V -)/2, the V_{COM} circuit will turn off.

- **ICL7116 POWER SUPPLY: SINGLE 9V**

  V+ - V- = 9V
  Digital supply is generated internally
  $V_{TEST} \cong$ V+ - 4.5V

- **ICL7116 DISPLAY: LCD**

  Type: Direct drive with digital logic supply amplitude.

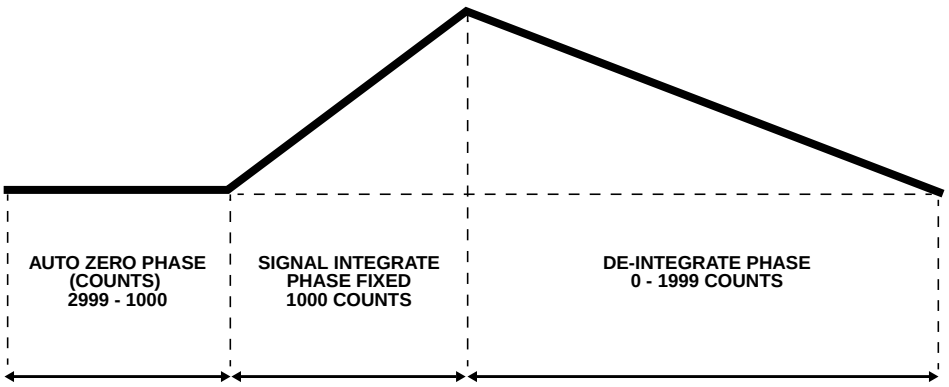
- **ICL7117 POWER SUPPLY: DUAL ±5.0V**

  V+ = +5V to GND
  V- = -5V to GND
  Digital Logic and LED driver supply V+ to GND

- **ICL7117 DISPLAY: LED**

  Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 4000 x t_{CLOCK} = 16,000 x t_{OSC}

Pin Descriptions

PIN NUMBER		NAME	FUNCTION	DESCRIPTION
40 PIN DIP	44 PIN FLATPACK			
1	8	HLDR	Input	Display Hold Control.
2	9	D1	Output	Driver Pin for Segment “D” of the display units digit.
3	10	C1	Output	Driver Pin for Segment “C” of the display units digit.
4	11	B1	Output	Driver Pin for Segment “B” of the display units digit.
5	12	A1	Output	Driver Pin for Segment “A” of the display units digit.
6	13	F1	Output	Driver Pin for Segment “F” of the display units digit.
7	14	G1	Output	Driver Pin for Segment “G” of the display units digit.
8	15	E1	Output	Driver Pin for Segment “E” of the display units digit.
9	16	D2	Output	Driver Pin for Segment “D” of the display tens digit.
10	17	C2	Output	Driver Pin for Segment “C” of the display tens digit.
11	18	B2	Output	Driver Pin for Segment “B” of the display tens digit.
12	19	A2	Output	Driver Pin for Segment “A” of the display tens digit.
13	20	F2	Output	Driver Pin for Segment “F” of the display tens digit.
14	21	E2	Output	Driver Pin for Segment “E” of the display tens digit.
15	22	D3	Output	Driver pin for segment “D” of the display hundreds digit.
16	23	B3	Output	Driver pin for segment “B” of the display hundreds digit.
17	24	F3	Output	Driver pin for segment “F” of the display hundreds digit.
18	25	E3	Output	Driver pin for segment “E” of the display hundreds digit.
19	26	AB4	Output	Driver pin for both “A” and “B” segments of the display thousands digit.
20	27	POL	Output	Driver pin for the negative sign of the display.
21	28	BP/GND	Output	Driver pin for the LCD backplane/Power Supply Ground.
22	29	G3	Output	Driver pin for segment “G” of the display hundreds digit.
23	30	A3	Output	Driver pin for segment “A” of the display hundreds digit.
24	31	C3	Output	Driver pin for segment “C” of the display hundreds digit.
25	32	G2	Output	Driver pin for segment “G” of the display tens digit.
26	34	V-	Supply	Negative power supply.
27	35	INT	Output	Integrator amplifier output. To be connected to integrating capacitor.
28	36	BUFF	Output	Input buffer amplifier output. To be connected to integrating resistor.
29	37	A-Z	Input	Integrator amplifier input. To be connected to auto-zero capacitor.
30 31	38 39	IN LO IN HI	Input	Differential inputs. To be connected to input voltage to be measured. LO and HI designators are for reference and do not imply that LO should be connected to lower potential, e.g., for negative inputs IN LO has a higher potential than IN HI.
32	40	COMMON	Supply/ Output	Internal voltage reference output.
33 34	41 42	C_{REF}- C_{REF}+		Connection pins for reference capacitor.
35 36	43 44	V+ REF HI	Supply	Power Supply.
37	3	TEST	Input	Display test. Turns on all segments when tied to V+.
38 39 40	4 6 7	OSC3 OSC2 OSC1	Output Output Input	Device clock generator circuit connection pins.

Detailed Description

Analog Section

Figure 3 shows the Analog Section for the ICL7116 and ICL7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000\left(\frac{V_{IN}}{V_{REF}}\right).$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.5V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

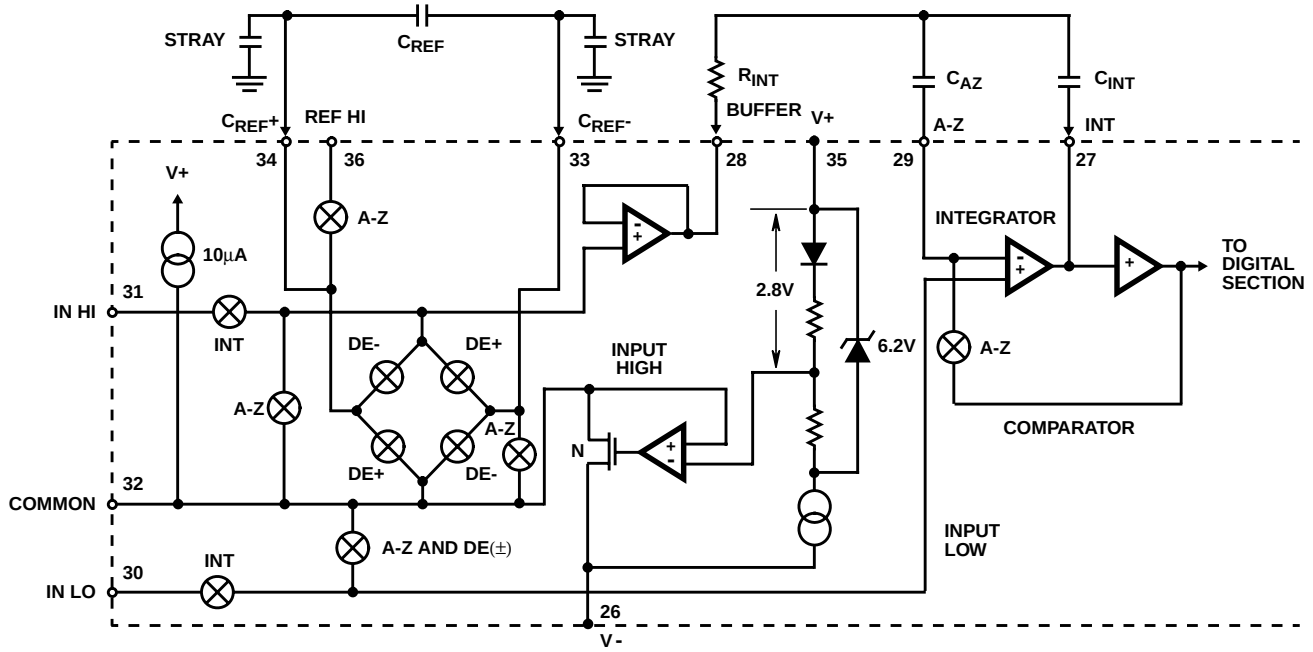


FIGURE 3. ANALOG SECTION OF ICL7116 AND ICL711

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (ICL7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V less than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6.8V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>6.8V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/^{O}C.

The limitations of the on chip reference should also be recognized, however. With the ICL7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25μV to 80μV$_{P-P}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over range and a non-over range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The ICL7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the lC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

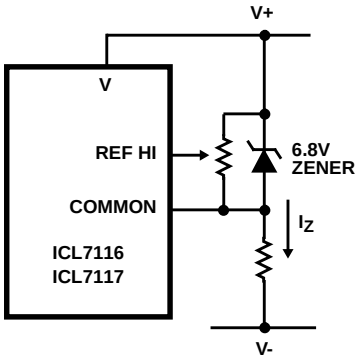


FIGURE 4A.

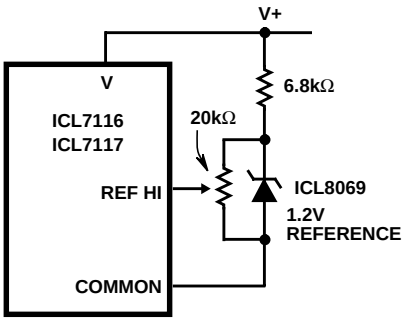


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the ICL7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other annunciator the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

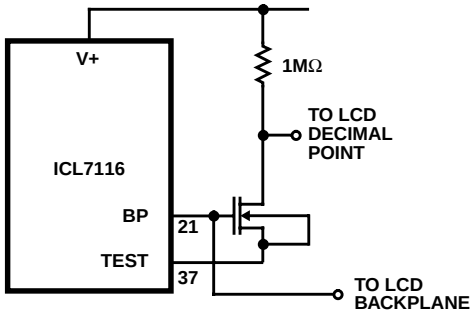


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

The second function is a “lamp test”. When TEST is pulled high (to V+) all segments will be turned on and the display should read “-1888”. The TEST pin will sink about 5mA under these conditions.

CAUTION: On the ICL7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

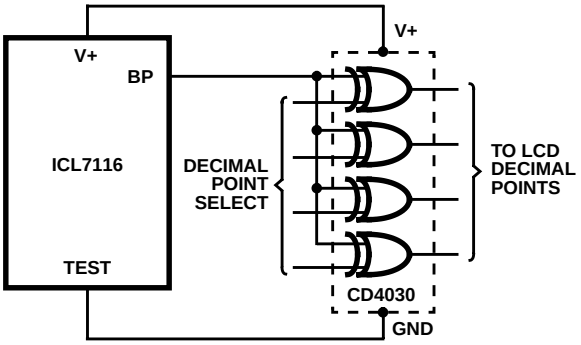


FIGURE 6. EXCLUSIVE 'OR' GATE FOR DECIMAL POINT DRIVE

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (ICL7116) or GROUND (ICL7117) to continuously update the display. This input is CMOS compatible, and has a 70kΩ (See Figure 7) typical resistance to either TEST (ICL7116) or GROUND (ICL7117).

Digital Section

Figures 7 and 8 show the digital section for the ICL7116 and ICL7117, respectively. In the ICL7116, an internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the ICL7117. It is identical to the ICL7116 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

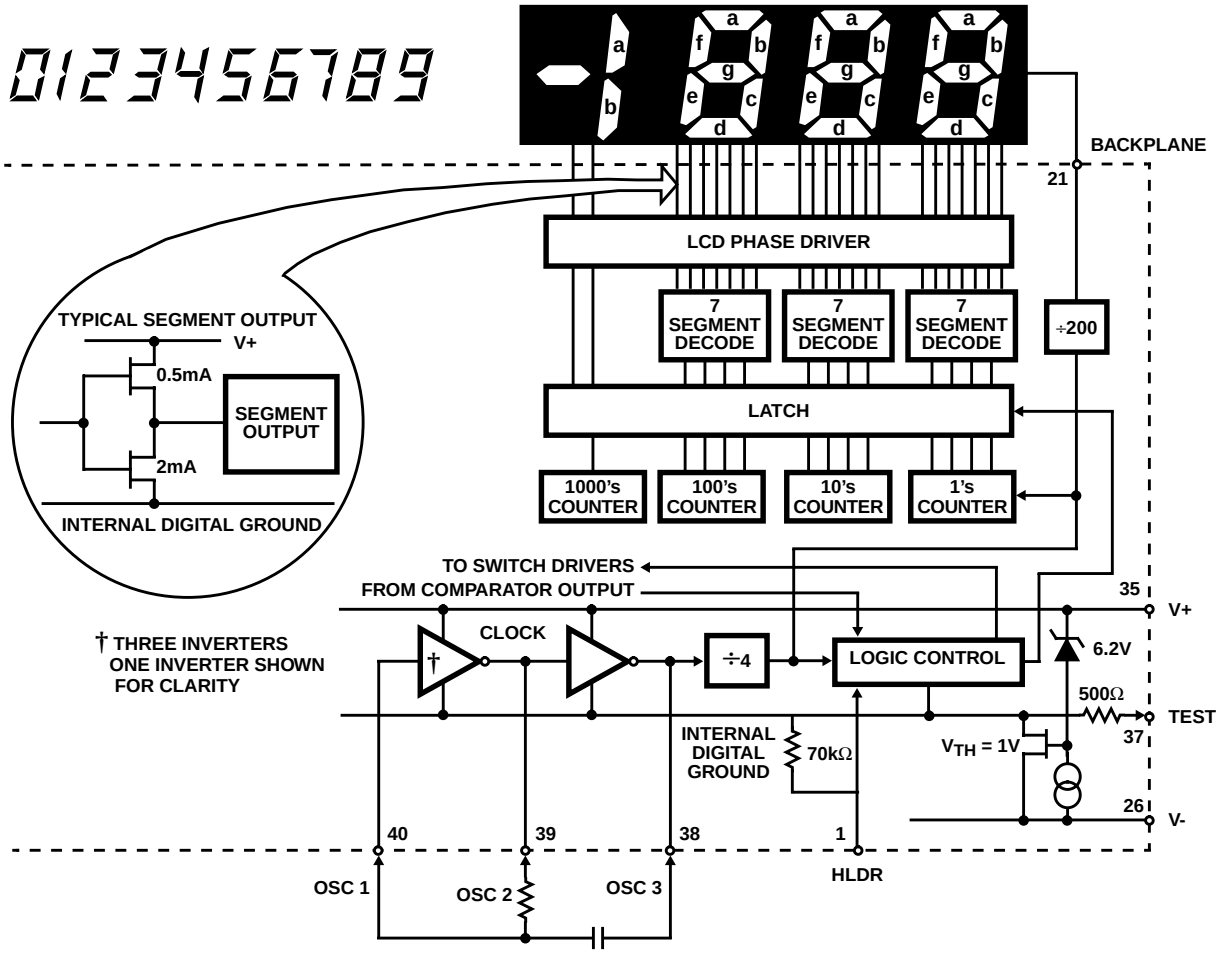


FIGURE 7. ICL7116 DIGITAL SECTION

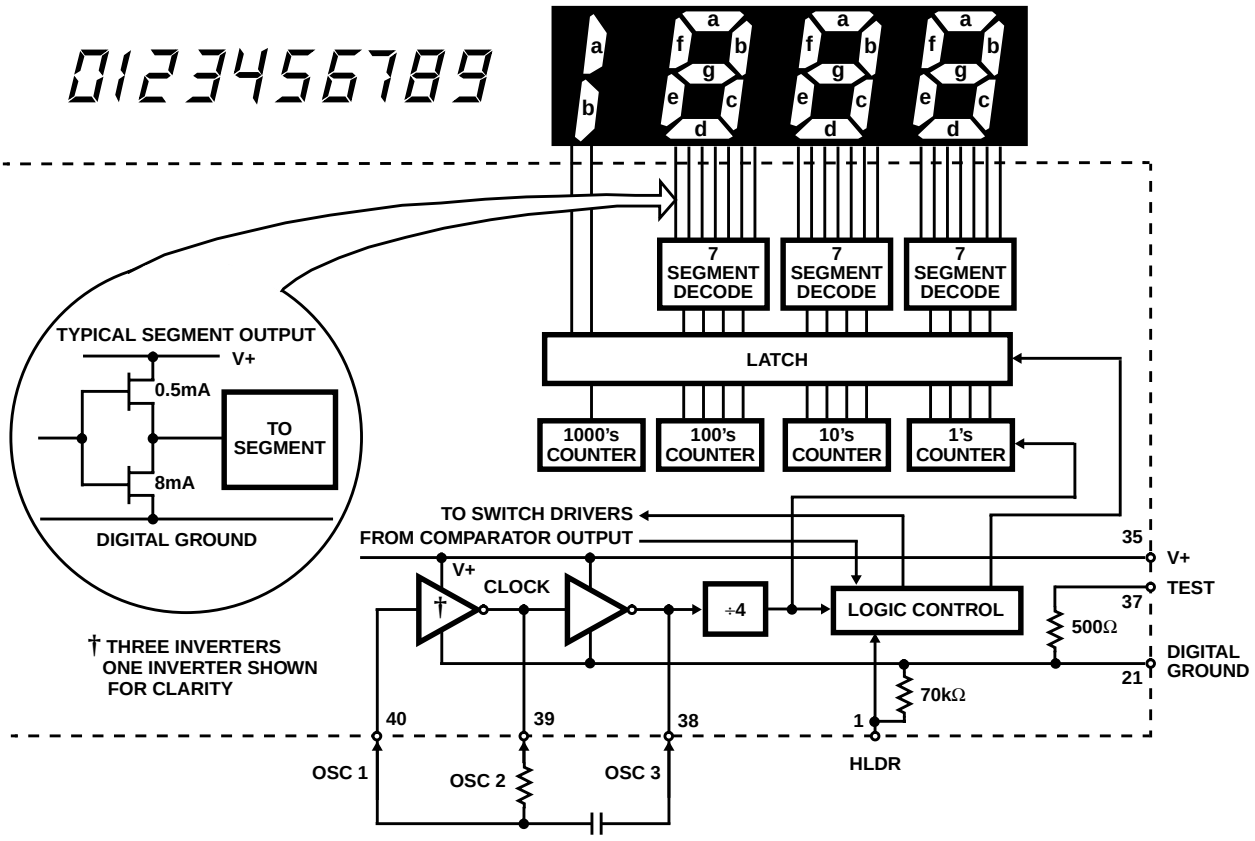


FIGURE 8. ICL7117 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the ICL7116 and ICL7117. Two basic clocking arrangements can be used:

1. Figure 9A, an external oscillator connected to pin 40.
2. Figure 9B, an R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 counts to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^{1}/_{3}$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^{2}/_{3}$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

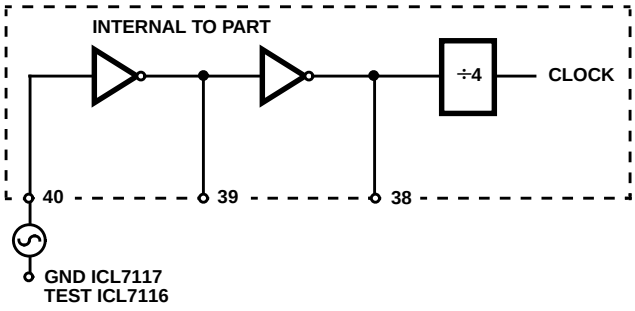


FIGURE 9A. EXTERNAL OSCILLATOR

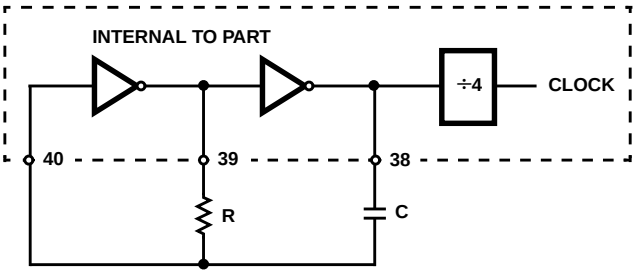


FIGURE 9B. RC OSCILLATOR

FIGURE 9. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 4µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.5V from either supply). In the ICL7116 or the ICL7117, when the analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For the ICL7117 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22µF and 0.1µF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47µF capacitor is recommended. On the 2V scale, a 0.047µF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1µF capacitor gives good results in most applications. Generally 1µF will hold the roll-over error to 0.5 counts in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation:

$$f = \frac{0.45}{RC}$$ For 48kHz Clock (3 Readings/sec), $C = 100pF$.

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22µF. This makes the system slightly quieter and also avoids a divider network on the input. The ICL7117 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

ICL7117 Power Supplies

3. The ICL7117 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive IC. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

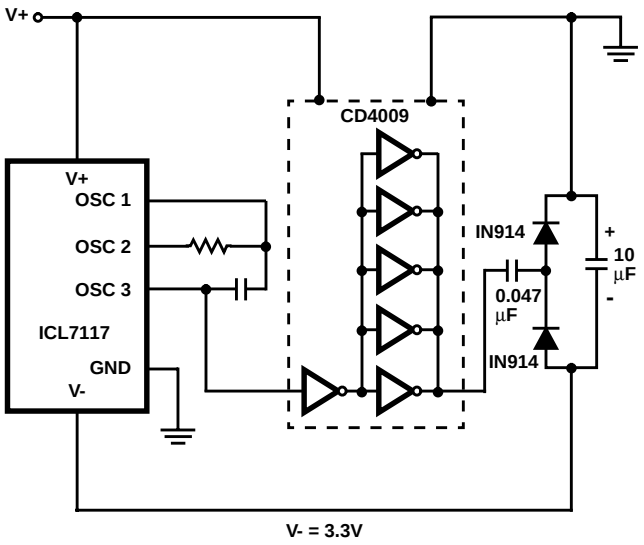


FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

Typical Applications

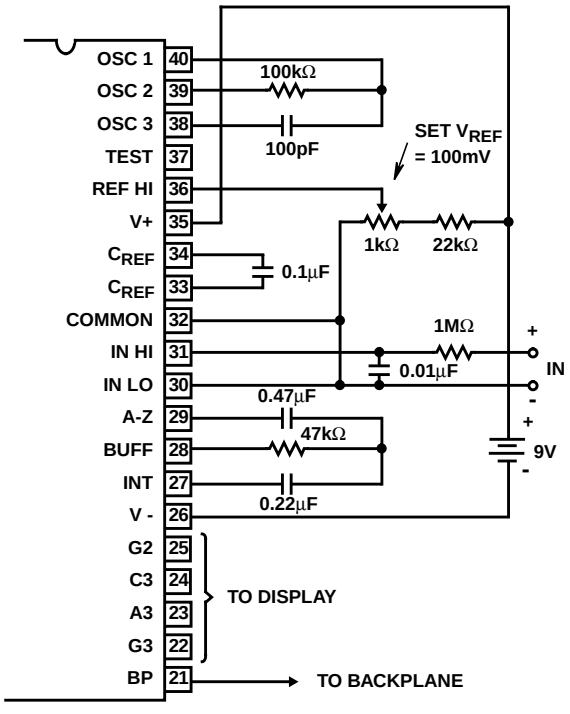
The ICL7116 and ICL7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

The following application notes contain very useful information on understanding and applying this part and are available from Intersil Corporation.

Application Notes

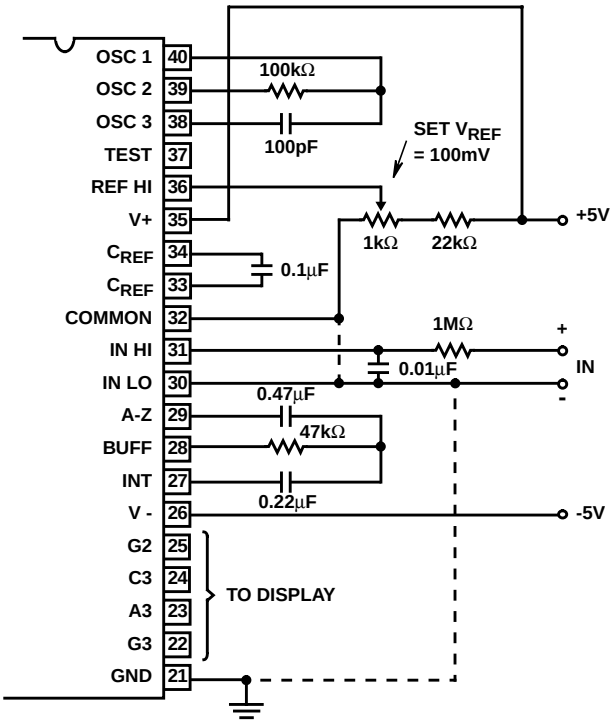
NOTE #	DESCRIPTION	AnswerFAX DOC. #
AN016	"Selecting A/D Converters"	9016
AN017	"The Integrating A/D Converter"	9017
AN018	"Do's and Don'ts of Applying A/D Converters"	9018
AN023	"Low Cost Digital Panel Meter Designs"	9023
AN032	"Understanding the Auto-Zero and Common Mode Performance of the ICL7136/7/9 Family"	9032
AN046	"Building a Battery-Operated Auto Ranging DVM with the ICL7106"	9046
AN047	"Games People Play with Intersil' A/D Converters," edited by Peter Bradshaw	9047
AN052	"Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"	9052

Typical Applications



Values shown are for 200mV full scale, 3 readings/sec., floating supply voltage (9V battery).

FIGURE 11. ICL7116 USING THE INTERNAL REFERENCE



Values shown are for 200mV full scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

FIGURE 12. ICL7117 USING THE INTERNAL REFERENCE

Typical Applications (Continued)

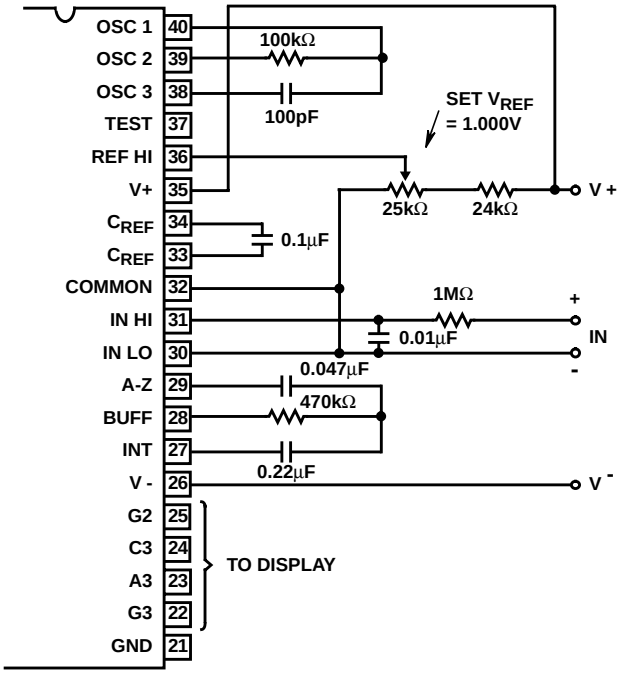
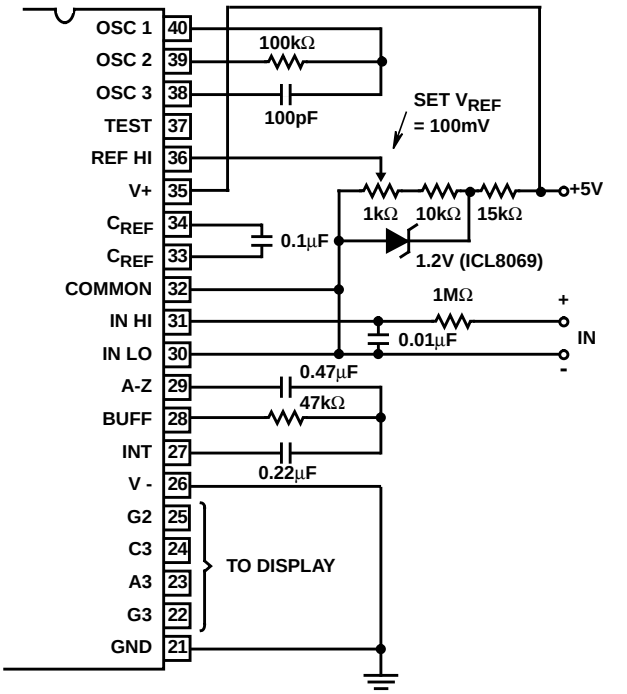
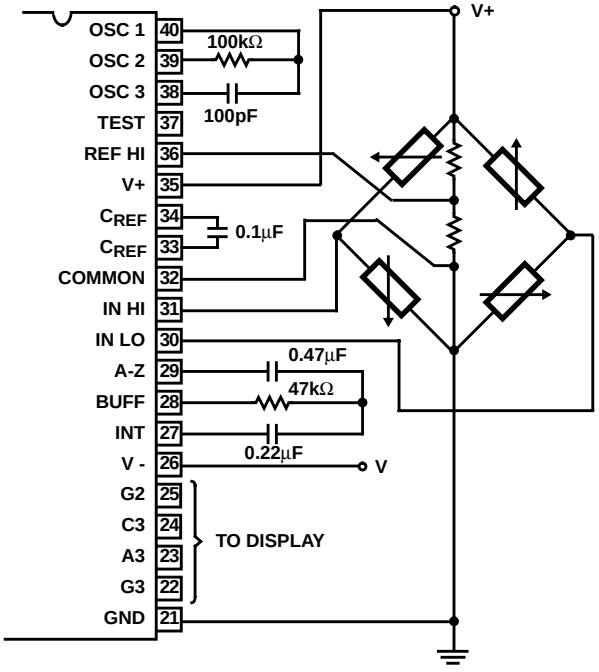


FIGURE 13. ICL7116 AND ICL7117: RECOMMENDED COMPONENT VALUES FOR 2.0V FULL SCALE



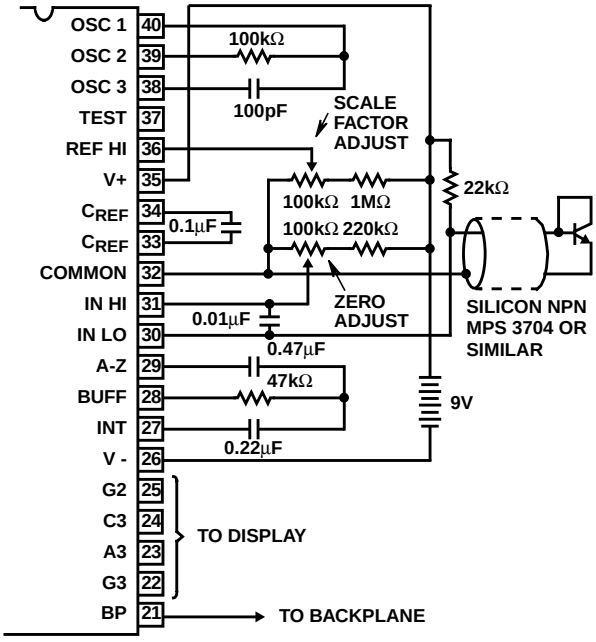
An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

FIGURE 14. ICL7117 OPERATED FROM SINGLE +5V SUPPLY



The resistor values within the bridge are determined by the desired sensitivity.

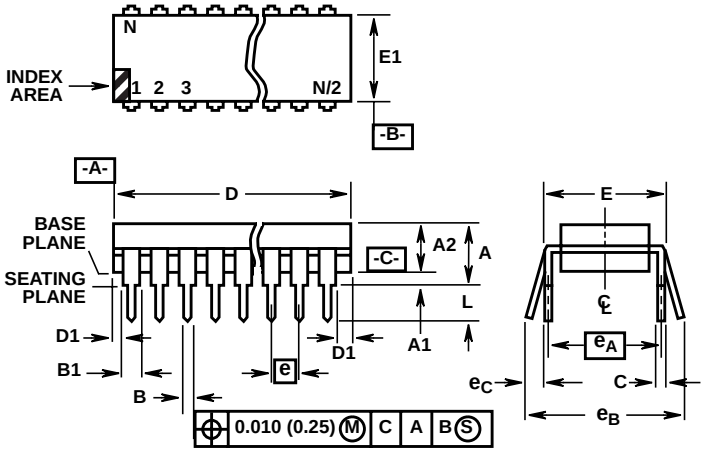
FIGURE 15. ICL7117 MEASUREING RATIOMETRIC VALUES OF QUAD LOAD CELL



A silicon diode-connected transistor has a temperature coefficient of about -2mV/^{0}C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

FIGURE 16. ICL7116 USED AS A DIGITAL CENTIGRADE THERMOMETER

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

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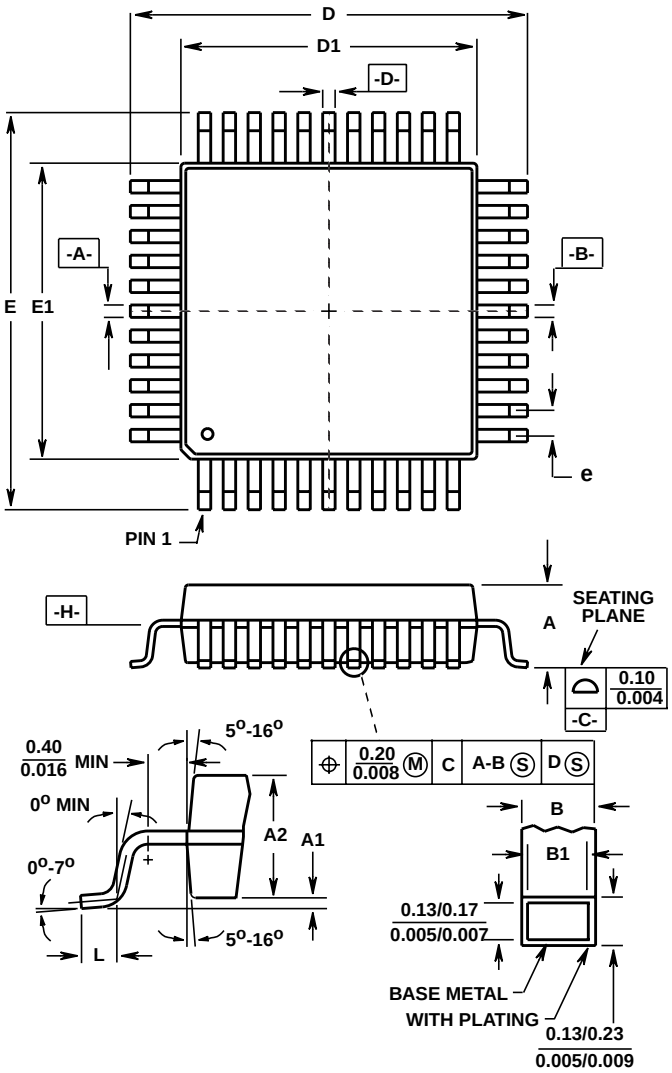
Metric Plastic Quad Flatpack Packages (MQFP/PQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

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