

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4006B

MSI

18-stage static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

18-stage static shift register

HEF4006B MSI

DESCRIPTION

The HEF4006B is an 18-stage shift register arranged as two 4-stage and two 5-stage shift registers with a common clock input (\overline{CP}). The two 4-stage shift registers each have a data input (D_A, D_B) and a data output (O_{3A}, O_{3B}); the two

5-stage shift registers each have a data input (D_C, D_D) and data outputs from the fourth and fifth stages ($O_{3C}, O_{4C}, O_{3D}, O_{4D}$).

The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data are shifted into the first register position of each register from the data inputs (D_A to D_D) and all the data in each register are shifted one position to the right on the HIGH to LOW transition of \overline{CP} .

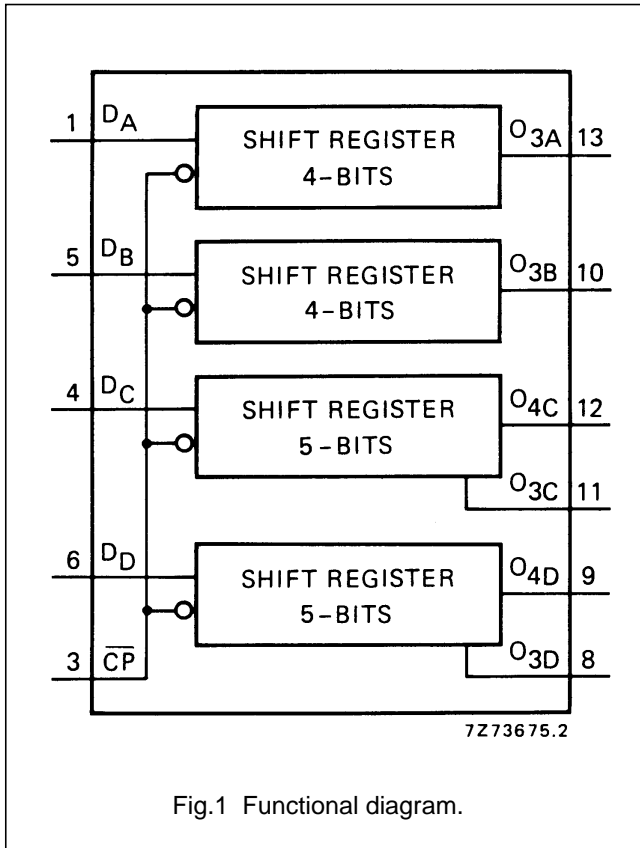


Fig.1 Functional diagram.

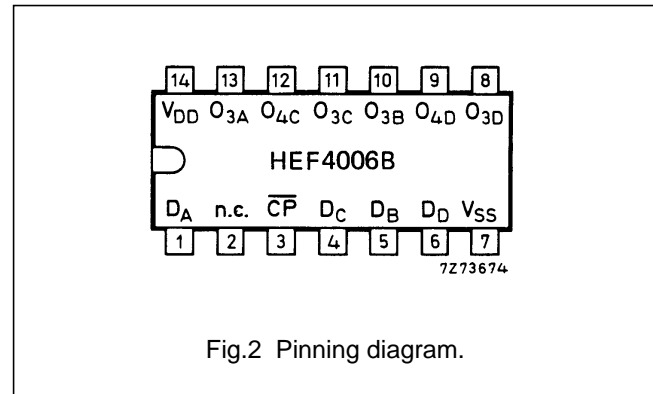


Fig.2 Pinning diagram.

FUNCTION TABLE

D_n	\overline{CP}	$O_n^{(5)}$
D_1		D_1
X		no change

Notes

- X = state is immaterial
- = positive-going transition
- = negative-going transition
- D_1 = either HIGH or LOW
- The moment D_1 appears at O depends on the register length.

- HEF4006BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4006BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4006BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America

PINNING

- D_A to D_D data inputs
- \overline{CP} clock input (HIGH to LOW; edge-triggered)
- O_{3A} to O_{3D} ; O_{4C} ; O_{4D} data outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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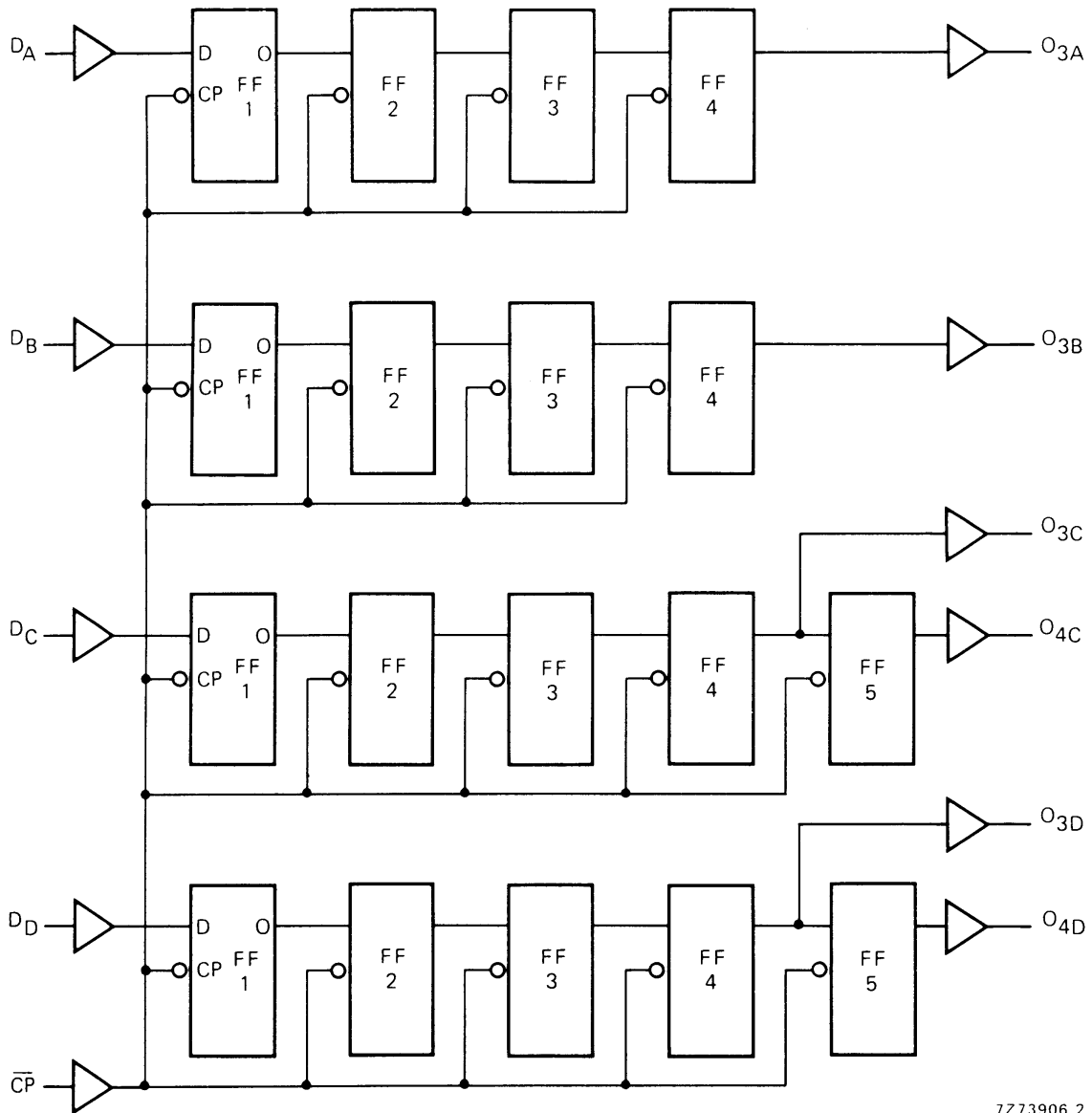


Fig.3 Logic diagram.

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN	TYP	MAX	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $\overline{CP} \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{PLH}		90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10		40	85	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
Minimum clock pulse width; HIGH	5	t_{WCPH}	60	30		ns	see also waveforms Fig.4
	10		40	20		ns	
	15		30	15		ns	
Set-up time $D_n \rightarrow \overline{CP}$	5	t_{su}	20	10		ns	
	10		10	5		ns	
	15		5	0		ns	
Hold time $D_n \rightarrow \overline{CP}$	5	t_{hold}	5	-5		ns	
	10		5	0		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f_{max}	9	18		MHz	
	10		15	30		MHz	
	15		18	36		MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$600 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3200 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$11\ 600 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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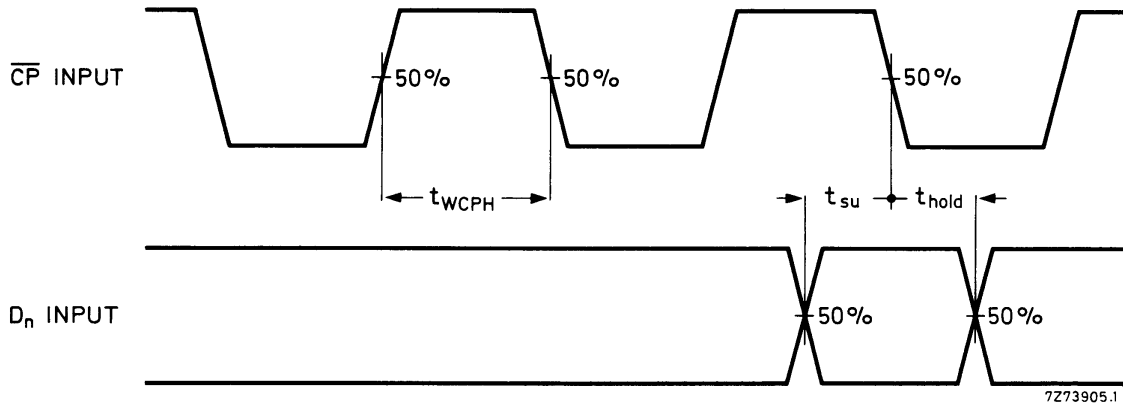


Fig.4 Waveforms showing minimum clock pulse width, and set-up and hold-times for D_n to \overline{CP} . Set-up and hold times are shown as positive values but may be specified as negative values.