INTEGRATED CIRCUITS EQUIVALENTS LIST

COMMERCIAL VERSIONS

Type No.	*Mullard equivalent*	*Type No.*	*Mullard comparable types*
DTL range		**TTL range**	
– RC 206	FCH 141	7400N	FJH131
	FCL 101	7401N	FJH231
– RC 210	FCH 221	7402N	FJH221
– RC 216	FCH 151	7410N	FJH121
	FCK 101	7420N	FJH111
– RC 224	FCH 101	7430N	FJH101
– RC 225	FCJ 101	7440N	FJH141
– RC 226	FCH 161	7441AN	FJL101
– RC 227	FCY 101	7450N	FJH151
– RC 231	FCH 121	7451N	FJH161
– RC 234	FCH 111	7453N	FJH171
– RC 236	FCH 171	7460N	FJY101
– RC 246	FCH 181	7470N	FJJ101
– RC 261	FCH 131	7472N	FJJ111
– RC 266	FCH 191	7473N	FJJ121
– RC 286	FCH 201	7474N	FJJ131
– RC 296	FCH 211	7475N	FJJ181
		7476N	FJJ191
		7490N	FJJ141

MILITARY VERSIONS

DTL range

Type No.	*Mullard equivalent*	*Type No.*	*Mullard equivalent*
		– RM 227	FCY 102
– RM 206	FCH 142	– RM 231	FCH 122
	FCL 102	– RM 210	FCH 112
– RM 210	FCH 222	– RM 236	FCH 172
– RM 216	FCH 152	– RM 246	FCH 182
	FCK 102	– RM 261	FCH 132
– RM 224	FCH 102	– RM 266	FCH 192
– RM 225	FCJ 102	– RM 286	FCH 202
– RM 226	FCH 162	– RM 296	FCH 212

D.T.L. NAND/NOR SEXTUPLE INVERTER GATE

FCH211

TENTATIVE DATA

The FCH211 is a monolithic sextuple diode-transistor logic inverter gate with collector resistors. By connecting the output of two or more gates the NOR function can be performed.

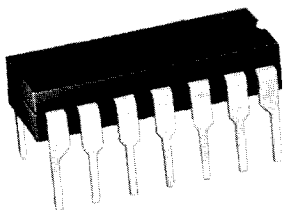
QUICK REFERENCE DATA		
Supply voltage (nominal)	+6.0	V
Operating temperature range	0 to +75	^{o}C
Fan-in capability using expander diode array FCY101	14	
Fan-out capability (full temperature range)	8	
Signal noise immunity ('Low') at 25^{o}C (typ.)	1.2	V
Average propagation delay Fan-out=6, C_L=60pF	31	ns
Average power dissipation per gate 50% duty cycle, T_{amb}=25^{o}C	11	mW

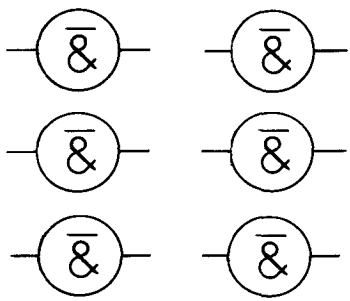
Unless otherwise stated data applies to individual gates

OUTLINE

Dual in-line package

For details see General Explanatory Notes





LOGIC FUNCTION

The logic function is a 'NAND' function when the most positive voltage is a '1' and a 'NOR' function when the most positive voltage is a '0'. All inputs are to be 'High' in order for the output to be 'Low'. Any 'Low' input will give the output 'High'.

DESIGN DATA

Over the full temperature range 0 to 75°C

	Min.	Nom.	Max.	
Supply				
Supply voltage	5.7	6.0	6.3	V
Current consumption from supply per gate				
Output 'Low' V supply = 6.0V	-	2.6	-	mA
V supply = 6.3V	-	-	4.2	mA
Output 'High' V supply = 6.0V	-	1.3	-	mA
V supply = 6.3V	-	-	2.0	mA
Input				
Voltage for 'High' input state S.N.I. = 0	2.3	-	6.3	V
S.N.I. = 1.6V	3.9	-	6.3	V
Current for 'High' input state	-	-	25	μA
Voltage for 'Low' input state S.N.I. = 0	-	-	0.8	V
S.N.I. = 0.4V	-	-	0.4	V
Current for 'Low' input state (full temperature range, see curve on page C2 for other temperatures)	-	-	2.0	mA
Input capacitance (equivalent)	-	7.0	-	pF
Output				
Voltage for 'High' output state (max. loading)	3.9	-	6.3	V
Voltage for 'Low' output state	-	-	0.4	V
Current capability at 'Low' output state (full temperature range, see curve on page C2 for other temperatures)	-	-	12.6	mA
Collector load resistance	-	4.4	-	kΩ
Output capacitance (equivalent)	-	25	-	pF
D.C. Fan-out				
1. Uniform system temperature and voltage	-	-	8	
2. Uniform system temperature, adjacent circuits at extremes of supply voltage	-	-	7	
3. Adjacent circuits at extremes of temperature and supply voltage	-	-	6	

Wired 'OR' capability

For details see curve on page C3

Truth table (for two input terminals)

Input 1	Input 2	Output
Low	Low	High
High	Low	High
Low	High	High
High	High	Low

The 'High' state normally corresponds to a voltage level between 3.9 and 6.3V.
The 'Low' state normally corresponds to a voltage level between 0 and 0.4V.

PERFORMANCE

	Min.	Nom.	Max.	
Signal noise immunity 'Low' state	400	-	-	mV
'High' state	1.6	-	-	V
(full temperature range, see curve on page C1 for other temperatures)				
Average propagation delay time	-	42	-	ns

CHARACTERISTICS (Supply voltage = +6.0V, $T_{amb} = 25^{o}C$)

		Min.	Nom.	Max.	
V_{TH} 'Low'	Input threshold voltage for 'Low' input state ($V_{out} = 5.6V$, $I_{out} = 0$)	1.0*	-	-	V
V_{TH} 'High'	Input threshold voltage for 'High' input state ($I_{out} = 14.4mA$)	-	-	2.2*	V
V_{out} 'Low'	Output voltage for 'Low' output state ($V_{in} = 2.2V$, $I_{out} = 14.4mA$)	-	-	0.4*	V
V_{out} 'High'	Output voltage for 'High' output state ($V_{in} = 1.0V$, $I_{out} = 0$)	5.6*	-	-	V
I_{in} 'Low'	Input current for 'Low' input state ($V_{in} = 0.4V$)	-	-	1.8*	mA
I_{in} 'High'	Input current for 'High' input state ($V_{in} = 6.0V$, all other inputs = 0)	-	-	1.0	μA
t_{pdr}	Rise propagation delay time				
	Fan-out = 1, $C_L = 40pF$	-	50	85	ns
	Fan-out = 6, $C_L = 60pF$	-	30	70	ns
t_{pdf}	Fall propagation delay time				
	Fan-out = 1, $C_L = 40pF$	-	26	65	ns
	Fan-out = 6, $C_L = 60pF$	-	32	85	ns

*These are the characteristics which are recommended for acceptance testing purposes.
See curves for other conditions, and explanatory notes for measuring methods.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

Maximum positive supply voltage (pin 7)	8.0	V
Maximum positive output voltage (pins 1, 3, 5, 8, 10 and 12)	8.0	V
Maximum negative output voltage	0	V
Maximum positive voltage on inputs (pins 2, 4, 6, 9, 11 and 13)	8.0	V
*Maximum negative input current	20	mA

*The maximum negative voltage allowed on the input pins is limited by the current drawn. At 20mA this voltage is typically 0.6V.

Temperature

T_{stg} min.	-35	°C
T_{stg} max.	125	°C
T_{amb} min. operating	0	°C
T_{amb} max. operating	75	°C

PINNING

12.	Output gate 1	4.	Input gate 2
10.	" " 2	6.	" " 3
8.	" " 3	9.	" " 4
5.	" " 4	11.	" " 5
3.	" " 5	13.	" " 6
1.	" " 6	7.	Positive supply
2.	Input gate 1	14.	Common and earth

CIRCUIT DIAGRAM