Silicon diffused power transistors — BU508A; BU508D

High-voltage, high-speed switching npn transistor in SOT93A envelope intended for use in horizontal deflection circuits of colour television receivers. The BU508D has an integrated efficiency diode.

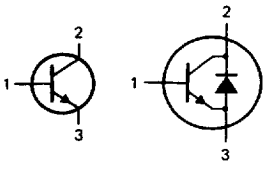
QUICK REFERENCE DATA

Collector-emitter voltage peak value; V_{BE} = 0	V_{CESM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (DC)	I_C	max.	8 A
Collector current peak value	I_{CM}	max.	15 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125 W
Collector-saturation voltage I_C = 4.5 A; I_B = 2 A	V_{CEsat}	max.	1 V
Saturation collector current	I_{Csat}	typ.	4.5 A
Diode forward voltage (BU508D) I_F = 4.5 A	V_F	typ.	1.6 V
Fall time I_{CM} = 4.5 A; $I_{B(on)}$ = 1.4 A	t_f	typ.	0.7 µs

MECHANICAL DATA

Dimensions in mm

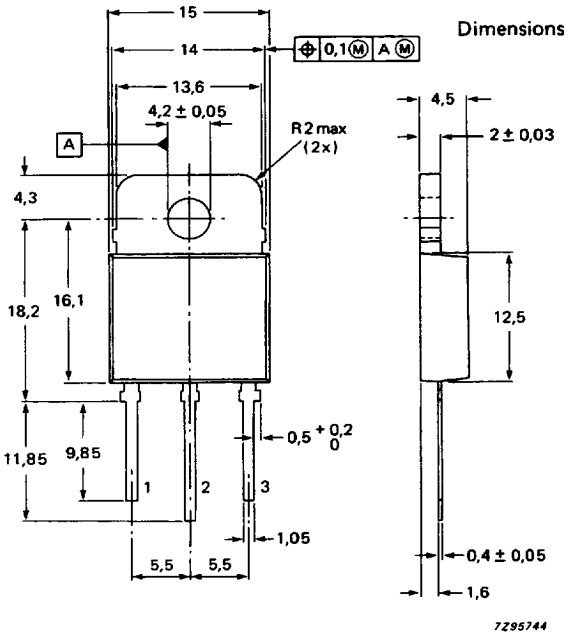
Fig. 1 SOT93A.



BU508A BU508D

1 = base
2 = collector
3 = emitter

Collector connected to mounting base.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage peak value; V_{BE} = 0	V_{CESM}	max.	1500 V
Collector-emitter voltage (open base)	V_{CEO}	max.	700 V
Collector current (DC)	I_C	max.	8 A
Collector current peak value	I_{CM}	max.	15 A
Base current (DC)	I_B	max.	4 A
Base current (peak value)	I_{BM}	max.	6 A
Reverse base current (DC or average over any 20 ms period)	$-I_{B(AV)}$	max.	100 mA
Reverse base current* (peak value)	$-I_{BM}$	max.	5 A
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	125 W
Storage temperature range	T_{stg}		−65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	=	1 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current**			
V_{BE} = 0; V_{CE} = $V_{CESMmax}$	I_{CES}	max.	1 mA
V_{BE} = 0; V_{CE} = $V_{CESMmax}$; T_j = 125 °C	I_{CES}	max.	2 mA
Emitter cut-off current			
V_{EB} = 6 V; I_C = 0	I_{EBO}	max.	10 mA
Collector-emitter sustaining voltage			
I_B = 0; I_C = 100 mA; L = 25 mH	$V_{CEOsust}$	min.	700 V
Saturation voltages			
I_C = 4.5 A; I_B = 2 A	V_{CEsat}	max.	1 V
	V_{BEsat}	max.	1.3 V
DC current gain			
I_C = 100 mA; V_{CE} = 5 V	h_{FE}	min.	6
	h_{FE}	typ.	13
	h_{FE}	max.	30
Transition frequency at f = 5 MHz			
I_C = 0.1 A; V_{CE} = 5 V	f_T	typ.	7 MHz
Collector capacitance at f = 1 MHz			
$I_E = I_e$ = 0; V_{CB} = 10 V	C_c	typ.	125 pF

* Turn-off current.

** Measured with half-sinewave voltage (curve tracer).

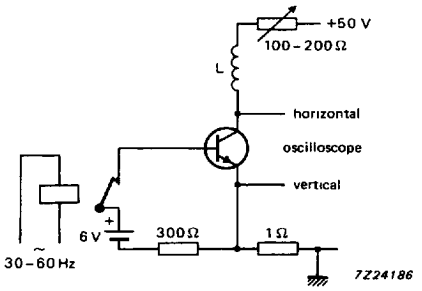


Fig. 2 Test circuit for $V_{CEOsust}$.

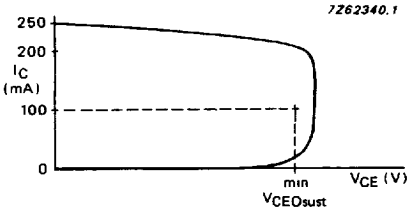


Fig. 3 Oscilloscope display for $V_{CEOsust}$.

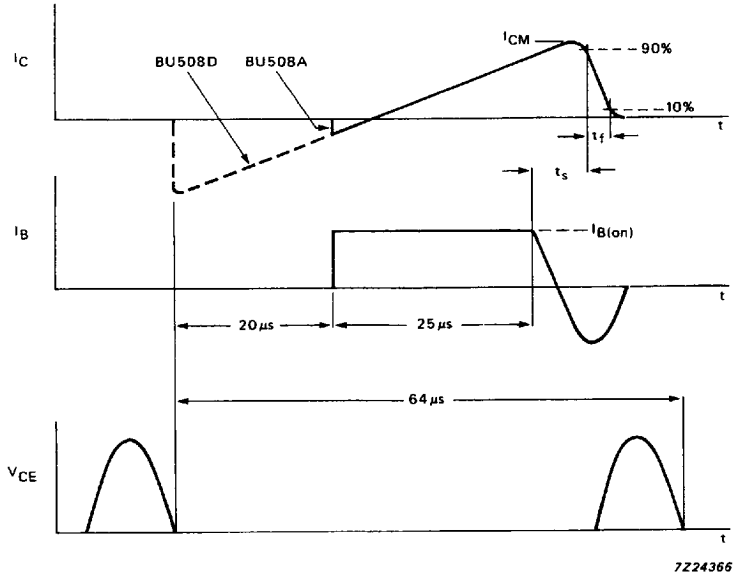


Fig. 4 Switching times waveforms; I_{CM} = 4.5 A; $I_{B(on)}$ = 1.4 A; L_B = 6 μH; $-V_{BB}$ = 4 V; $-dI_B/dt$ = 0.6 A/μs; typical value of t_s = 6.5 μs; typical value of t_f = 0.7 μs.

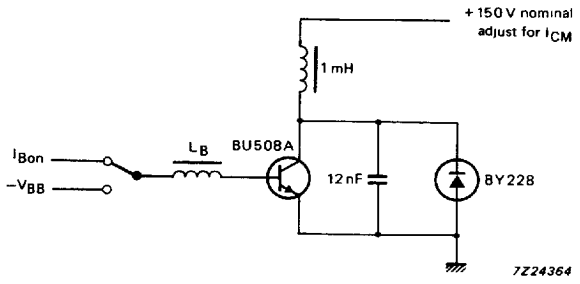


Fig. 5 Switching times test circuit (BU508A).

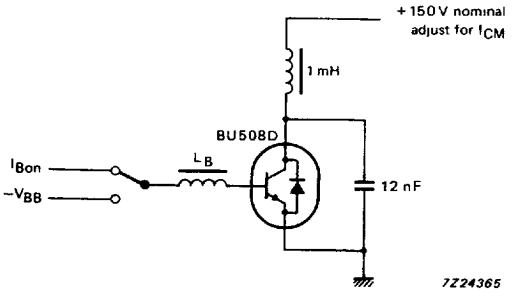
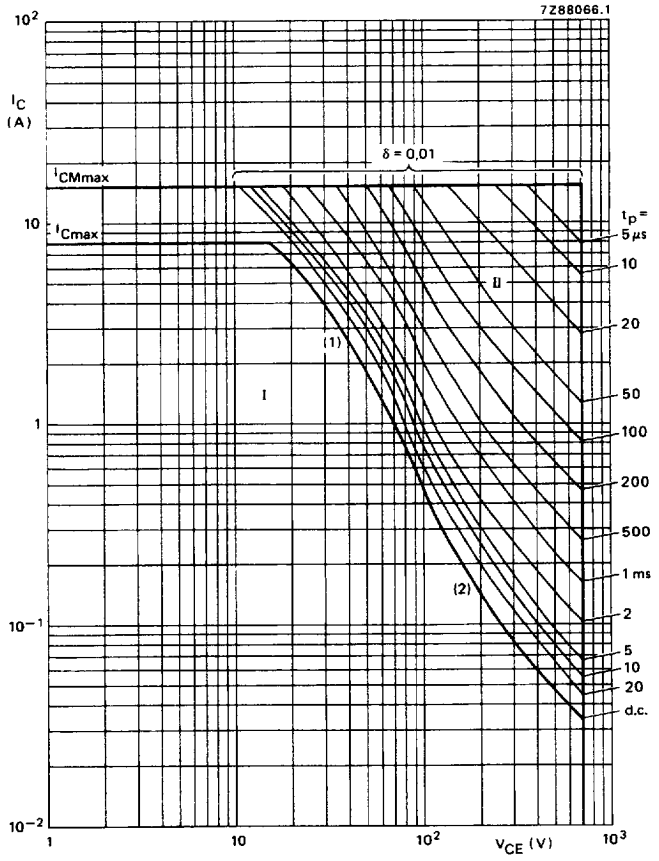


Fig. 6 Switching times test circuit (BU508D).



(1) $P_{tot\ max}$ line.
(2) Second-breakdown limits (independent of temperature).
I Region of permissible DC operation.
II Permissible extension for repetitive pulse operation.

Fig. 7 Safe operating area; $T_{mb} < 25\ ^oC$.

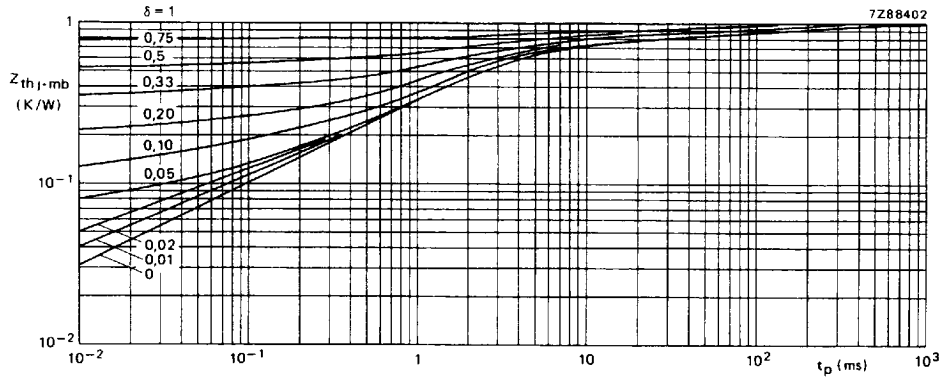


Fig. 8 Pulse power rating chart.

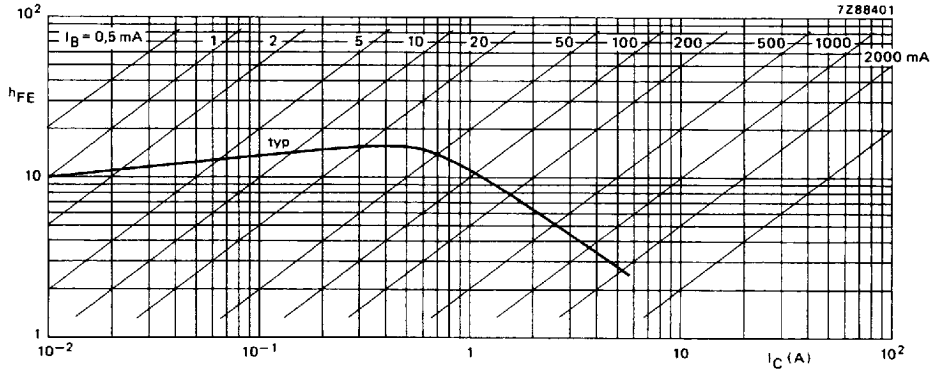


Fig. 9 Typical values DC current gain at V_{CE} = 5 V; T_{mb} = 25 °C.

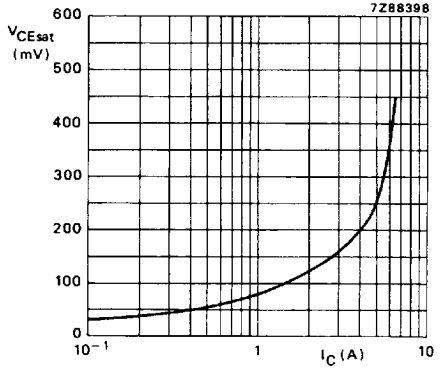


Fig. 10 Typical values I_C/I_B = 2; T_j = 25 °C.

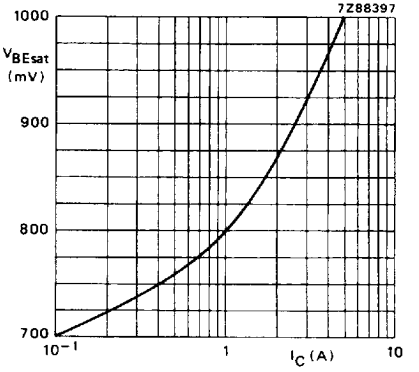


Fig. 11 Typical values I_C/I_B = 2; T_j = 25 °C.

APPLICATION INFORMATION – HORIZONTAL DEFLECTION CIRCUIT WITH BU508A/D

In designing horizontal deflection circuits, allowance has to be made for component and operating spreads in order not to exceed any Absolute Maximum Rating. Extensive analysis has shown that, for the peak collector current and the collector emitter voltage of the output transistor, the total allowance need not be higher than 15% and, the following recommended base-drive and heatsink conditions are based on this figure.

To simplify the presentation the design curves given refer to nominal conditions. Where the collector current will be modulated by the E-W correction circuit the average value of the peak collector current applies, if the modulation is less than 10%.

The BU508D is a BU508A with an integrated efficiency diode without a parasitic base-emitter resistor. Therefore a circuit optimized for a BU508A can use a BU508D without alterations. N.B. if a BU508D is used total device dissipation is increased due to the integrated diode losses.

To obtain a short fall time and minimum turn-off dissipation, with a high-voltage transistor, the storage time must be sufficiently long and, during turn-off, the negative base-emitter voltage must be sufficiently high. Both requirements can easily be realized by including a small coil in series with the base of the output transistor. To reduce base current variations a series base resistor is added to most designs. This has the disadvantage of reducing the energy in the base inductance during turn-off which, in turn, reduces the negative base-emitter voltage. This with large resistor values may lead to an insufficient negative voltage for correct device turn-off. This can be improved by providing a shunt diode or capacitor in parallel with the base resistor. Instead of giving various detailed base circuits based on these considerations, it is a more direct approach to specify the recommended $-dI_B/dt$ (see Fig. 15).

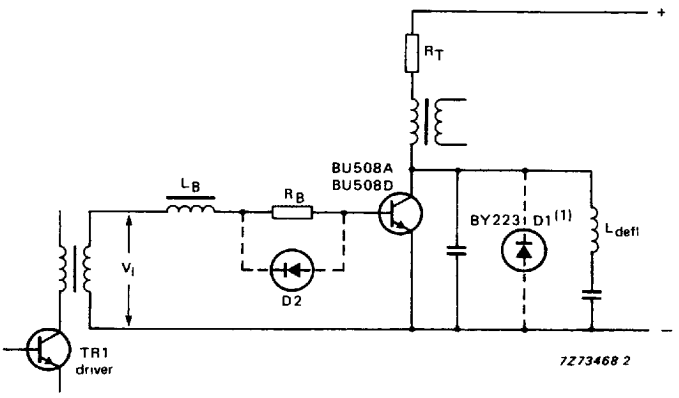
The maximum transistor dissipation depends largely on the tolerance in the drive conditions. The dissipation given in Fig. 16 allows for base current and $-dI_B/dt$ tolerances of ± 15%. The curve applies to a limit-case transistor at a mounting base temperature of 85 °C. The thermal resistance for the heatsink can be calculated from:

$$R_{th\ mb\text{-}a} = \frac{85 - T_{amb\ max}}{P_{tot\ max}}$$

In which $T_{amb\ max}$ is the maximum ambient temperature of the transistor.

In order to assure a value of thermal resistance at which thermal stability is achieved, the minimum value for T_{amb} in the above equation is 45 °C.

APPLICATION INFORMATION (continued)



(1) Not required for this circuit when BU508D is used.

Fig. 12 Simplified horizontal deflection circuit.

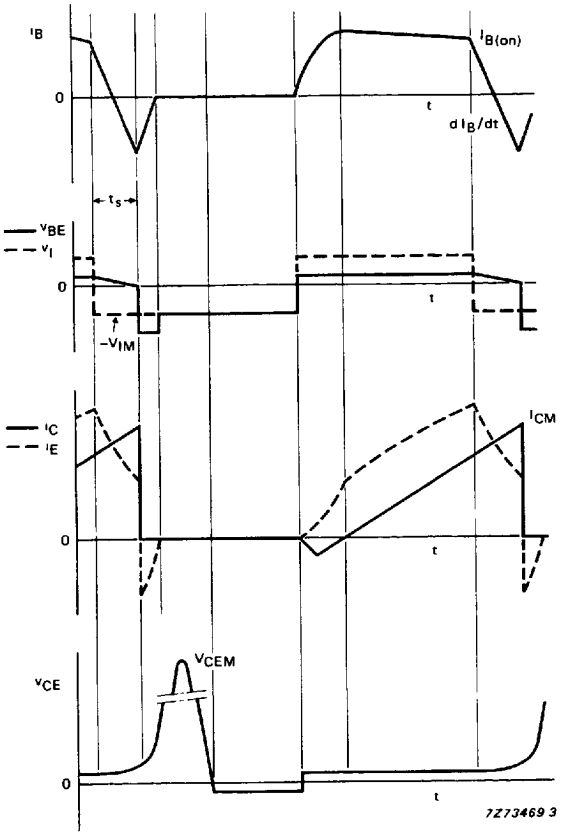


Fig. 13 Fundamental waveforms (BU508A).

APPLICATION INFORMATION (continued)

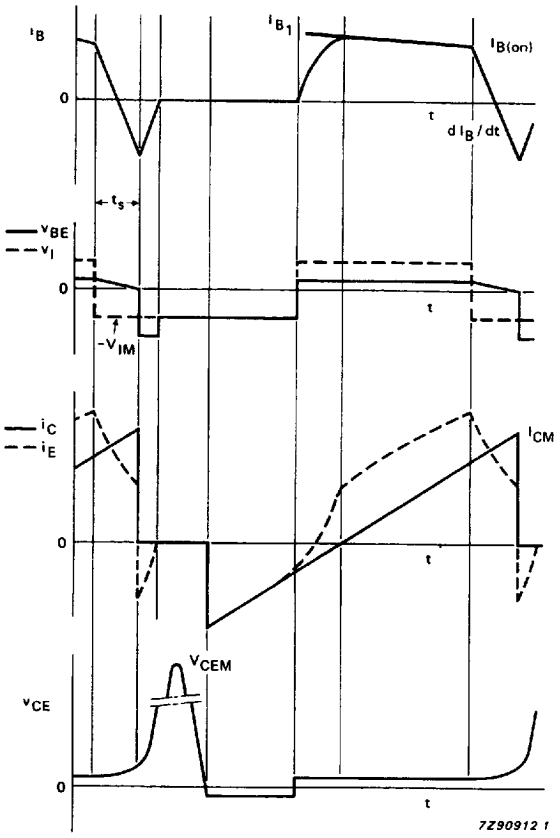


Fig. 14 Fundamental waveforms (BU508D).

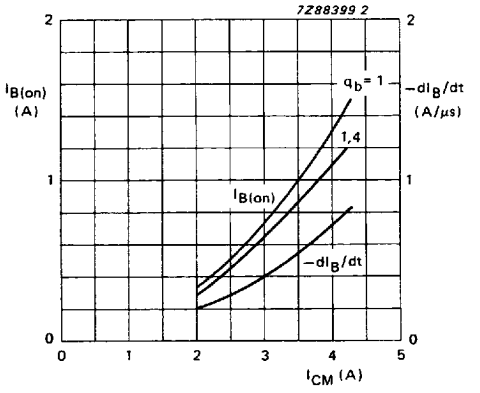


Fig. 15 Nominal end value of the base current and its rate of fall during turn-off as a function of nominal peak collector current.
A 15% spread allowance is included on these nominal values. Q_B is defined as $I_{B1}/I_{B(on)}$ (see Fig. 14).
The reverse drive voltage during the storage and fall time ($-V_{IM}$) must be > 2 V.

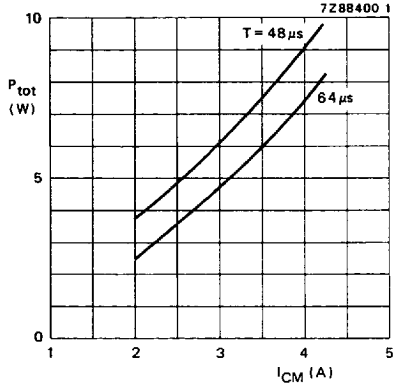


Fig. 16 Total dissipation of a limit-case transistor under maximum operating conditions for 625 and 819 lines ($T_{mb} = 85$ °C).